THE CUSTOMER APPROACH IN THE DESIGN OF ASIC FOR INDUSTRIAL ELECTRONICS

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1. SUMMARY

The IC design center in the customer company oriented to use ASIC has to bridge over a lot of conflicting requirements in order to be successful interface between electronic system development and modern microelectronic technology. To be able to guess the usefulness of ASIC in the application field of the industrial electronics, it is important to understand the general model of the electronic controlled process. In the paper also a few developed ASIC are described, their common characteristics are pointed out, some expected trends are mentioned, and our criteria in use of ASIC are discussed.

2. THE CONFLICTING POINTS IN THE ACTIVITY OF IC DESIGN CENTER (ICDC) IN THE CUSTOMER COMPANY

The ASIC customer company described in the paper comes from the field of the industrial electronics with the main involvement in the production of the power system protection equipment, energy converters, data processing and control systems, household appliances, motor drives etc. The ASIC required often combines analog as well as digital functions on the same chip. Only small or moderate annual volume of the chips is foreseen, i.e. 100.000 of those chips may be required per year at the beginning of the ICDC activity. The conflicting points derive from the task that ICDC has to be successful interface between the electronic system designers in the house and the modern microelectronic technology in the silicon foundries.

2.1. System design

The "built in" advantage of ASIC is that it doesn't allow the changes of project after the circuit layout has been finished. Therefore the step of defining the electronic system requirements (where ASIC is still the black box) is emphasized. System description includes functional description with the transfer functions, I/o electrical signals specification, reliability requirements and the real world influence (atmospheric, noise, radiation etc.). If the probability of using ASIC is high enough, IC designer has to be the member of the team in the very beginning of the project definition. His/her task is to influence system engineers to take into account the possible ASIC level of integration as the criterion of the system "Floor-planning". The output of that step we call "System Technical Requirements". The document has to be unambigous and complete, because system engineers like to change the requirements after that step has been finished, and IC designer is in inferior psychological position because his/her knowledge of the particular system is less than their. We would like to stress that the IC designer involvement in the system definition expressed in man-month is almost the same as in all remaining steps of the IC design job (Table 1.).

Steps in ASIC design procedure	IC designer (man-month)	Schedule for ASIC (time in month)
System design	4	x " + 1
ASIC design	3	2
ASIC processing	1	2 - 3
Evaluation	1	1

Notes:

") x counts electronic system development time independent of the use of ASIC.

1) IC designer man-month include all service activities i.e. technician, draughtman, etc., so that it is more expensive than usually.

2) The data given in the Table refer to the ASIC of moderate complexity, i.e. gate array of 500 equivalent NAND gates or MSI analog circuit.

Table 1. Man-months and time in ASIC design procedure.

2.2. Silicon foundry

The troubles with silicon foundries often start from "too small" overall annual quantity of ASIC to be processed. Some manufactures insist on annual business rate. In our opinion the better approach from the silicon foundry side is to separate ASIC developing from ASIC production expenses. The silicon foundry technologies (or cell libraries) would have to tend to become standardized for particular technology so that second source problem disappears. The silicon compilers will be good solution too, but that way of achieving the technological independence doesn't annihilate the expenses of mask plates in the case of changing the silicon foundry partnership.

2.3. Physical layout

The physical design is an integral part of the circuit design procedure. The technological origin of the design rules influences circuit design and provokes the changes in circuit shematic too. The circuit designer, not the technologist, is the right person to do resimulation. The troubles arise with the physical design rules because silicon foundry prefers to release the more rigid design rules to the customer than for themselves. The chip silicon area is obviously sacrificed when the customer makes the IC layout and PG tape.

2.4. ASIC evaluation

ASIC evaluation has three separate steps:

- -incoming inspection (parametric and functional testing with automatic test equipment; reliability if reguired),
- application evaluation (protoboarding in simulated real conditions),
- exploitation evaluation (prototype in real conditions).

The incoming inspection is the part of IC designer job whereas the application and exploitation is the part of system engineers job (which is similar as in the case of classical PCB). The initial ASIC testing is done by silicon foundry with its automatic test equipment (ATE). Testability and test program generation have to be solved formerly. The question is if the customer need for the incoming inspection accounts for the high expenses of buying ATE. Probably we are too suspicious in the silicon foundry output but we have interesting experience with the standard IC suppliers. Their delivery's quality were much higher when they realized that we had introduced 100 % incoming inspection! The compromising solution is to test ASIC with neutral partner equipped with ATE. Is it possible to find at the market cheap ATE for non-standard, medium complexity, medium performance IC?

3. CHARACTERISTICS OF ASIC IN THE INDUSTRIAL ELECTRONICS

The general model of the electronic controlled industrial process is shown on Figure 1. In the sen-

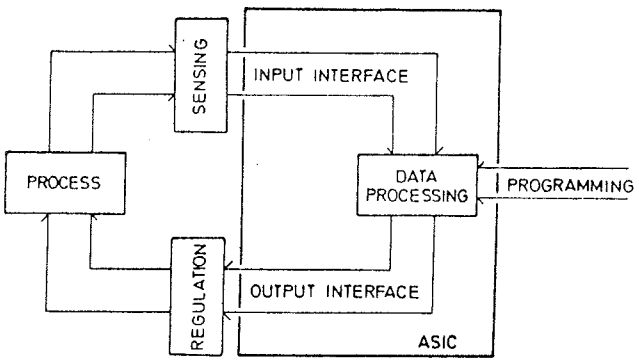

Fig.1 Model of electronically controlled industrial process

sing block the physical values of the process are transformed into electrical values adapted for the use in the data processing block. Its output (processed electrical signals) drives the process parameters regulation block in which the electrical signals are transformed back to the physical values for the process control. In general, the structure of those

blocks and I/O interfaces between them depends on the kind of the process. The structure of the sensing block is usually built by such elements: precise operational amplifiers and comparators, A/D converters and transducers, filters, transformers, opto-couplers, etc. The output are low level signals. The regulation block, which deals with high level signals (power control), contains power transistors, thyristors, transformers, heating elements, motors etc. The data processing block, which is always the core of the possible ASIC, contains: analog, digital or, the most frequently, mixed analog-digital elements of the data processing. The choice of the technology (including either monolithic or hybrid) and also the economics of ASIC are influenced by the way of the data processing (analog or digital), onter part of the system (voltage supply, programmability, etc.) and atmospheric.

Gate array technique mainly makes possible realization of digital functions. Standard cell technique, on the contrary, allows integration of more complex functions (e.g. RAM, ROM, etc.) or analog blocks (e.g. amplifiers, comparators, SC circuits, etc.). For small production volumes such an approach is economically unaccep table, although it offers integration of the greatest part of the sensing and regulation blocks. Sacrificing ASIC area, the same result, but with considerable lower development costs, offers hybrid (thin or thick film). In addition to extended voltage and current range and greater power dissipation, this technique also offers broard choice of standard electronic devices. Besides that, the technique may combine the high quality analogue capabilities of the thick film hybrid with the outstanding digital performance of the gate array (GA).

4. ASIC EXAMPLES

Through a few examples of developed ASIC we will try to work out some common characteristics of those circuits and further necessities for such type of circuits in the house. Smaller quantities of chips direct us infallibly to GA design methodology. Two such circuits in their environment are given on Figures 2. and 3.: ASIC overpressure and fan controller in mine elec-

ASIC Character.	household appliances	μprocessor control	power syst. protection	power syst. protect.
Application field				
Technology	5 μm CMOS	5 μm CMOS	7 μm CMOS	thick film
Methodology	std.cells	GA	GA	-
Foundry	Iskra ME Ljubljana	Iskra ME Ljubljana	Ei-Niš	Iskra HIPOT
Complexity	1100 gates	500 gates	150 gates	MSI/LSI
Pins count	28	18	24	40
Power consum.	not critic	not critic	not critic	not critic
Max. clock	1 kHz	2,5 MHz	10 Hz	-
Interface to foudry	schematic + test alg.	layout + test alg.	PG tape + test.alg.	schematic

Table 2. Some characteristics of developed ASIC

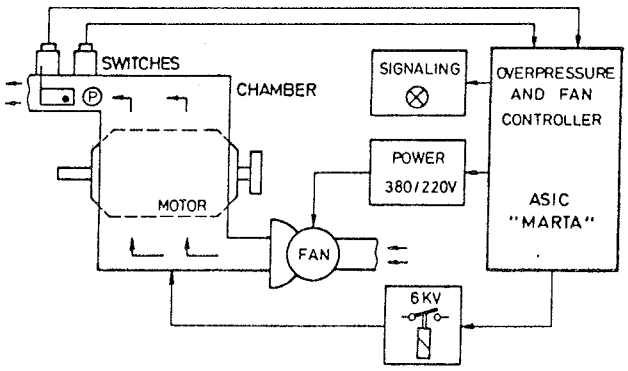

Fig.2 Overpressure and fan control system

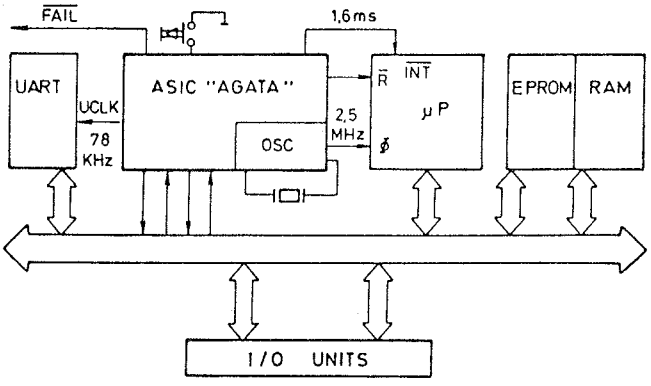

Fig.3 Time base for microprocessor Z-80

tronics and ASIC for application in microprocessor control, time base and interrupt generator. Larger quantities of ASIC (what we expect in electronic devices for household appliances) condition the change of design methodology from GA to standard cell. The typical application of ASIC programmable timer in time controlled system with electronic temperature regulation for electric water heater is shown on Figure 4. Rewiew of characteristics of those examples

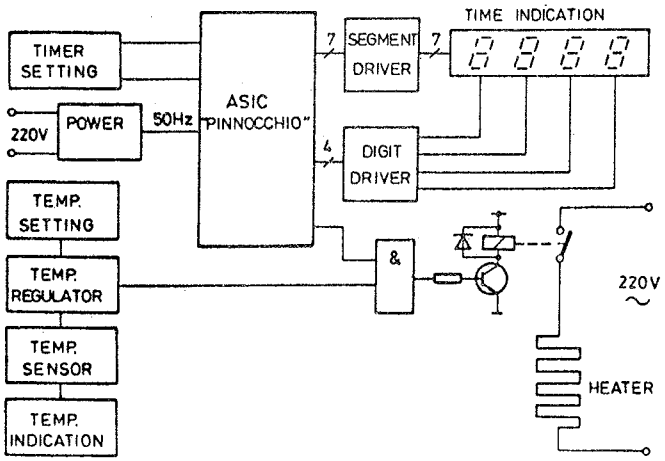

Fig.4 Example of programmable timer application in household appliances

which are digital and one mixed analog/digital circuit, is shown in Table 2. It is necessary to stress that from the project beginning we take into account all other possible applications of respective ASIC: in that way more universal function of ASIC is achieved.

With taking down future necessities for ASIC in the house, we can predict the next trends: higher complexity (with regular structures like ROM, PLA, etc.); increasing clock rates; higher output drive capabilities; increasing need for mixed analog-digital functions; increasing pin counts (influenced by SMD technology).

5. CONCLUSION

The quantifying of the technical and business criteria to choose ASIC depends on the specific situation in the country. In our case the deviation from the usually accepted facts is as follows:

- the engineer work is relatively cheap so that the expenses of designer man-month are lower. The same is for microprocessor programming so that ex post expenses are not too high. Therefore, microprocessor application on the lower level of utilization is comparable to ASIC.

- the silicon foundry service in the country is on the lower technological level, what doesen't influence actual project, but also doesn't allow to improve IC designers knowledge for more complicated circuits. Partnership with silicon foundries abroad is, among others, limited by the low annual business rate.

- the use of Asic lowers the import of standard IC, lowering the expenses and bureaucratic procedures, which makes ASIC much more attractive than classical PCB.

- the modern solution of the electronic systems improves the chances for succes on the world market.

Acknowledgment

The authors thanks to their colleagues both from ICDC and from the area of electronic systems development for the good collaboration and understanding.

Published in the Proceedings of the First Hungarian Custom Circuits Conference, pp. E43-1 to E43-8, Gyöngyös, 1987 May, Pag. 12-15.

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