HCMOS SECOND - SOURCING OF 74 SERIES BIPOLAR LOGIC

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Key Words: CMOS, HCMOS, TTL, ASIC, Bipolar Logic, Integraded Circuit, Second Sourcing

ABSTRACT: It is well known that shortages of state of the art memory and microprocessor integrated circuits are a fact of life that equipment manufacturers must learn to live with. However, it is not always realised that severe shortages of much simpler devices occur. This article will describe how an HCMOS part was designed and manufactured to replace the 74H01, a high speed quad open collector Nand gate that is no longer in production.

NADOMEŠČANJE BIPOLARNIH VEZIJ IZ SERIJE 74 S HCMOS VEZJI

Ključne besede: CMOS, HCMOS, TTL, ASIC, bipolarna logika, integrirano vezje, nadomestno vezje

POVZETEK: Trenutno pomanjkanje spominskih in mikroprocesorskih vezij na trgu je dejstvo, s katerim se morajo sprijazniti proizvajalci opreme. Manj znano dejstvo pa je, da prihaja do pomanjkanja tudi dosti bolj preprostih vezij. V članku je opisano na kakšen način je načrtano in proizvedeno HCMOS vezje z namenom zamenjati standardno bipolarno vezje 74H01, četvera zelo hitra NE-IN vrata z odprtim kolektorjem, ki ni več v redni proizvodnji.

Main Text

The customer was a computer manufacturer with a mature system that had been in production for several years. One board in this computer was a particular problem, about 20% of the devices were 74H01 and it had become impossible to source this part. The major semiconductor manufacturers had dropped it from their catalogs and the replacement device they offered had a different pinout. Either the whole board could be replaced with an ASIC or a brand new source for the 74H01 could be generated. For reasons of cost and minimum risk the customer decided to obtain a new 74H01.

The most important parameters of the 74H01 from the design viewpoint are as follows /1/:

1) Output sink current = 20mA at 0.4V at 70 deg.C

2) Normal TTL input levels of 2.0V and 0.8V worst case

3) Propagation delays of 12ns to a rising input and 15ns to a falling input, worst case, measured 1.5V to 1.5V, with a load of 25pF and 280 Ohms

It pays to read the specifications carefully. Notice the minimum and maximum d.c. parameters are specified at 70 deg. but the a.c. timing parameters are specified at 25 deg. to ease testing. The next step in this particular design is to decide on the logic to be used. There are two possibilities, shown in Figs 1 and 2.

Figure 1 combines the functions of 2 input Nand and input stage into a single gate followed by an inverter driving the large n- channel output transistor. It is an advantage to have the large internal gate capacitance of Q7 charged and discharged by single transistors, the inverter pair, Q5/Q6. However there will be some lack of matching in the input characteristics depending on which pair of devices, Q1/Q3 are controlling the gate.

In Figure 2 the opposite compromises have been made. The output transistor must be charged internally by the two p-channel devices in series, Q3 and Q4. This would seem to be a slower approach than Figure 1. But the input inverters are logically and physically identical and so will be fast and perfectly matched.

Both circuits were simulated using identical 3000/3.5μm

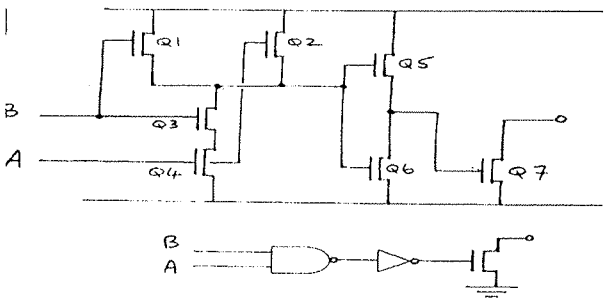

Figure 1: First approach to design 74CH01
Q1 = Q2 = 300/4
Q3 = Q4 = 1200/4
Q5 = 2000/3.5
Q6 = 800/3.5
Q7 = 3000/3.5

output transistors. This size had been determined by hand calculation to sink 20mA at 0.2V at 25 deg. As a starting point, device sizes were chosen so each stage increased in size by a factor of 3. Experience has shown this to be close to optimum. In addition, for this particular HCMOS process, the ratio of n-channel device to p-channel must be 1:2.5 for equal impedances. Before the

transistor sizes can finally be fixed for simulation, the input ratio must be chosen for TTL compatability. Again, drawing on prior experience, this was provisionally fixed at n:p = 4:1. Using these guide lines, the sizes below were compared in the circuit simulator:

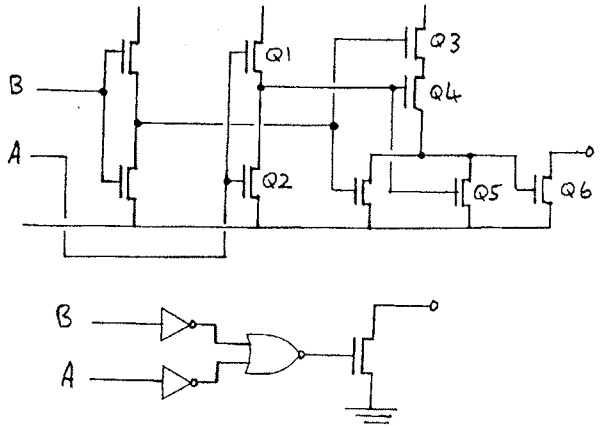

Figure 2: Second approach to design 74CH01
Q1 = 100/4
Q2 = 400/4
Q3 = Q4 = 1600/3.5
Q5 = 400/3.5
Q6 = 3000/3.5

The results were so close that there seemed little to chose between the two approaches. This is partly due to the dominant effect of the large output load capacitance, 25pF. But if we compare total channel langth for each circuit as a measure of the final active area, Fig 1 = 8800 microns, Fig 2 = 7800 microns. So even at this early stage, before any layout has begun, the Fig 2 circuit appears about 12% smaller. At this point it was decided to choose the Fig 2 circuit as it has the further advantage of better control of the input inverter.
After more simulation it was found possible to reduce the internal NOR gate to 500/125 microns instead of the first guess of 1600/400. To conclude this simulation work, the ratio of the input n-ch to p-ch transistors was varied with a mid-point TTL input of 1.6V, the corresponding output voltages are shown below:

p:n ratio	100/420	100/460	100/470	100/480	100/500
output voltage	3.45V	2.95V	2.85V	2.5V	2.0V

The input ratio of 100/480 was therefore used as this gives a mid-point output voltage for a mid-point input. The circuit is now as Fig 3. below:

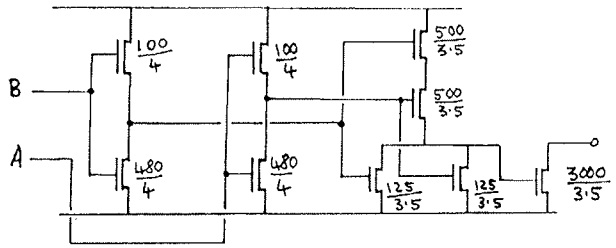

Figure 3: Final design and transistor geometries for 74CH01

Design Tolerancing

HCMOS circuit performance is dominated by two parameters, transistor threshold voltage, VT, and device gain, K', usually expressed in μA/V2. Any manufacturing process will have a spread on these parameters and it follows that the design must accomodate these variations and still perform within the specification. At 25 deg. C the total tolerances are as below:

	Min.	Typ.	Max.
p-channel threshold (V)	-0.7	-1.0	-1.3
n-channel threshold	+0.7	+1.0	+1.3
p-ch gain (uA/V2)	5	6	7
n-ch gain	18	23	28

It is clearly not possible to simulate every combination of these parameters. Some engineering judgement must be exercised in selecting combinations and based on prior experience the following parameters were considered realistic extremes on the same chip at 25 deg. C:

	Threshold Voltage (V)	Device Gain (uA/V2)
Strong p-ch	-0.7	7.0
Weak n-ch	1.0	18.0
Weak p-ch	-1.3	5.0
Strong n-ch	1.0	28.0
Typical p-ch	-1.0	6.0
Typical n-ch	1.0	23.0

The first parameters simulated
DHL = 5.5 ns
DLH = 9.5 ns
The second parameters simulated
DHL = 6.0 ns
DLH = 10.0 ns
The third, typical parameters simulated
DHL = 5.5 ns
DLH = 8.5 ns

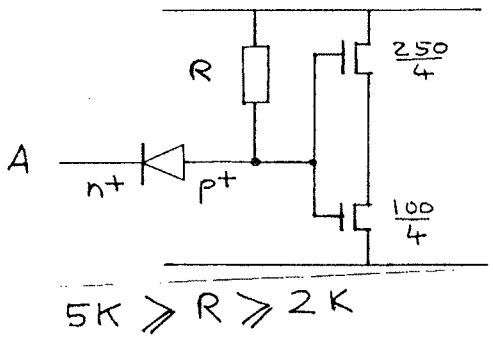

Figure 4: Possible design of the input inverter

All these results were within a comfortable margin of error of meeting the specification,

DHL = 7.5 ns typ. 12 ns max. at 25 deg

DLH = 10 ns typ. 15 ns max.

At this point the design could be considered fixed and ready for layout to begin. However, a new idea appeared! Consider the input inverter shown in Fig. 4

This copies the TTL input structure and could be implemented in HCMOS. The n+ p+ diode would sit in its own isolated n-well. This approach has the following advantages:

1) No MOS gates are exposed to external pins. This should give a robust circuit, immune from static damage possibilities.

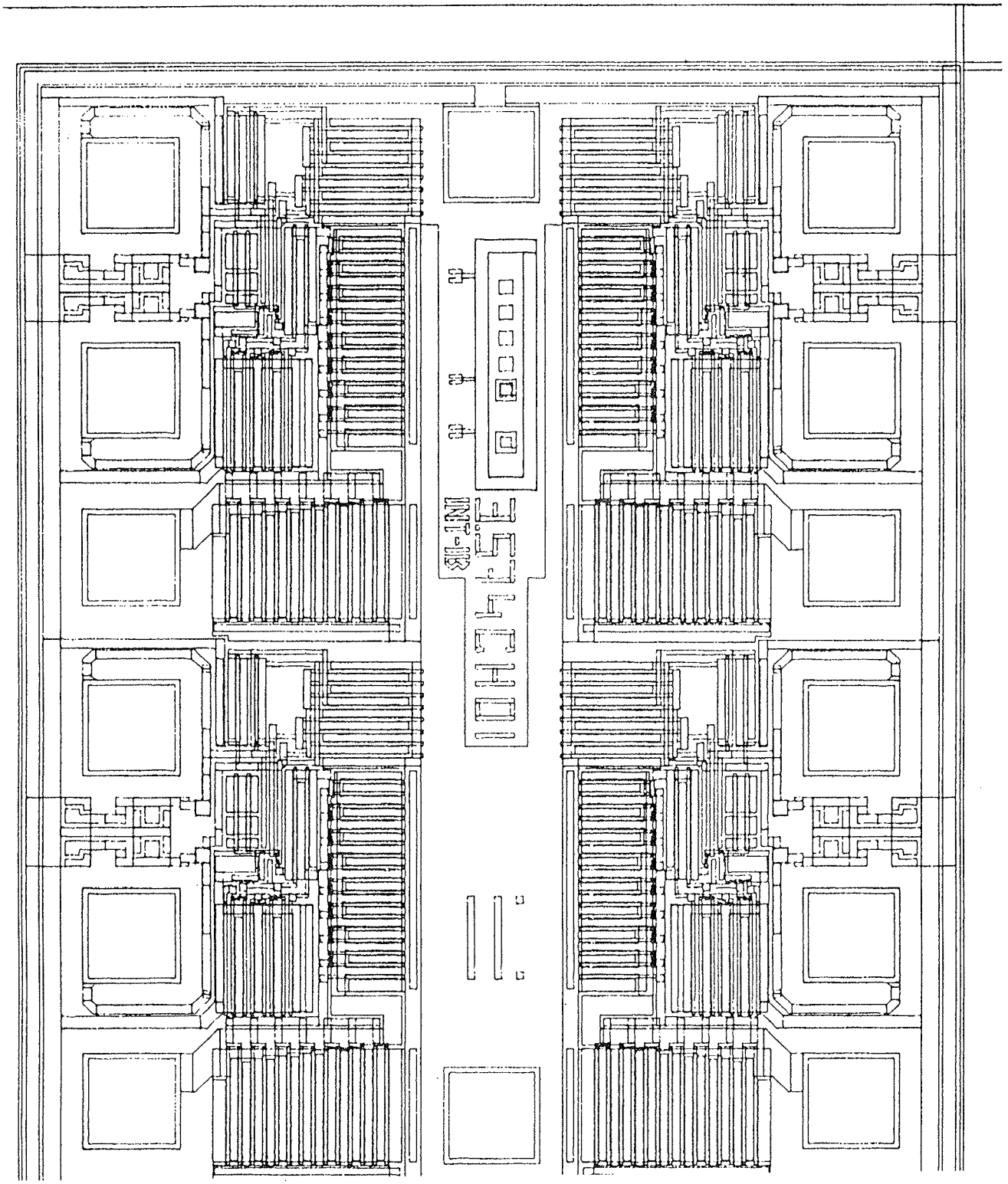

Figure 5: Plot of the finished chip

2) The circuit now has input current almost like a TTL gate. The only difference is the current does not cut off at Vin = 1.6V, but decreases linearly as Vin rises to 4V.

3) The diode has the further advantage of level shifting the switching point to about 2.5V at the inverter input. This allows a normal ratio of p to n transistor size of 2.5:1 instead of the previously calculated input ratio of 1:4.8, resulting in a smaller layout for this inverter.

This circuit was simulated and proved to have delay times very similar to the more conventional MOS inputs.

In the event it was decided not to proceed with this approach. It was a bit of a hybrid, not exactly TTL, not exactly CMOS either. Also it would fail a TTL input high leakage test and it was considered very important that the existing incoming inspection test program could be used for the CMOS replacement without any modifications.

Fig. 5 shows a plot of the finished chip, 1.1 mm x 1.4 mm. It has been successfully fabricated at ISKRA MIKROELEKTRONIKA and accepted by the customer. Both speed and current sinking capabilities are virtually identical to the 74H01 with the added bonus of a far lower d.c. power consumption.

Conclusions

Modern HCMOS technology is an ideal way to avoid shortages in all TTL families up to and including Low Power Schottky. Gate delays are very similar and CMOS outputs have no trouble sinking 20 mA worst case up to 70 deg. C. In all cases a very substantial power saving will result from the zero standby current of CMOS.

Although not shown by this particular design example even greater savings in power and board space can result if an entire board or logic system is replaced, either by a gate array or a dedicated standard cell ASIC.

References:

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