AN APPROACH TO THE MANUFACTURING YIELD IN DIGITAL FILTER CIRCUITS

E. M. Saad, A. Rabie, N. Hanna

KEY WORDS: digital signal processing, digital filters, digital circuit, circuit design, design method, centering technique.

SUMMARY: The object of this paper is to use a design centering technique to improve the realization accuracy of digital filters. That should maximize the number of digital filter circuits which meet specifications. For a certain f_s and in a certain frequency band, the coefficients a's and b's represent n-vector of statical varying parameters. The constraints are the amplitude response /h(jw)/ over a prescribed range of frequency. Then, under and/or within certain specification, we get the acceptable region, otherwise failed region. After determinig the acceptable region, the design center is defined as the point at which the parameters can have maximum variation and still, the response satisfies the specifications. Consequently, a new set of nominal values for the coefficients is obtained. Using these new values, the number of digital filter circuits that meet specifications is maximized.

PRISTOP K IZBOLJŠANJU IZPLENA VERZIJ, KI VSEBUJEJO DIGITALNE FILTRE

KLJUČNE BESEDE: digitalno procesiranje signalov, digitalni filtri, digitalna vezja, načrtovanje vezij, načrtovalske metode, tehnika centriranja

POVZETEK: Namen prispevka je prikazati uporabo tehnike centriranja za izboljšanje točnosti pri realizaciji digitalnih filtrov. Rezultat teh prizadevanj mora biti povečano število vezij z digitalnimi filtri, ki ustrezajo specifikacijam. Za določeno vrednost f_s in določen frekvenčni pas. Koeficienti a in b predstavljajo n dimenzionalni vektor statistično spremenljivih parametrov. Edina omejitev je potek amplitude/hjw)/ v določenem frekvenčnem pasu. Nato ob upoštevanju določenih pogojev, dobimo območje sprejema oz/ali zavrnitve. Po določitvi območja sprejema tako določimo center načrtovanja, da ko se parametri maksimalno spreminjajo, je odziv še vedno znotraj specifikacij. Nato izberemo nov set nominalnih vrednosti koeficientov, s katerimi število vezij z digitalnimi filtri, ki maksimalno ustrezajo specifikacijam.

INTRODUCTION

It is appropriate to the economy of circuit manufacture to maximize circuit yield and to produce circuit which satisfy the specification at minimum unit cost. Design centering technique increases manufacturing yield by finding new set of nominal values for the circuit parameters[1].
The transfer function H(Z) of an IIR digital filter can be written as [2-3],

$$H(Z)= \frac{\sum_{n=0}^{M} a_n Z^{-n}}{(1+\sum_{n=1}^{N} b_n Z^{-n})} \quad \ldots (1)$$

$M \leq N$

where $Z = e^{jwT}$ and T is the sampling time.

This transfer function H (Z) is a function of the coefficients a's, b's, the sampling frequency $f_s = 1/T$, and the frequency f.
For a certain f_s and a certain frequency band, the coefficients a's and b's represent n-vector of statistical varying parameters. The constraints are the amplitude response /H(jw)/ over a prescribed range of frequency.

METHOD

The object is to find another values for the coefficients a's and b's of H(Z) in (1), such that maximum yield in these coefficients can occur and the transfer function amplitude /H(Z)/ of the filter remains specifying the requirement. These new set of the nominal values of the coefficients determine the transfer function which achieve increasing of the manufacturing yield.

Considering H(Z) is realized in cascaded form as follows,

$$H(Z)= \Pi_i H_i(Z) \quad \ldots (2)$$

where $H_i(Z)$ is either a second order and/or first order section and equal to:

$$H_i(Z)= \frac{(a_{0i} + a_{1i} z^{-1} + a_{2i} z^{-2})}{(1 + b_{1i} z^{-1} + b_{2i} z^{-2})}$$

$a_{0i} = a_{2i}$ or

$$H_i(Z)= \frac{(a_{0i} + a_{1i} z^{-1})}{(1 + b_{1i} z^{-1})}$$

$a_{0i} = a_{1i}$

The coefficients a_{0i} and a_{1i} are varied, leaving the others fixed, till the response (amplitude response) of the overall filter gets out the tolerance scheme at any frequency point. Accordingly, an acceptable region (countour) is obtained, as ex., Fig.1. The center of that region gives a_{0i} and a_{1i} values which specify maximum yield. That center is obtained graphically or using numerical scane[4].

Now, givivg a_{0i} and a_{1i} the new values, and repeating the process for the coefficients b_{1i} and b_{2i}, the centered values for these two coefficients are obtained. Naturally, the variation the coefficients should be in the positive and negative direction with respact to starting values. Then that section, i, is finished.

The process is repeated for the other filter-sections, till we get the transfer function H(Z) with new set of coefficients. This transfer function H(Z) with the new set of coefficient values can be given to the manufacturers, to specify increasing manufacture yield, and accordingly increases number of circuits that meet the specifications.

ILLUSTRATIVE EXAMPLE

The method is applied to an infinite impulse response (IIR) PCM low pass digital filter from the fifth order which obeys the CCITT requirements. The transfer function H(Z) is written as:

$$H(Z)=\frac{(a_1+a_1z^{-1})}{(1+b_1z^{-1})}\cdot\frac{(c_1+c_2z^{-1}+c_1z^{-2})}{(1+d_1z^{-1}+d_2z^{-2})}\cdot\frac{(e_1+e_2z^{-1}+e_1z^{-2})}{(1+g_1z^{-1}+g_2z^{-2})} \quad ...(3)$$

The ceofficients are as follows:-

original set	centered set
a_1= 0.1910345325	a_1= 0.1891248038
b_1= -0.617930935	b_1= -0.617930935
c_1= 0.2011466295	c_1= 0.20154892276
c_2= -0.120242261	c_2= -0.12360904431
d_1= -1.305885856	d_1= -1.3084167
d_2= 0.587936854	d_2= 0.5875
e_1= 0.56870605	e_1= 0.56106
e_2= -0.683605882	e_2= -0.6683333
g_1= -1.426924416	g_1= -1.4268
g_2= 0.8807306387	g_2= 0.878

and f_s=32 kHz.

Searching for the design center of each two coefficients, leaving the other fixed, then giving the design centering values for two coefficients and searching for next two, and so forth for the filter sections successively as mentioned in the method, a new set of nominal values for the coefficients is obtained [4]. The new coefficient values are written in the right side of the original coefficients.

Figure 1 shows the acceptable region for the coefficients d_1, d_2 and for the e_1 and e_2, as exemple.

Due to rounding errors, the response falls within the tolerance scheme even at 6 bit coefficient lenght, figure 2. The response of the same filter without design centering gets out the scheme, at 6 bit length.
Consequently, using design centering technique, circuit yield increases. Accordingly, the number of digital filter circuits that meet specification can be maximized.

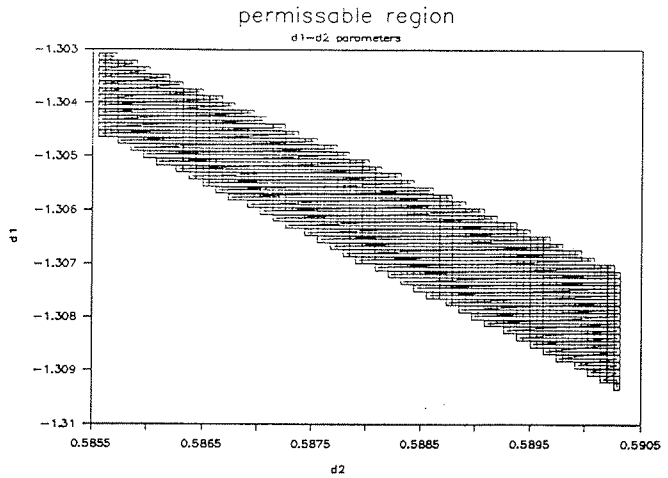

Fig. 1. Acceptable region for the coefficients 1a) d_1, d_2 and 1b) e_1, e_2

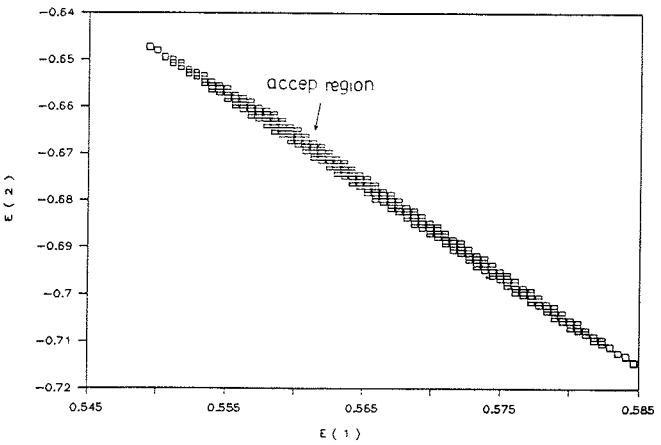

Fig. 1.b

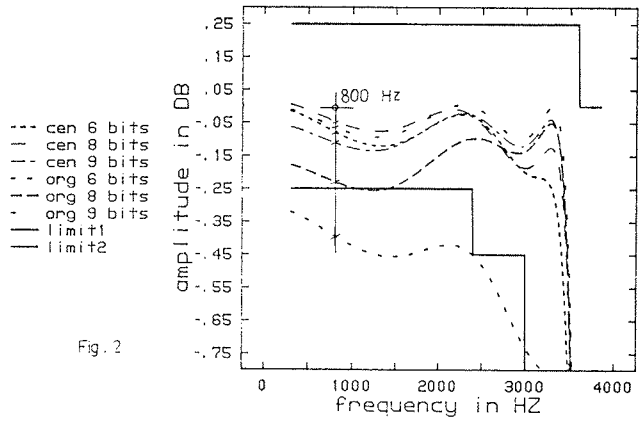

Fig. 2

Fig. 2 Amplitude Response Rounded Parameters

REFERENCES

1. S. W. Director, et al. "The simplicical approximation approach to design centering" IEEE Trans. on circuits and systems, Vol. 7, july, 1977, PP.363-372.

2. L. R. Rabiner & B. Gold "Theory and application of digital signal processing" Prentice=Hall, 1975.

3. E. M. Sadd, et al. "Analysis of errors and possible cancellation of their effects in digital filters" Modeling, Simulation & Control, A. AMSE Press, Vol. 16, No.=4.1988, PP. 1-6.

4. A. Rabie "Hardware realization of microprocessor-based digital filters "M. Sc. Thesis, Univ. of Helwan, expected end 1989.

El Sayed M. Saad,
Assoc. Prof., Faculty of Engineering and Technology, Univ. of Helwan, Egypt.
Nabil N. Hanna, Prof.,
Faculty of Engineering and Technology, Univ. of Helwan, Egypt.
Ahmed Rabie,
Engineer, National Institute of Astronomy and Geophysics, Helwan, Egypt.

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