G A L s - GENERIC ARRAY LOGIC (Part I) (A member of PLDs family)

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KEY WORDS: Programmable logic circuits, integrated circuits, Aplication specific integrated circuits, ASIC, EECMOS, VLSI, Output Logic Macro Cells, GAL, SGS-THOMSON

ABSTRACT: An overview on GALs, a PLDs from SGS-THOMSON, is presented. Over traditional PALs fabricated in bipolar technology, GALs exibit several important advantages which are coming from high performance EECMOS process and distinctive architectural features.

GALi - Generične logične mreže (I. del)

KLJUČNE BESEDE: programabilna logična vezja, integrirana vezja, vezja po naročilu, ASIC, EECMOS, VLSI, izhodne logične makrocelice, GAL, SGS-THOMSON

POVZETEK: Podane so osnove GAL, programabilnih logičnih vezij firme SGS-THOMSON. V primerjavi s tradicionalnimi PAL vezji, izdelanimi v bipolarni tehnologiji, imajo GAL vezja vrsto prednosti, ki izhajajo pretežno iz visokokakovostnega procesa EECMOS in same arhitekture vezja.

1. INTRODUCTION: PLDs - A DYNAMIC MARKET

Digital logic functions can be designed from a wide range of components.These include discrete components such as transistors, diodes and SSI,MSS up to VLSI integrated circuits.Choosing a component is an engineering decision that depends on factors such as cost, physical size, availability, level of integration,power consumption,propagation delay and heat dissipation. Programmable logic devices (PLDs) are another option when making this decision.

Programmable logic devices are an ordered collection of elementary logic circuits which can be electrically programmed by the user to accomplish a specific logic function.Their versality makes them exstremelly attractive to a vast range of electronic equipment manufacturers.

The whole PLD market is expected to escalate from 500 million dollars in 1988 to about 1.3 billion dollars in 1992;this corresponds to an average increase greater than 30% a year over a five year period,much more than average semiconductor market increase.

At the present moment PLDs made in bipolar technology occupy the largest share of the market.However,a rapid increase in the use MOS PLDs is expected.This relatively new technology accounted for 20% of the total PLD market in 1988,and by the early 1990s is predicted to surpass its bipolar counterpart.

Altough PLDs have been around since the early 1970s,they are only now starting to take off in a big way.The increase in interest in these devices is due to two main reasons:

* the computer market,which accounts for the largest absorption of PLDs,is growing dramatically and will continue to count for more than 60% of the whole PLD market.
* PLDs for semiconductor manufacturers are standard devices;for customers however,they are ASICs due to their programmability.

Over other semicustom devices PLDs exibit some very important advantages:

* low design-in cost
* no prototype cost
* no mask remaking costs
* no supplier computer time cost
* no NRE (Non Recurring Expenses)
* capital investment is necessary only once.The programming and development equipment costs are very low.
* no dedicated inventory.One single PLD can cover many different applications.
* the complete design cycle is in the hands of the customer.This means the design-to-production cycle time can be days,not weeks or months as in the case of gate arrays.

PLDs manufactured using bipolar technology use the fuse link concept developed at the beginning of 1970s for the bipolar PROMs.One of the most succesfull devices using this bipolar technology are the PALs,and the company which today has the leadership in the PLD market is MMI/AMD with its bipolar PALs.

MOS PLDs on the other hand use technologies and circuits solutions originally developed for EPROM and EEPROM memories,and they are likely to repeat the history of their parents,MOS memories,by achieving a market share higher than their bipolar counterparts.

2. G A L s - GENERIC LOGIC ARRAYS

GALs are trademark of American semiconductor company LATTICE SEMICONDUCTOR CORP. from Oregon.In Europe SGS-THOMSON has second source contract for GALs with which he entered the CMOS PLDs market less than three years ago.On following pages a general overview and main features of SGS-THOMSON's GALs are presented.

Technology employed on all GAL devices is a state of the art high performance EECMOS process which has the best speed-power characteristics available from any user-programmable technology.

GALs are clearly teh next evolutionary step in programmable logic. In general they also use basic PAL architecture (programmable "AND" array driving fixed "OR" array as it is shown on Figure 1) but on the other hand offer numerous advantages.

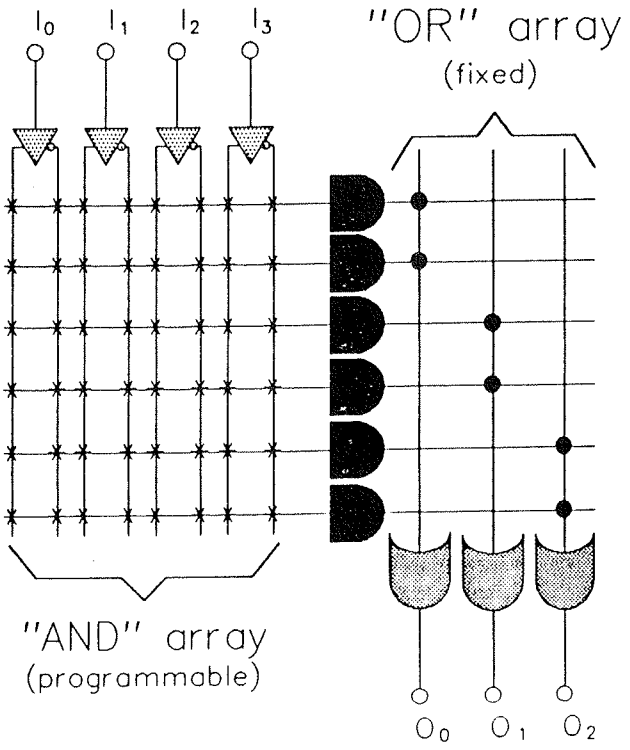


Figure 1: Basic GAL architecture

Main features of GALs are:

a) Electrical erasability

Electrical erasability and consequent reprogrammability offers a quick response to unforcasted design modifications.This becomes exstremely important during the prototyping phase when errors or design specifications changes are more likely to occur.

b) High speeds

* 12 ns propagation delay
* 12 ns max. clock-in data out
* Programming algorithem less than one second,50ms erasing time

c) Power consumption as low as 50% of comparable-speed bipolar devices

d) Output logic Macrocell (OLMC) technology

It allows the user to configure outputs to different also non standard architectures.So each output can be individually set to active high or active low with either combinational(asynchronous) or registered (synchronous) configurations.Common output enable can be connected to all outputs or separate inputs or product terms can be used to provide individual output enable control. In general OLMC technology provides the designer with maximal output flexibility in matching signal requirements.

e) PAL socket compatibility with full function/fuse map/parametric compatibility

One GAL type can emulate many PAL types.For example basic GAL type GAL16V8 can substitute 21 different types of 20-pin bipolar PALs.

f) 100% Functional testability

This testability is offered by the EEPROM technology that allows full AC/DC testing of teh logic path inside the PLD by writing the worst case pattern.This means 100% quaranted yield to the customer.After the test cycle,the device is erased and shipped.More than 100 write and erase cycles are possible.

g) Electronic signature

It allows to store documentation in every GAL as it is indetification number for device tracebility and version number and production date to trace the manufacturing flow.

h) High functional CMOS density

Basic GAL versions offer up to 300 equivalent gates of complexsity while new one based on FPLA (field programmable logic arrays) has the capacity of 600 equivalent gates.

i) Design/programming tools

GALs are supported from a variety of the industry's most popular design and programming tools.

j) Security cell

On all GALs the security cell is provided as a detereent to unauthorized copying of the array configuration patterns.Once programmed, the circuitry enabling array accsess is disabled,preventing further programming or verification of the array. The cell can be erased only in conjuction with the array during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed.

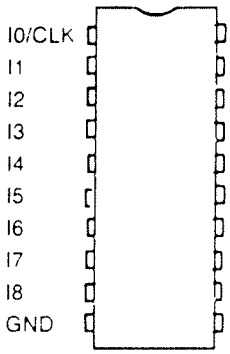
3) BASIC GAL DEVICES - GAL16V8 AND GAL20V8

The two main devices,GAL16V8 and GAL20V8 are the core of SGS- THOMSON's GAL productsportfolio.

PIN NAMES

I0-I15	INPUT
CK	CLOCK INPUT
B0-B15	BIDIRECTIONAL
F0-F7	OUTPUT
$\overline{OE}$	OUTPUT ENABLE
V_{CC}	POWER (+5V)
GND	GROUND

GAL16V8 EMULATING PAL DEVICES



V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
F7	I11	I13	I15	F7	B1	B3	F1
F6	F5	I12	I14	F6	F5	B2	B5
F5	F4	F3	I13	F5	F4	F3	B4
F4	F3	F2	F1	F4	F3	F2	B3
F3	F2	F1	F0	F3	F2	F1	B2
F2	F1	F0	I12	F2	F1	F0	B1
F1	F0	I11	I11	F1	F0	B1	B0
F0	I10	I10	I10	F0	B0	B0	F0
I9	I9	I9	I9	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	I9
10L8	12L6	14L4	16L2	16R8	16R6	16R4	16L8
10H8	12H6	14H4	16H2	16RP8	16RP6	16RP4	16H8
10P8	12P6	14P4	16P2				16P8
GAL16V8							

BLOCK DIAGRAM

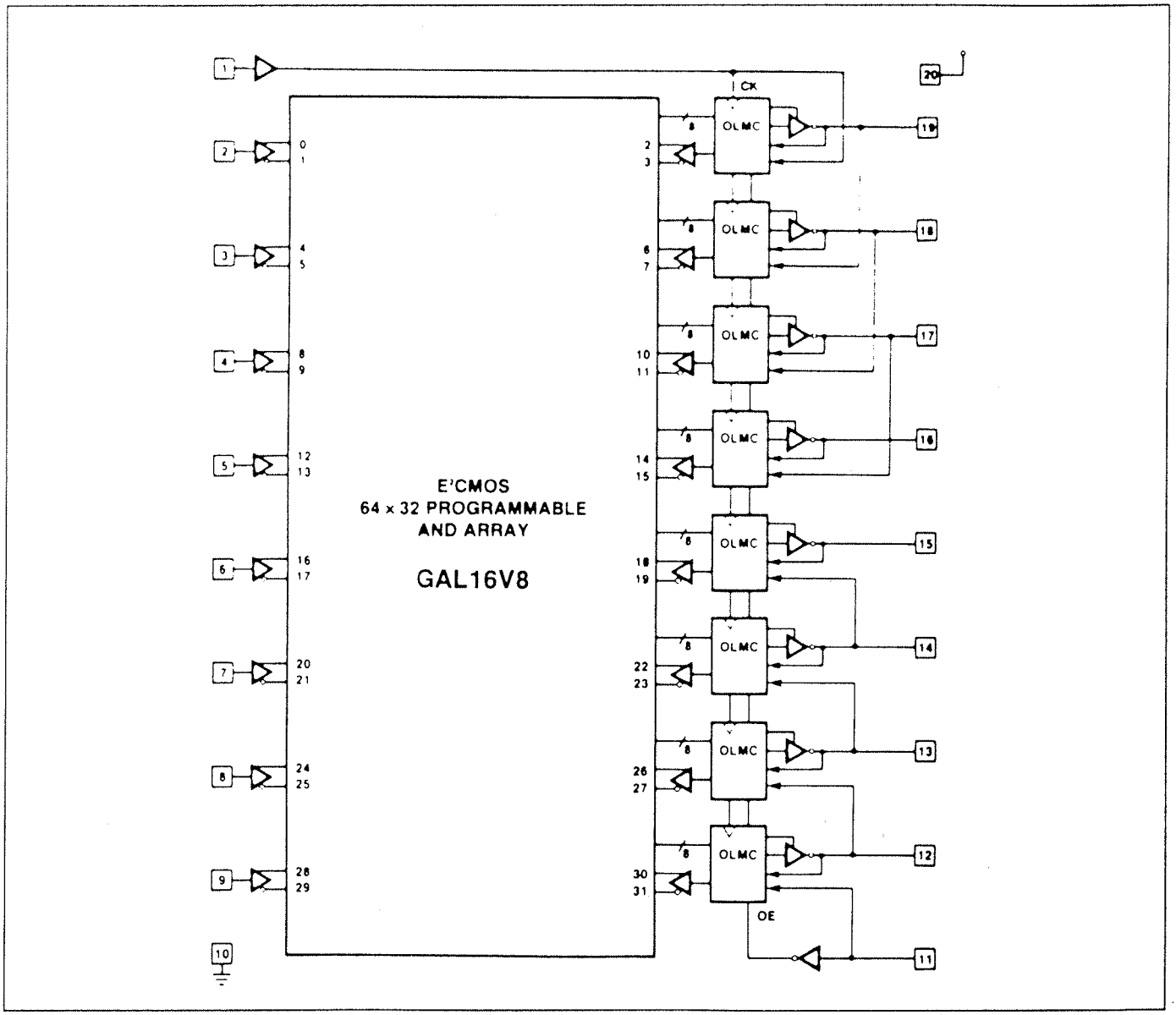


Figure 2: Block diagram of GAL 16V8 with PAL amulating scheme

a) GAL16V8 Features

* 16 input pins
* 8 output pins (OLMCs)
* 64x32 programmable "AND" array
* Low power:
  90/70 mA active/stand-by (Half-Power version)
  45/35 mA active/stand-by (Quarter Power)
* High speed:
  15 to 35 ns access time (Half Power version)
  20 to 35 ns access time (Quarter Power)
* Preload and power-on reset of all registers
* Emulates 20 pins PAL devices with full Function/Fuse map/Parametric Compatibility
* High speed programming algorithm
* Data retention exceeds 20 years
* Block diagram of GAL16V8 with PAL emulating scheme is presented on Figure 2, when Figure 3 shows its logic diagram.

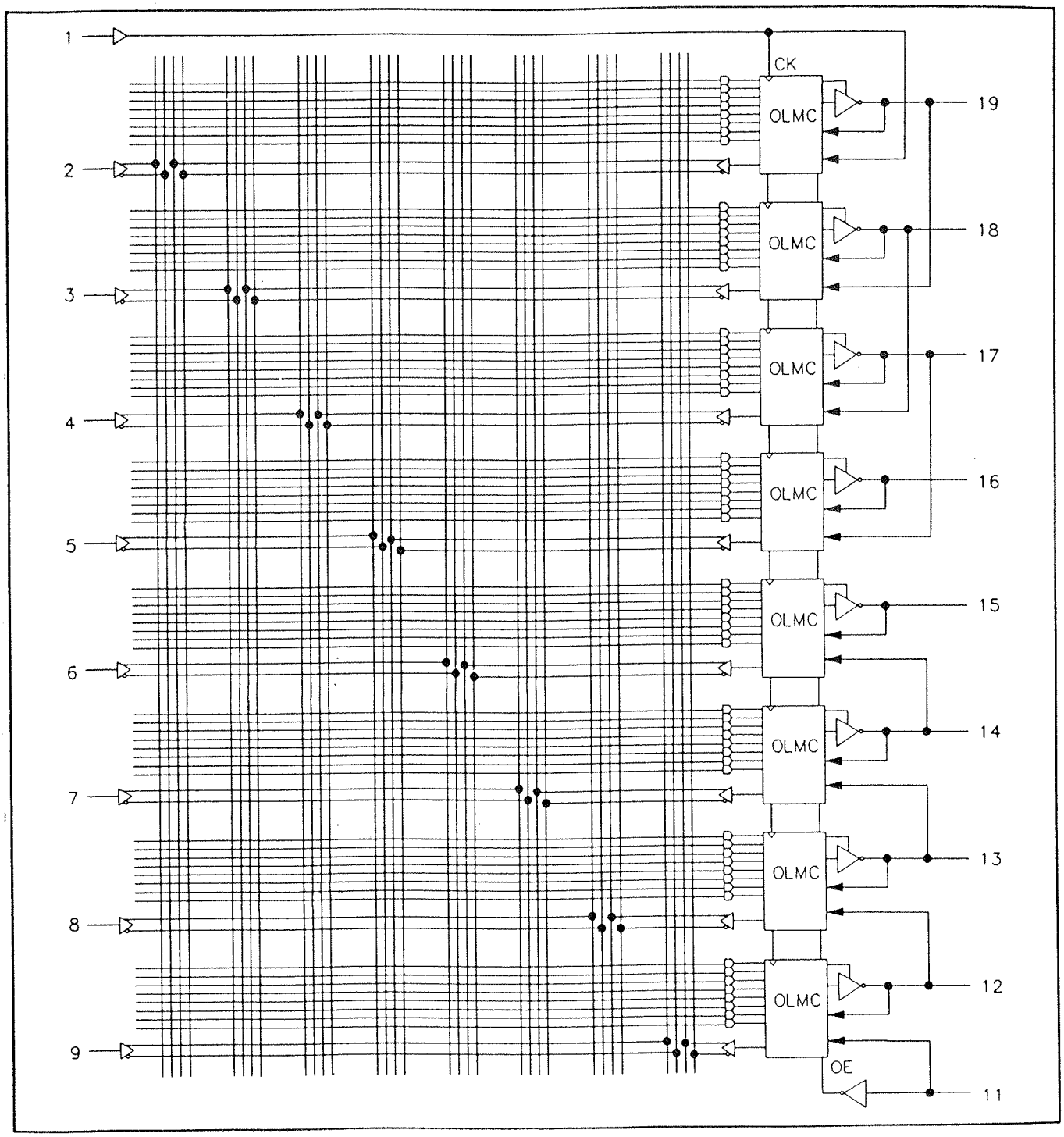


Figure 3: GAL 16V8 Logic diagram

b) GAL20V8 features

* 20 input pins
* 8 output pins (OLMCs)
* 64 x 40 programmable "AND" array
* other characteristics are the same as with GAL16V8

Both GAL types are available in different speed/power versions and variety of packages as is shown on Figure 4.

ORDER CODE	PACKAGE	SPEED AND MAX POWER
GAL16V8-25HB1	20 pin plastic DIP	25ns/90mA
GAL16V8-20HB1		20ns/90mA
GAL16V8-15HB1		15ns/90mA
GAL16V8-25HC1	20 pin PLCC	25ns/90mA
GAL16V8-20HC1		20ns/90mA
GAL16V8-15HC1		15ns/90mA
GAL20V8-25HB1	24 pin plastic DIP	25ns/90mA
GAL20V8-20HB1		20ns/90mA
GAL20V8-15HB1		15ns/90mA
GAL20V8-25HC1	28 pin PLCC	25ns/90mA
GAL20V8-20HC1		20ns/90mA
GAL20V8-15HC1		15ns/90mA
GAL16V8-35QB1	20 pin plastic DIP	35ns/45mA
GAL16V8-25QB1		25ns/45mA
GAL20V8-35QB1	24 pin plastic DIP	35ns/45mA
GAL20V8-25QB1		25ns/45mA

Figure 4: GAL types availability

4. PROGRAMMING GALs

Generating a completely functional circuit element from an unprogrammed GAL device requires three phases:

a) Design - defining the logic functions that the circuit must perform.

b) Programming - writing those logic functions into a blank device.

c) Testing - ensuring that each programmed device functions exactly as the design specifies.

Design phase consists of defining the neccesarry logic functions,expressing them in a natural and convenient form and creating,by means of special development software,so called input source file.This file is then converted to a binary fuse file or "JEDEC" file,which has standardized format for PLDs data transfer.

Quite a broad range of design software packages are very common and easily available from different vendors and approved by SGS- THOMSON.Main of them are listed on Figure 5.

SOFTWARE DEVELOPMENT TOOLS

PACKAGE	VENDOR	REVISION
CUPL	Logical Devices	V3.0
ABEL	Data I/O	V3.0
PLD test	Data I/O	V1.0
DASH - ABEL	Data I/O	V1.0
PALASM	Monolithic Memories Inc.	(I)
LC9000	Programmable Logic Tec.	V1.5
PLAQ	Qwerty Inc.	V1.0

Figure 5: Software development tools

During programming phase a JEDEC file is written into the device by means of programmer.Programmer reads JEDEC file and transfers it by applying the specific series of voltage pulses to the device.Programmers are usually driven by IBM PC compatible computer.SGS-THOMSON recommends to use only approved programming hardware listed on Figure 6.

GAL QUALIFIED PROGRAMMER LIST

VENDOR	PROGRAMMER	ADAPTER	REV. QUALIFIED	COMMENTS
QWERTY	GPR - 1000	n/a	v2.0	
-	GPR - 1000+	n/a	v1.0 , v1.1	
DATA I/O	29B (v04)	303A - 011A	v03	
-	-	-	v06	
-	-	-	v07 , v0.8 , v 0.9	
-	60A	360A - 011A	v11 , v12 , v13	v13 preferred
-	-	360A - 006	v12 , v13	
-	60H	n/a	v13	
-	Unisite - 40	n/a	v1.7	
-	-	n/a	v2.20 , v2.50	
Logical Devices	ALLPRO	n/a	v1.46c , v1.47c	
-	PALPRO - 2X	n/a	v4.2 , V4.3	
Inlab	Model 28	n/a	5.38	
Stag	ZL30A	n/a	30A21 , 30A28 , 30-32	
One - D	Sailor - PAL	n/a	v8.60	
Advin Systems	Sailor - PAL	n/a	v8.60	
BP Microsystems	PLD - 1100	n/a	v1.11	
Promac	P3	n/a	3.20	
System General	SGUP-85	UPPAL-15	v24 , v25	
-	-	UPPAL-17	v2.20	
SMS	Sprint PLUS	n/a	v3.2h	
PLT	Logic Lab	n/a	v2.10	

Figure 6: GAL qualified programmer list

Testing the programmed device under simulated operational conditions is an absolute necessity to avoid later high repair costs on the field.

There are three different tests which can be performed on the programmed device.These are fuse verification,vector testing and pseudorandom testing.The fuse verification is usually performed automaticaly and simply checks each and every fuse to ensure correct programming was accomplished.In general it is not sufficient to quarantee that device will operate properly.

Better aproach is vector testing which use design verification vectors generated by the engineer combined with vectors generated automatically by development software.

Pseudorandom testing is usually a programmer-dependent feature and has been built into some programming equipment.

GALs are certainly gaining higher and higher popularity inside the PLDs market which certainly shows one of the fastest grow on whole semiconductor market. In next part more detailed explanation on technical characteristic and programming aproaches of SGS-THOMSON's GALs will be presented.

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