G A L s - GENERIC ARRAY LOGIC (Part II) (A member of PLDs family)

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KEY WORDS: Programmable logic devices (PLDs), Aplication specific integrated circuits (ASIC), EECMOS, Output Logic Macro Cell (OLMC),

ABSTRACT: In Part I of this article an overview on GALs has been presented. This part (Part II) deals with architecture of GAL devices in more details.

GALi - Generične logične mreže (II. del)

KLJUČNE BESEDE: programabilna logična vezja (PLDs), integrirana vezja po naročilu (ASIC), EECMOS, izhodne logične makrocelice.

POVZETEK: V prvem delu članka je bil podan splošen opis GAL programabilnih logičnih vezij. Ta del (II. del) pa detaljneje podaja arhitekturo GAL vezij.

1. INTRODUCTION: PLDs BASIC CONCEPTS

The digital logic design process is based on Boolean algebra. Once we define the function we want to implement it is very important to optimize it to either two formats that are easily transferred into PLD logic map using well known Boolean algebra postulates and theorems. These two formats are the Sum Of Products (SOP) and the Product Of Sum (POS). The POS format can be used to describe any combinatorial logic function. This two level format consists of logical OR terms that are ANDed together. Thus logic function

(1) Y=A* (C+D) +B*C+B*D

can be simplified to:

(2) Y=A* (C+D) +B* (C+D)

and then

(3) Y= (A+B) * (C+D)

which is an AND of sum terms.

The most common represenation used in PLDs implementations is the dual of the Product Of Sums format and is known as the Sum Of Products. The SOP consists of several AND terms ORed (summed) together. So Eq. (1) can also be written to a SOP form:

(4) Y=A*C+A*D+B*C+B*D

The above transformations are shown in Figure 1.

There are some logic conventions used to describe PLD devices. A typical PLD input buffer is showed in Figure 2. Its two outputs are the true and complement of the input.

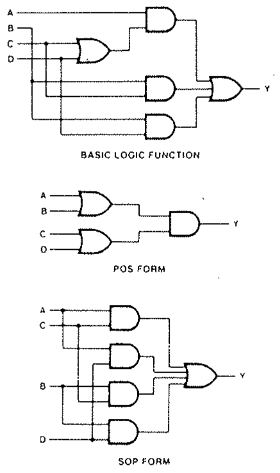
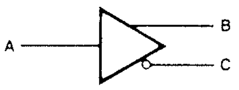


Figure 1: Basic Function Formate



A	B	C
0	0	1
1	1	0

Figure 2: PLD Input Buffer

Figure 3 illustrates the convention used to reduce the complexity of a logic diagram without sacrificing any of the clarity. Inputs of the PLD representation of the three input AND gate are so called **input terms** while multiple-input AND gate itself is known as a **Product term.**

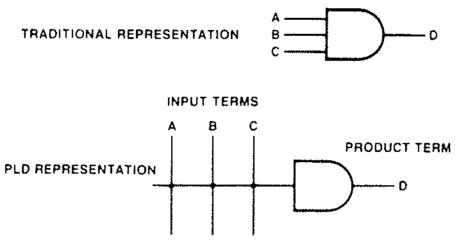


Figure 3: AND Gate Representations

Convention regarding PLDs connections shown on PLDs logic diagrams is described on Figure 4. As we can see the solid dot represents a permanent connection while X over the intersection implies that the connection is programmed (intact), whereas the absence of an X implies no connection.

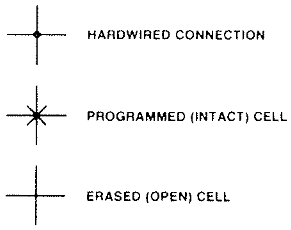


Figure 4: PLD Connections

2. ARCHITECTURE OF GAL DEVICES

The architecture of GAL devices is in basis a traditional PAL structure comprised of a programmable AND array driving a fixed OR array as it is shown on Figure 5. The difference is in the architecture and flexibility of the output functions.

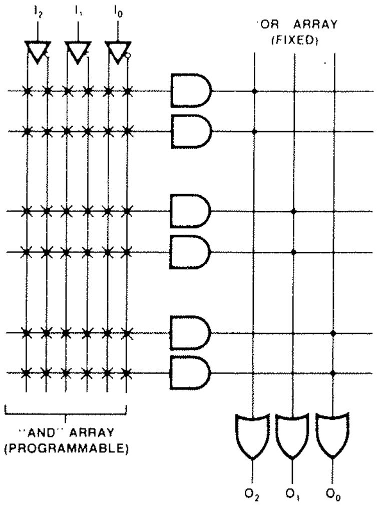


Figure 5: Basic PAL Device Architecture

2. 1. Output Logic Macrocells (OLMCs)

GAL devices integrates so called Output Logic Macrocells (OLMC) on each of its output pins which provides the designer with maximal output flexibility in matching signal requirements. Each output can be individually set to active high or active low, with either combinational (asynchronous) or registered (synchronous) configurations.

The basic GAL device GAL16V8 and its eight OLMCs are shown on Figure 6. As it can be seen a programmable AND array is comprised of eight groups by eight (in total 64) product terms each with 32 input terms. Each group of eight product terms is ORed in one OLMC. Block diagram of OLMC itself is shown on Figure 7. Within the OLMC are four multiplexers which are used to configure the outputs. These are FMUX, OMUX, PTMUX and TSMUX which are controlled trough programming certain cells (SYN, AC0, AC1 (n), XOR (n)) within the 82-bit Architecture Control Word. The GAL16V8 Architecture Control Word Diagram is shown in Figure 8.

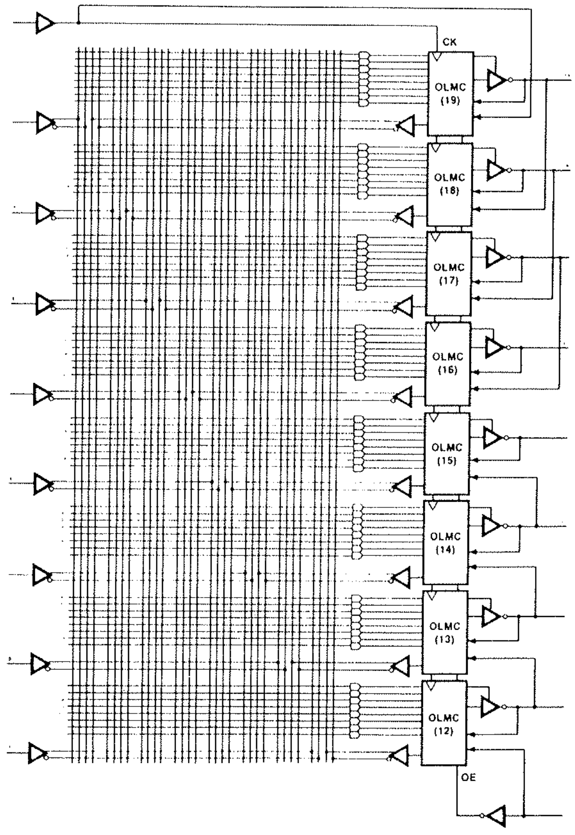


Figure 6: GAL 16V6 Block Diagram

The SYN bit determines whether or not a device will have registered output capability or will have purely combinational outputs. It also replaces the AC0 bit in the two outermost macrocells, OLMC (12) and OLMC (19). When first setting up the device architecture, this is the first bit to choose.

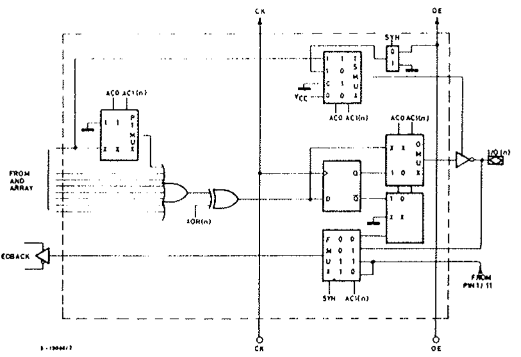


Figure 7a: GAL 16V6 Output Logic Macrocell: Pin 12 and 19

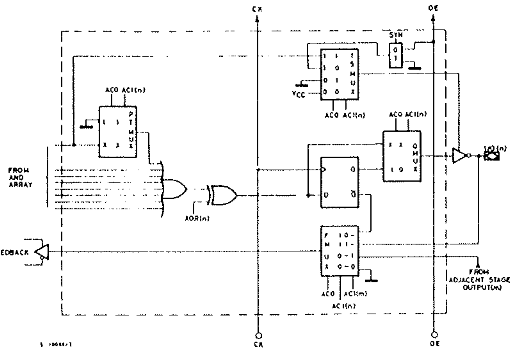


Figure 7b: GAL 16V6 Output Logic Macrocell: Pin 13 to 18

Architecture Control bit AC0 and the eight AC1 (n) bits direct the outputs to be wired always on, always off (as an input), have a common OE term (pin 11), or be three-state controlled separately from a product term. The Architecture Control bits also determine the source of the array feedback term trough the FMUX, and select either combinational or registered outputs.

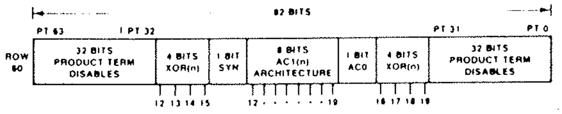


Figure 8: GAL 16V8 Architecture Control Word Diagram

The programmable polarity feature deserves special attention. Located in the heart of OLMC, the programmable polarity function is implemented by the Exclusiv-OR (XOR) gate that follows the OR gate from the array. Programmable polarity is used extensively in DeMorgan's Law to reduce the number of product terms required to implement a function.

The OLMCs are configurable by the designer to perform the various functions. For example, the designer merely specifies two active-low registers, one active-high register and the device is configured instantly.

Since each of the OLMCs contains the same logic, it is also possible to "tweak" an existing design for the convenience of the manufacturing department. One example might be moving a function to an adjacent pin to optimize board layout.

It should be noted that all the actual architectural implementation is accomplished by development software / hardware and is completely transparent to the user.

2. 2. Row Address Map Description

Figure 9 shows a block diagram of the row address map. There are a total 32 unique row addresses available to the user when programming the GAL16V8 device. Row addresses 0-31 each contain 64 bits of input term data. This is the user array where the custom logic pattern is programmed. Row 32 is the Electronic Signature Word. It has 64 bits of reprogrammable memory that can contain user-defined data. Some use include user ID, revision numbers, or inventory control. This signature data is always available to the user independent of the state of the security Cell.

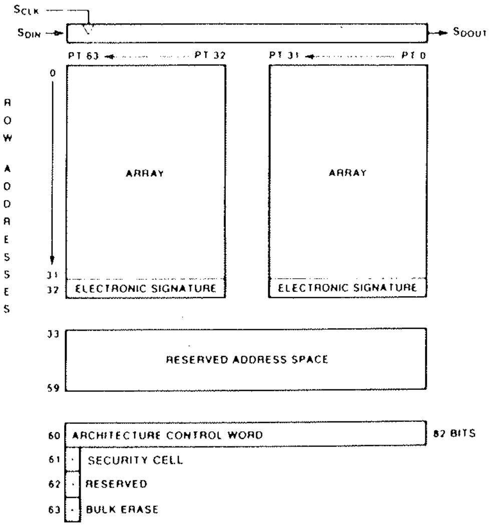


Figure 9: GAL 16V8 Row Address Map Block Diagram

Row 33-59 are reserved by the manufacturer and are not available to the user.

Row 60 is previous mentioned 82-bit Architecture Control Word.

Row adress 61 contains one-bit Security cell which is provided on all GAL16V8 devices as a deterrent to unathorized copying of the array configuration patterns. Once programmed, the circutry enabling array access is disabled, preventing further programming or verification of the array (rows 0-31). The cell can be erased only in conjuction with the array during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. On the other hand signature data is always available to the user.

By addressing row 63 during programming cycle, a clear function performs a bulk erase of the array and the Architecture Control Word. In addition, the Electronic Signature Word and the Security cell are erased. This mode resets a previously configured device back to its virgin state.

2. 3. Output Register Preload

When testing state machine designs, all possible states and state transition must be verified in the design, not just those required in the normal machine operations. This is because in system operation, certain events occur that may throw the logic into illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these condition, a way must be provided to break the feedback paths and force any desired (i. e. illegal) state into a register. Then the machine can be sequenced and the outputs tested for the correct next state condition.

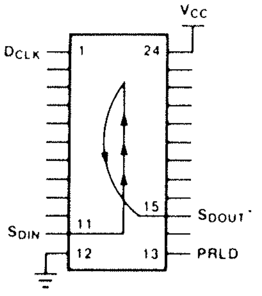


Figure 10: Output Register Preload Pinout

The GAL16V8 device includes circutry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. Figure 10 shows the pin functions necessary to preload the register. The register preload timing and pin voltage levels necessary to perform the function are shown on Figure 11. This test mode is entered by raising PRLD to VIES, which enables the serial data in (SDIN) buffer and serial data (SDOUT) buffer. Data is then serially shifted into the registers on each rising edge of the clock, DLCK. Only the macrocells with registered output configurations are loaded. If only three outputs have registers, then only three bits need be shifted in. The registers are loaded from the bottom up as shown on Figure 10.

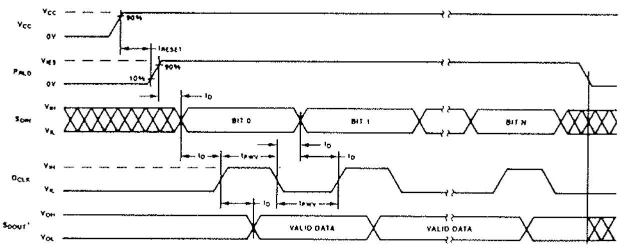


Figure 11: Register Preload Waveforms

2. 4. Latch-up Protection

GAL devices are designed with on board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circutry to latch. Additionally, outputs are designed with n-chanell pullups instead of traditional p-channel pull-ups to eliminate any possibility SCR induced latching.
Circutry within the GAL16V8 provides a reset signal to

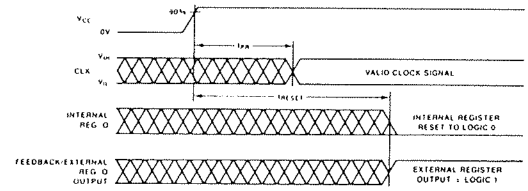

VCC
0V
90%
tPR
VIH
CLK
VIL
VALID CLOCK SIGNAL
tRESET
INTERNAL REG O
INTERNAL REGISTER RESET TO LOGIC 0
FEEDBACK/EXTERNAL REG O OUTPUT
EXTERNAL REGISTER OUTPUT = LOGIC 1

Figure 12: Power-up Reset

all registers during power-up (see Figure 12). All internal registers will have their Q outputs set low after a specified time (t RESET). As a result, the state on the registerd output pin (if they are enabled trough OE) will always be high on power-up, regardless of the programmed polarity of the uotput pins. These features can greatly simplify state machine design by providing a known state on power-up.

The timing diagram for power-up is shown on Figure 12. Because of asynchronous nature of system power-up, some conditions must be met to quarantee a valid power-up reset of the GAL16V8. First, the Vcc rise must be monotonic. Second, the clock input must become a proper TTL level within the specified time (tPR). The registers will reset within a maximum of tRESET time. As in normal system operation clocking of the device should be avoided untill all input and feedback path setup times have been met.

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