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INTEGRATED SCANNER SENSOR ARRAY ELECTRONICS

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KEY WORDS: sensor array, analog signal processing, smart sensors, integrated circuits integrated analog computation

ABSTRACT: A universal approach to process an array of sensor signals by means of analog preprocessing techniques was developed. It contains analog to digital and digital to analog interfaces for further digital sensor signal processing. Analog preprocessing of sensor signals is preferred to digital in many cases. For instance, it is necessary to use analog techniques when the required dynamic range exceeds the A/D converter input voltage range and resolution or when fast operations on a large number of signals have to be performed. Analog processing is also cost and performance effective where fine step or even continuous regulatory loops are required.

INTEGRIRANI ELEKTRONSKI VEZJI ZA POLJE SENZORJEV ZA SKANERJE

KLJUČNE BESEDE: senzorska polja, analogno procesiranje signalov, pametni senzorji, integrirana vezja, integrirano analogno računanje

POVZETEK: Razvita je bila tehnika za analogno predprocesiranje signalov senzorskega polja. Vsebuje vmesnike med analognim in digitalnim okoljem, ki omogočajo nadaljnje procesiranje signala. Analogno predprocesiranje je pogosto ustreznejše n.pr. v primeru, ko zahtevano dinamično območje presega območje in občutljivost A/D pretvornika ali pa kadar gre za hitro pretvorbo množice kanalov. Analogno procesiranje je tudi učinkovitejše pri razmerju med ceno in lastnostmi in kadar gre za zvezne ali diskretne regulacije s finim korakom.

INTRODUCTION

A standard analog cell approach (1,2,3,4) was extended to effectively design smart sensor electronics in an advanced analog CMOS process.

Several functional blocks were developed for smart sensor signal processing.

Optimal signal processing of an array of analog signals can be achieved by combination of analog and digital approaches. Digital signal processing offers better flexibility than analog; however, it is often not applicable or too expensive, due to final resolution of A/D converters and large amounts of parallel signal processing.

In the described approach, the benefits of digital signal processing are retained after applying analog preprocessing, and through digital control of the analog processing parameters. Figure 1 shows the block diagram of the smart sensor electronics.

It consists of the following building modules:

1. DC sensor level equalizing module.
2. Sensor sensitivity equalizing module.
3. Sensor sensitivity reference module.
4. Sensor trip-point positioning module.
5. A/D dynamic range expansion module.
6. A/D & D/A converters and digital signal processing module.

Modules 1 through 4 were integrated in a two chip system.

Block 1 performs the solution of n integral equations:

$$f_{out_i}(t) = f_{in_i}(t) - \frac{A}{Ta} \cdot \int_{-\infty}^{t} f_{out_i}(\tau)\, d\tau \qquad (\#1)$$

where Ta is selected time constant and A is the amplification of variable gain.

Block 2 can be described with n equations:

$$f_{z_i}(t) = \frac{f_{out_i}(t) \cdot R(t)}{\int_{-\infty}^{t} \left| f_{out_i}(\tau) \right| e^{\gamma/Tb} d\tau} \qquad (\#2)$$

where Tb is a gain equalizing time constant and R(t) is a reference voltage computed in block 3. Block 3 solves equations 3 and 4:

$$R(t) = \frac{\int_{-\infty}^{t} \left| \frac{1}{n} \sum_{i=1}^{n} f_{in_i}(t) - \bar{v}(\tau) \right| e^{\gamma/Tb} d\tau}{\int_{-\infty}^{t} e^{\gamma/Tb} d\tau} \qquad (\#3)$$

$$\bar{v}(t) = \frac{1}{n} \sum_{i=1}^{n} f_{in_i}(t) - \frac{K}{Ta} \int_{-\infty}^{t} \bar{v}(\tau)\, d\tau \qquad (\#4)$$

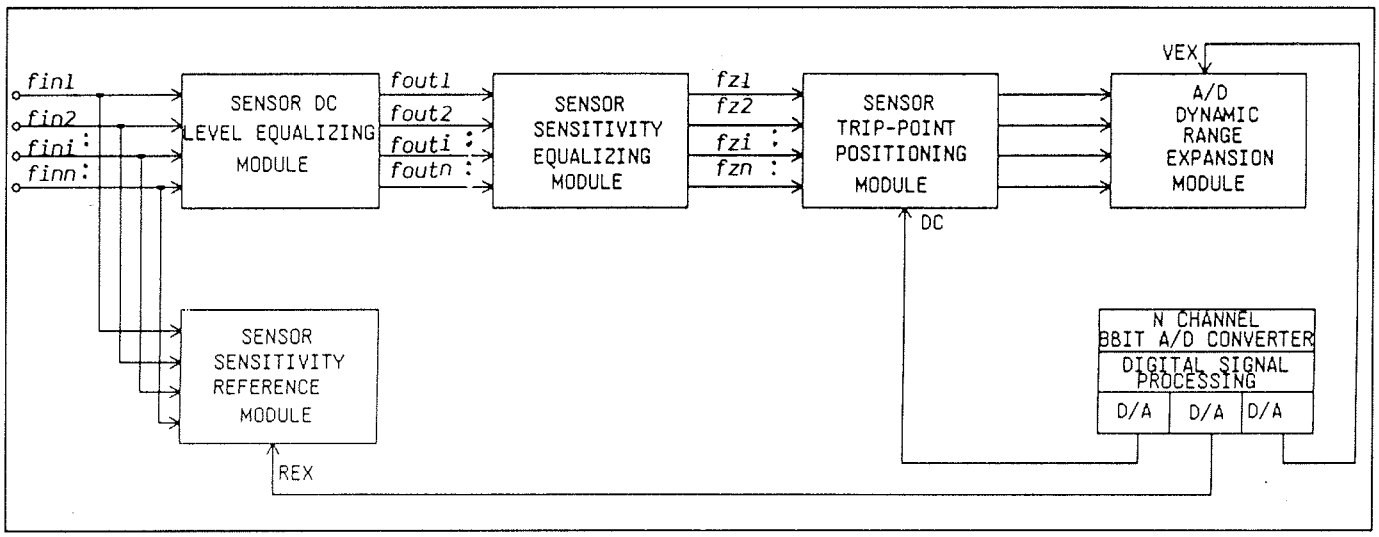

Figure 1: The block diagram of the smart sensor electronics

where K is the Vex to Vref ratio and is controlled externally through the variations of Vex.

Modules 4 and 5 operate in two modes using non-linear elements. Their behaviour can be better understood by describing its actual electronic implementation rather than mathematical description.

FUNCTIONAL DESCRIPTION OF ANALOG SYSTEM

It is almost impossible to manufacture an array of sensors having the same physical properties. Therefore, it is necessary to adjust the DC level and transformation characteristics of individual sensors in an array to equalize their apparent characteristics. This analog signal processor performs transformations of the sensor output signals to equalize the long-term average output characteristics of all sensors in the array. The characteristics of importance are the long-term average and RMS output values. Sensor arrays are often employed when scanning techniques are not permitted. Such situations can exist when high frequency response or high resolution is determined from the measurement system. Mechanical, mechanical/optical, and optical scanners are not usable in many applications due to size and/or reliability considerations. The sensor array permits a lower cost, mechanically simpler, and smaller solution, without the inherent reliability problems found in a mechanical system.

Referencing figure 2, over the physical interval (X2-X1), the functional relationship between the physical quantity being measured and the output voltage of the sensors is approximately linear.

The sensors differ from one another in output offset voltage and sensor sensitivity as shown on the upper left graph in figure 2.

This graph represents the family of characteristics of n sensors. All analog processing on the represented family of sensor characteristics is grouped into two transformations. The first transformation performs equalization of all sensor sensitivities and DC voltage offsets. The second transformation expands the selected physical interval to the full range for the A/D converter used in the system. This step is represented by the lower left graph in figure 2.

CHIP DESCRIPTION

The described system has been implemented in two chips for an 8-channel array sensors.

Analog computation techniques were selected to design the described system. Standard analog cell design methodology (1,3) allowed IC design of both chips containing over 140 analog operators such as integrators, sumators, multipliers, and closed loop amplifiers, together with required digital logic.

The sensor equalization methodology is based on the assumption that information is contained only in the higher frequency components of the sensor signal (above 100 Hz), while lower frequency components are the same for all sensors. All sensors are equalized so that they have the same longterm RMS value, disregarding DC offsets.

CHIP A DESCRIPTION

Figure 3 shows a simplified block diagram of the circuit for performing the first transformation.

The upper block in Figure 3 performs computation of equations 3 and 4 to generate the reference voltage R(t). This voltage can be described as the exponentially

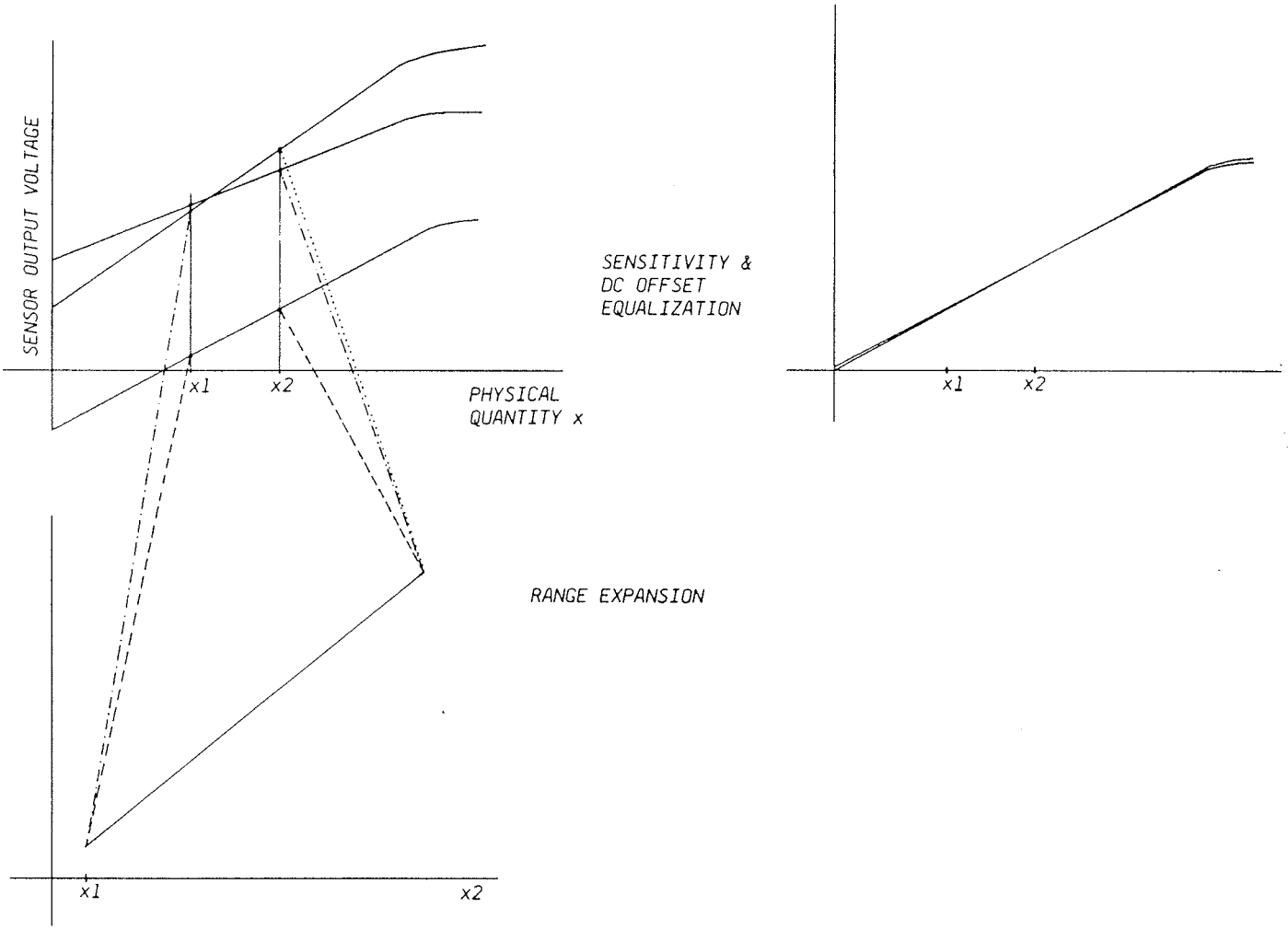

Fig.2 Family of characteristics of n sensors

weighted mean value of the rectified AC component of the sum of the n sensors and is used as a reference voltage in each of eight sensor channels. Using a reference which basically represents an average sensor ensures that gain control will not decrease sensor signal dynamic range. The simplified schematic of one sensor channel is shown in the lower portion of figure 3. This portion solves equation 1 and 2.

Every signal channel has a variable gain amplifier which is controlled by differential integrator 2. This integrator monitors the difference between the reference voltage and the rectified AC component of the channel, equalizing the signal levels for all channels. DC blocking is accomplished by integrator 3 in the feedback loop of the variable gain amplifier. Integrator 3 also reduces the error caused by the offset voltage in the amplification path.

Figure 4 shows the implementation of the variable gain block.

The variable amplification block consists of two inverting amplifiers. The first is used for summing the input signal and the signal from the DC blocking integrator (S3) ensuring that only the AC component is applied to the second amplifier, which has variable gain. Both transistor pairs act as variable resistors to controle voltage gain of the second operational amplifier. Non-linear behaviour of the MOS transistor used as variable resistor is minimized by using gate control voltages exceeding the power supply. Voltage level translation is performed with poly silicon resistors and external high voltage sources.

Harmonic distortion is reduced by the DC blocking of the first amplifier and through optimization of the ratio of N and P transistor sizes. This allowed the achievement of total harmonic distortion less than 0.4% within the 10 dB regulation range used for normal signal levels.

External capacitors are used for integrators, to ensure time constants large enough so that the regulatory loops do not affect the information carrying frequencies.

The stability of the regulation in this circuit is not critical, because of large integrator time constants and the separation of the two regulatory loops.

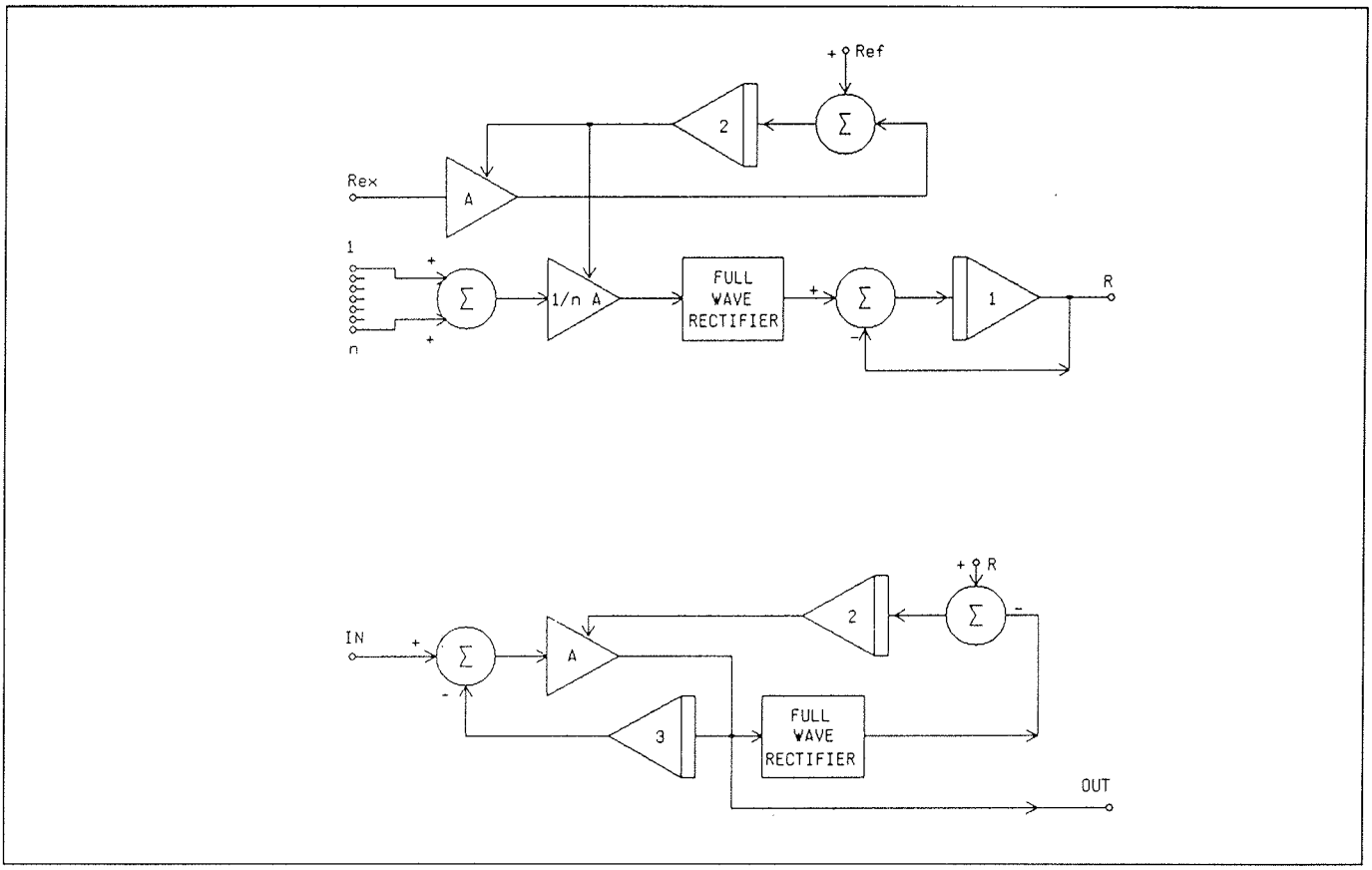

Fig.3: A simplified block diagram of the circuit for performing the first transformation.

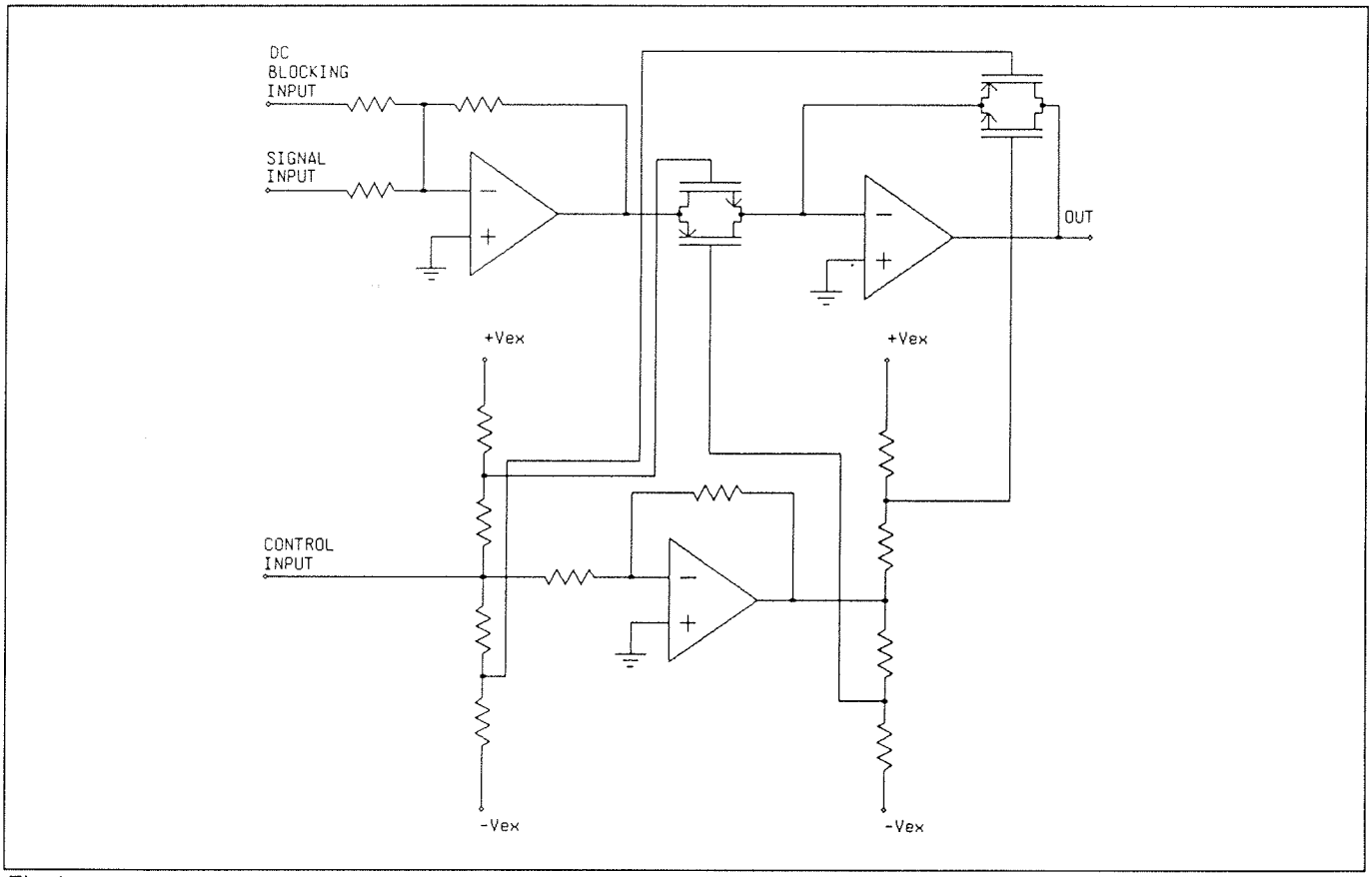

Fig.4: The implementation of the variable gain block.

CHIP B DESCRIPTION

The outputs of the described circuit, chip A, are the inputs to the circuit performing the second transformation, chip B. A block diagram of one channel of chip B is shown in figure 5. A DC voltage is added to the input signal to select the position of the voltage window corresponding to the physical interval of interest. It can be the same for all channels, or can be made different using channel select pins and an internal decoder. This feature offers the possibility of additional software correction of sensor mismatches. This voltage can be set once, or stepped through different values to provide coverage over a longer range of physical intervals, and allows a wide range of control applications, from simple to sophisticated microprocessor control.

The amplification factor of the variable gain amplifier defines the window width. While the first circuit works continuously, the second one has two modes: operation, and adjustment. The adjustment mode has two phases. In the first phase, the DC value is set, and in the second phase, the gain value is set. In the first phase, all inputs are connected to ground, and integrator 1 forces the output of the amplification path to zero voltage. This reduces the error caused by the offset voltage in the amplification path to less than $\pm$ 5 mV. At the end of phase one, the input of integrator 1 is disconnected and

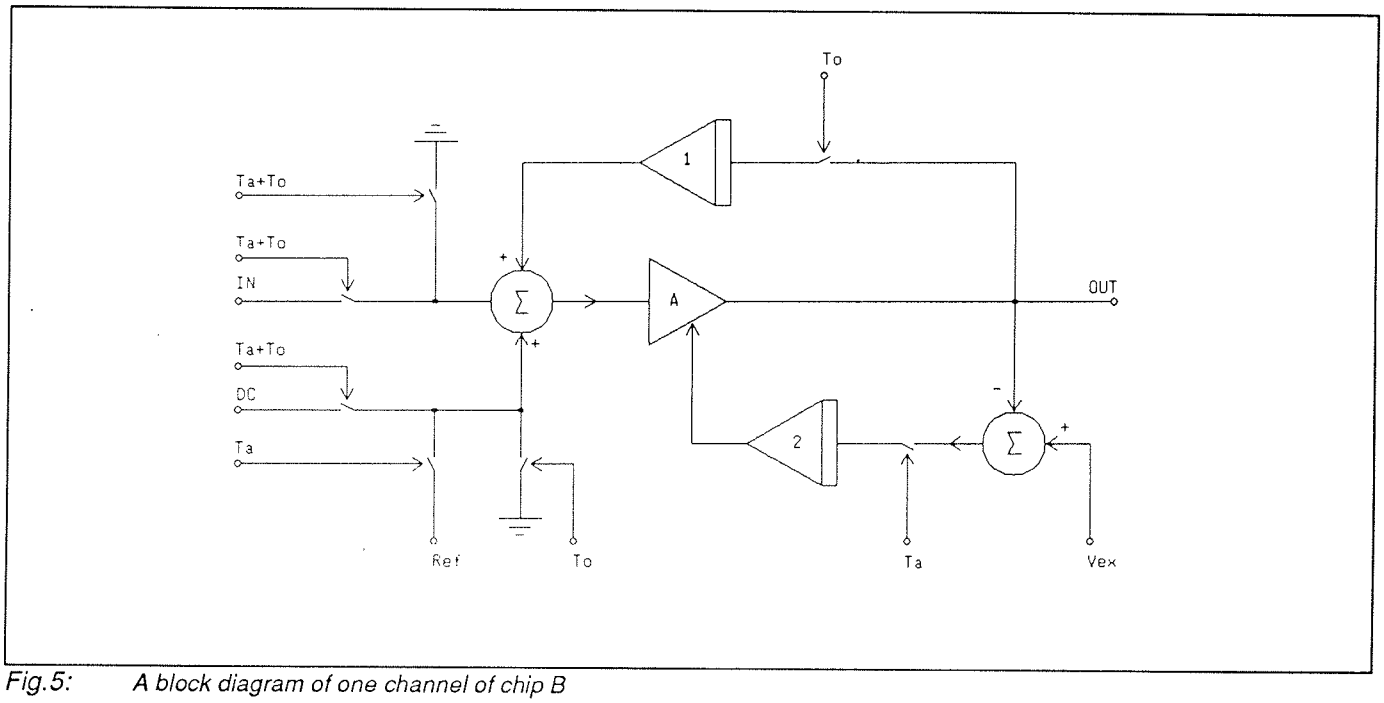

Fig.5: A block diagram of one channel of chip B

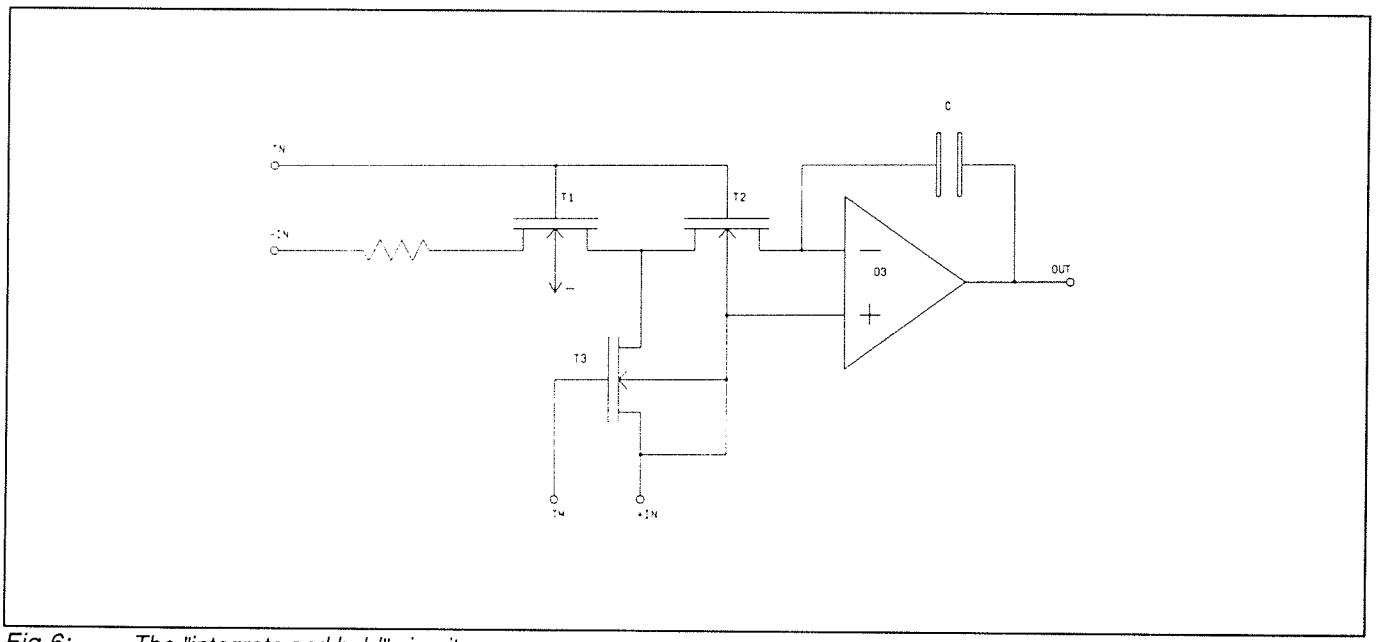

Fig.6: The "integrate and hold" circuitry

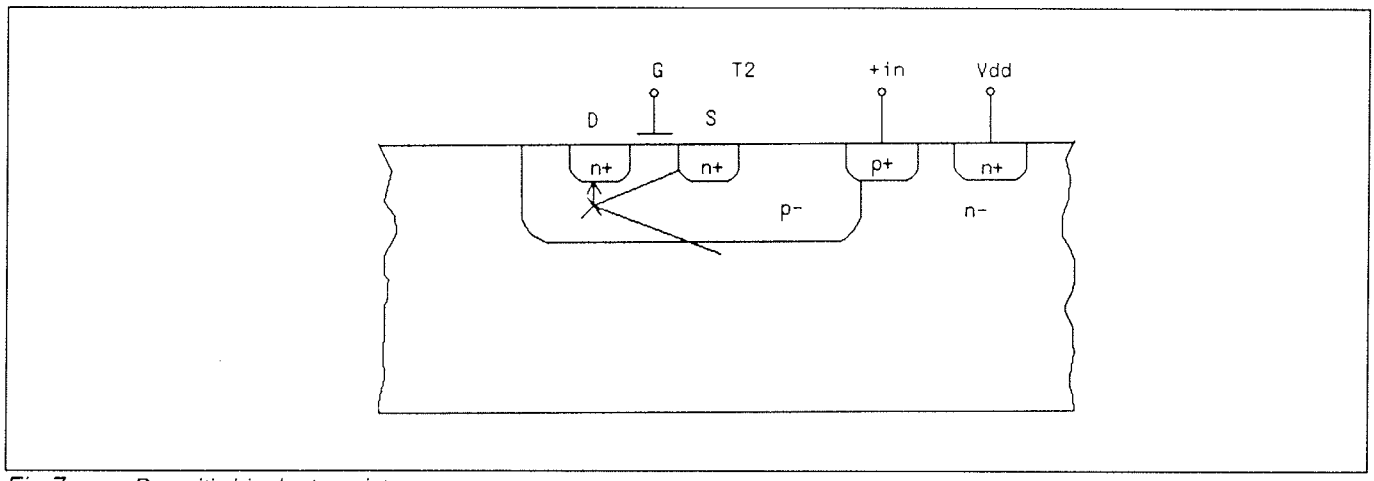

Fig.7: Parasitic bipolar transistor

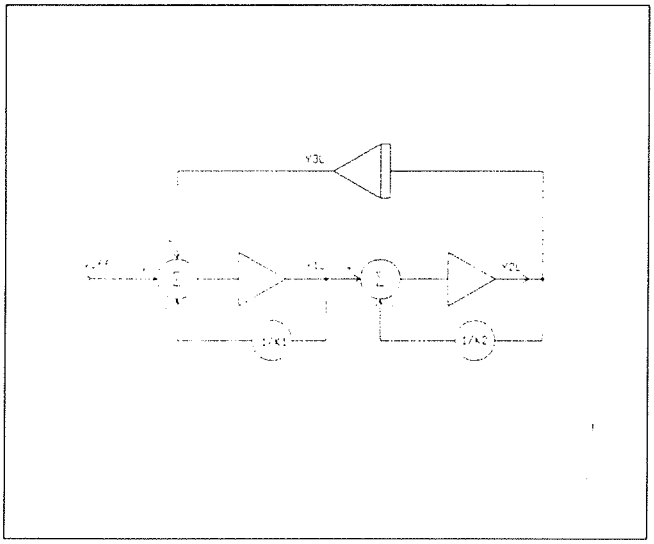

Fig.8: Regulatory loop

the integrator holds the output voltage. In the second phase, the input of the amplifier is switched to the reference voltage (Vref) and its output is compared to the external control voltage (Vex). Differential integrator 2 compares the output of the amplifier to the external control voltage and adjusts the gain until they match each other. At the end of phase two, the input of integrator 2 is disconnected, allowing the offset correction voltage and gain to remain constant during the operation mode. The switching between operation and adjustment modes is defined externally for the system application.

Several design refinements were employed to make this chip cost effective without sacrificing its performance and flexibility.

The "integrate and hold" circuitry shown in figure 6 was designed for minimum drift during the operation period. The main source of the integration drift is source to body leakage current of transistor T2. To minimize this current the body of transistor T2 is connected to the positive input of the integrator. During the operation mode the regulation is in steady state, and source and bulk potential of transistor T2 are equalized. Switching transistors T2 and T3 were added to prevent the current flow caused by parasitic bipolar transistor shown in cross section on figure 7. All integrator elements were integrated. The selected integrator time constant Tc is only 10 microseconds to minimize silicon area. However, the experimental results indicate that the operation mode could be extended to several seconds with only a few milivolts of output drift, even at the highest operating temperatures.

Design for stability of both regulatory loops in chip B is critical and needs special attention, due to the fact that the integrator time constants are very short compared to the poles and zero of the operational amplifier used.

Additionally, the maximum gain of the signal path is over 45 dB, and is variable, agravating the stability problem.

The behaviour of the regulatory loop shown in figure 8 is described as follows:

$$\frac{d^2y_1}{dt^2} + \frac{dy_1}{dt}\left(\omega_1 + \omega_2\right) + y_1\omega_1\omega_2 - A_0\omega_1\omega_2x_1 = 0 \qquad (\#5)$$

$$x_1 = V_{off} - \frac{Y_{1L}}{K_1} Y_{3L} \qquad (\#6)$$

$$x_2 = Y_{1L} - \frac{Y_{2L}}{K_2} \qquad (\#7)$$

$$\frac{d^2y_2}{dt^2} + \frac{dy_2}{dt}\left(\omega_1 + \omega_2\right) + y_2\omega_1\omega_2 - A_0\omega_1\omega_2x_2 = 0 \qquad (\#8)$$

$$x_3 = \frac{Y_{2L}}{Tc} \qquad (\#9)$$

$$y_3 = \int x_3\, dt \qquad (\#10)$$

where K1 and K2 are selected amplification factors for the signal path; and Y1L, Y2L, and Y3L are operational amplifier output signals with limited output voltage swing.

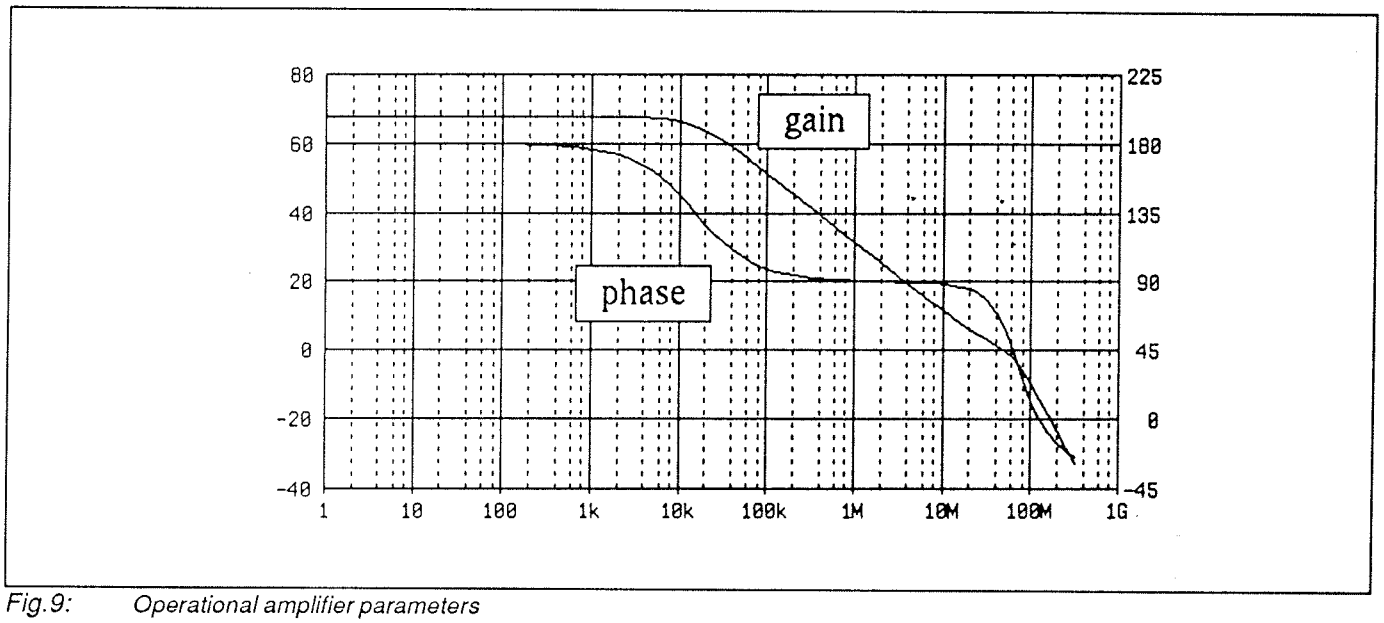

Fig.9: Operational amplifier parameters

Operational amplifier parameters were identified by worst case measurement of the transfer function of standard analog cell 03 as shown in figure 9. The stability analysis was performed by solving sets of differential equations using SIMCOS (5).

Some of the measured results on both chips are summarized in table A.

TABLE A

Specification Summary - chip A

CIRCUIT 1

Channel range:	8
Frequency span:	100 Hz - 1 MHz
Gain correction range:	±10 dB
DC blocking range:	±2 V
Nominal output level:	1.5 V pp
Maximum input voltage:	4 V pp
Output DC error:	<10 mV between any two channels
Output RMS mismatching:	<10 mV between any two channels
Total harmonic distortion:	<1% (signal 1.5 F pp)

Specification Summary - chip B

CIRCUIT 2

Channels:	8
Frequency span:	100 Hz - 1 MHz
Variable gain range:	17 - 45 dB
Nominal output level:	4 V pp
Total harmonic distortion:	<1%
Output DC error:	<10 mV between any two channels
Gain mismatch error:	<0.5%
Gain feedback controle loop setting time:	<100 µsec
Offset correction setting time:	<20 µsec at 40 dB gain

Photomicrographs of chip A and chip B are shown in figure 10a and 10b.

CONCLUSION

Analog signal preprocessing for an array of 8 sensors was implemented in a two-chip set, using an advanced analog CMOS process. This technique is superior to digital approaches. It offers wider signal range and substantially improved resolution. To achieve similar resolution in a digital system would require 18 bit A/D

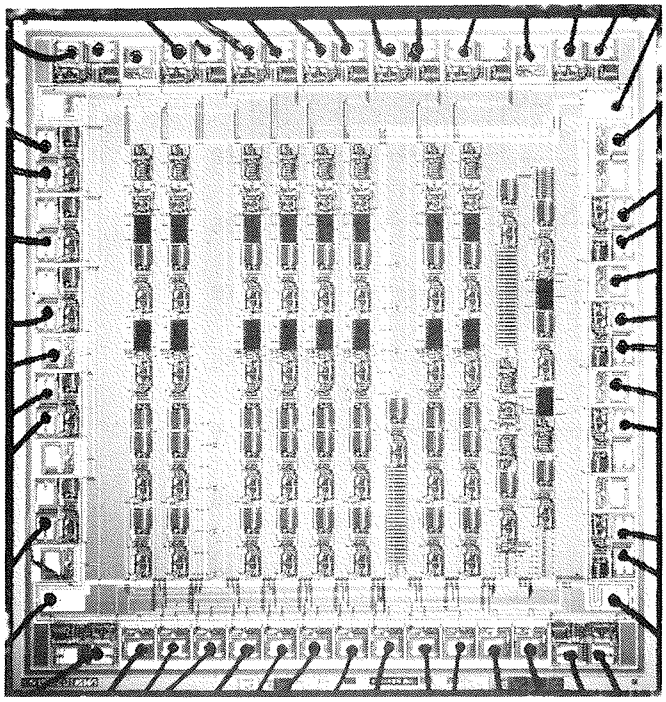

Fig. 10a: Chip A photomicrograph

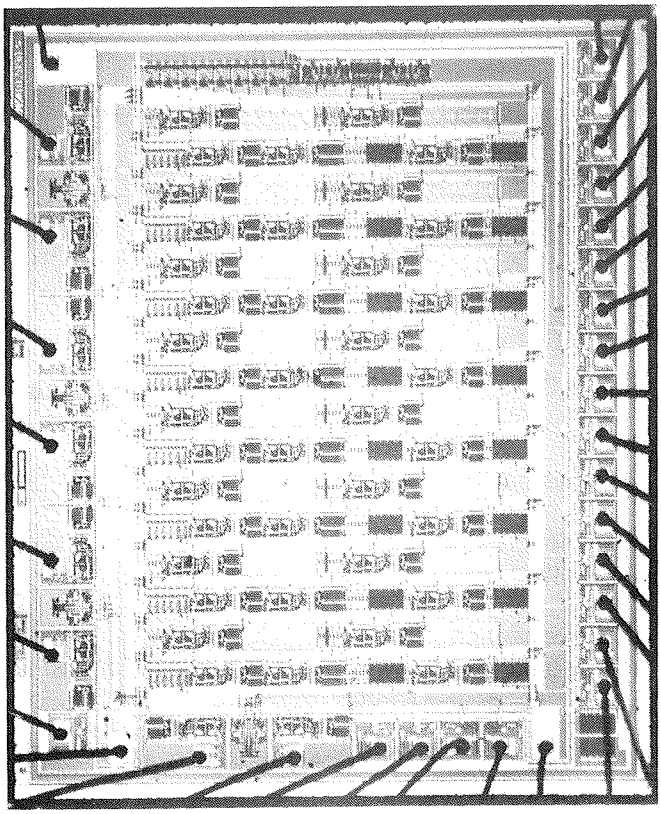

Fig. 10b: Chip B photomicrograph

conversion. A standard analog design approach was used to design this two-chip set. The set can be used in a wide variety of applications and is adaptable to many different sensors. The methodology described is expandable to large sensor arrays.

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