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ANALYSIS AND DESIGN OF LOW VOLTAGE OVERSAMPLING ΔΣ DATA CONVERTERS

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KEY WORDS: oversampling technique, A/D converter, D/A converter, modulation, demodulation, PCM, CODEC, S-C filters, circuits design, circuits analysis

ABSTRACT: An attractive implementation of high resolution A/D and D/A converters in VLSI technology is oversampling technique. In these paper brief overview of oversampling technique is given with the analysis, design and measured results for 13 bits low voltage oversampled A/D and D/A converters. A detailed design procedure is presented for the analog portions of each converter. Standard second order modulator topology was chosen because of its simplicity, robustness and insensitivity to the accuracy of the elements. It is shown that theoretical limit of 15 bits for oversampling ratio of 128 of such modulators can not be reached even with ideal modules which is proved by the simulation for the second order case.
Low voltage and low consumption operation is possible by appropriate design of basic building blocks and by taking into account important design parameters. Since the supply voltage can be as low as 2.4V the modulator uses fully differential structure to achieve required resolution. Low noise fully differential opamp with resistive common mode feedback circuit is used as a basic building block. Similar opamp is used in 1bit D/A converter circuit as well as in a corresponding S-C filter.

ANALIZA IN NAČRTOVANJE NIZKO NAPETOSTNIH KONVERTERJEV ΔΣ S PREVZORČENJEM

KLJUČNE BESEDE: tehnika prevzorčenja, konverterji A/D, konverterji D/A, modulatorji, demodulatorji, PMC, CODEC, filtri S-C, načrtovanje vezij, analiza vezij

POVZETEK: Ena od možnosti za realizacijo konverterjev A/D in D/A z visoko ločljivostjo je uporaba tehnike prevzorčenja. V članku je podan pregled tehnike prevzorčenja ter analiza, načrtovanje in merilni rezultati 13 bitnega nizkonapetostnega konverterja A/D in D/A.Podan je postopek načrtovanja za občutljivejše analogne dele konverterjev. Zaradi enostavnosti, robustnosti in neobčutlivosti na spremembe elementov in parametrov je za modulator uporabljena topologija drugega reda. Ločljivosti 15 bitov za razmerje med vzorčevalno in Nyquistovo frekvenco 128, ki jih podaja poenostavljena teoretična analiza ni mogoče doseči, kar dokazujejo rezultati simulacij idealiziranega modulatorja drugega reda. Izbira primernih diferencialnih nizkonapetostnih osnovnih gradnikov omogoča gradnjo konverterjev, ki delujejo z nizko napajalno napetostjo in imajo nizko porabo. Primerna je diferencialna struktura z uporovnim sofaznim povratnim vezjem. Podobni operacijski ojačevalniki so primerni osnovni gradniki tako za modulator, kot tudi za eno bitni D/A konverter in pripadajoči filterS-C.

1. Introduction

The introduction of fine line MOS processes provides a cost effective solution to built a flexible VLSI systems. As channel length of MOS processes continue to decrease, digital signal processing is becoming more attractive compared to analog signal processing because of high speed, better programmability, higher reliability, etc., but some analog signal processing is still needed. Among the analog blocks which must be integrated are antialiasing and/or smoothing filters, noise shaping filters, amplifiers and low cost, high resolution A/D and D/A converters. The applications of such analog modules are in the areas of instrumentation, telecommunications, audio, and video. Important requirements in portable systems are low consumption and low voltage operation *($V_{sup} < 3V$)* for battery operated systems.

Continuous time or sampled data filtering in analog domain followed by A/D conversion with the Nyquist rate converter was traditional way of signal processing in the integrated systems. Flash converters are appropriate for video applications, successive approximation converters for audio and telecom voice processing and integrating converters for low speed data acquisition. Analog filtering either continuous time or sampled data needs precise analog components to realize accurate poles and zeros and thus precise transfer function, while A/D and D/A converters needs precise analog components because each level must be accurate to reach required differential and integral linearity which is in the 13-16 bits range. Usually trimming is necessary. This is expensive and time consuming procedure. The problems which remains in these solution are poor repeatability, reliability, programmability as well as high production cost. New solution provides reduction of the number of precise analog components and their precision requirements to the necessary minimum and handle most of the signal processing with the digital DSP.

The main task of an A/D converter is to convert continuous time signal *x(t)* into a sequence of digital codes *y(kT)*

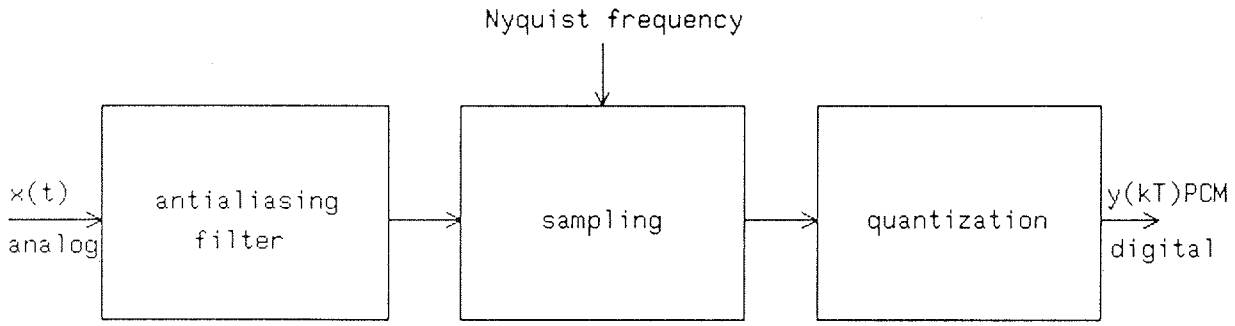

Figure 1: A/D converter block diagram

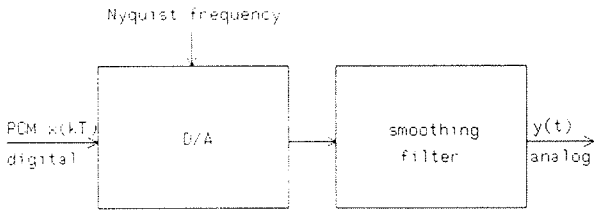

Figure 2: D/A converter block diagram

at the Nyquist rate f_n. In front antialiasing filter is necessary to limit the bandwith of the analog signal to half of the sampling rate. Similar but reversed situation happens on the other side where high frequency part of the spectrum above $f_n/2$ needs to be filtered out to get pure analog signal. The principle block diagrams of both conversions are shown on figure 1 and 2.

Nyquist rate converters perform A/D conversion of analog signal at its Nyquist rate which means that the spectrum of incoming analog signal must be negligible above $f_n/2$. Oversampled converters on the other hand sample the incoming analog signal at a rate which is much higher than the Nyquist frequency $(f_s >> f_n)$ and in this way they make use of high frequency offered by MOS processes. This is possible if the bandwith of the signal is small compared to the speed of available VLSI circuits. Because the sampling frequency is much higher than Nyquist rate the requirements for antialiasing filter are very much simplified and in this way it is possible to integrate it on a VLSI chip. Another difference between Nyquist rate converters and oversampling converters is the quantization. For Nyquist rate A/D converters quantization is performed for every sampling period with full precision of the converter. For example for the 16 bit resolution the spacing of the levels is in the microvolt range which requires much higher matching accuracy of integrated elements than it is really available (7). The solutions of these problems are either trimming or self calibration. Both solutions are expensive in terms of silicon area and time needed for test. For oversampled converters many rough amplitude quantizations are performed during one sampling period which are then averaged with decimation digital filters which purpose is to remove the out of band quantization noise and spurious out of band signals and to resample the signal at a Nyquist rate.

During last 5 years many publications appeared in the technical literature about different solutions for oversampling A/D and D/A converters, a few of them are listed at the end of this article (2) (5) (6) (10) (4) (3). Of the available solutions a second order $\Delta\Sigma$ modulator and 1 bit D/A converter was chosen because of its robustness and reliability.

Oversampling second order A/D and D/A converters were designed as well as corresponding analog filters. Both modules are running with the oversampling ratio of 128 and will be used in telecommunications CODEC. The main issues in designing these two blocks were low operating supply voltage which is available from the battery *(Vsup < 3V)*, low consumption and resolution in the range of 13-14 bits. Since $\Delta\Sigma$ modulators are nonlinear modules accurate analytical technique does not exist to predict the behavior, so our results are based on approximate analytical methods and extensive simulations and measurements.

In these paper short overview of oversampling methods used in A/D and D/A converters is given with the emphasize to the analog part of converters followed by analysis and design of low voltage second order $\Delta\Sigma$ modulator as well as analysis and design of 1 bit D/A converter and corresponding analog filters with the same low voltage and low consumption requirements. Simulation as well as measured results will be presented together with some practical considerations to achieve good crosstalk separation from digital to analog portion of the chip, low noise operation of analog blocks and thus the required resolution even with low operating voltage.

2. Overview of Oversampling Methods for A/D and D/A Conversion

2.1.Description of oversampling A/D converter

Figure 3 shows block diagram of a typical oversampled A/D converter. The first block is antialiasing filter which is necessary to attenuate out of band spectral components. It can be a simple first order passive filter which is integrated on the chip because the oversampling frequency is many times higher than the bandwith of the signal *x(t)*. Modulator block performs many rough quan-

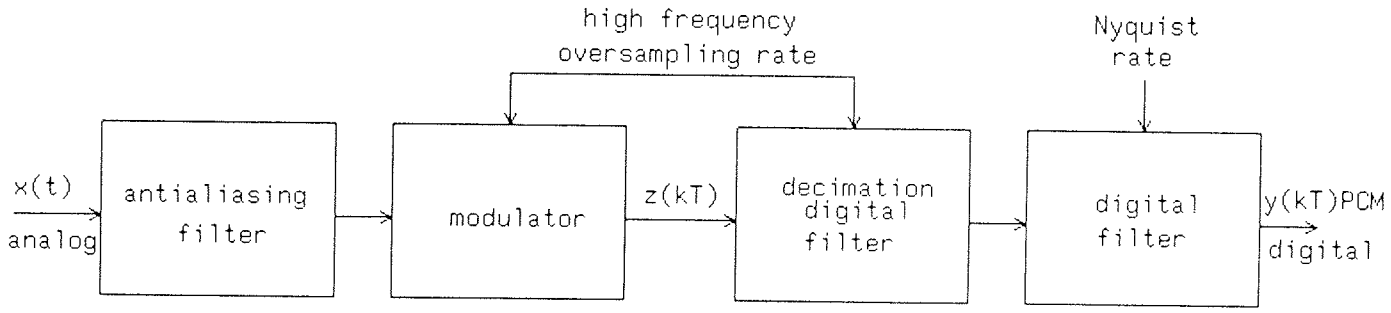

Figure 3: Oversampled A/D converter block diagram

tizations in one Nyquist period and the output signal is so called bits-stream *y(kT)* which is processed by digital decimation filter. Its task is to attenuate out of band quantization noise and resample the signal with the Nyquist rate f_n. The most critical component in the chain is a modulator block which must be carefully optimized to reach required performances.

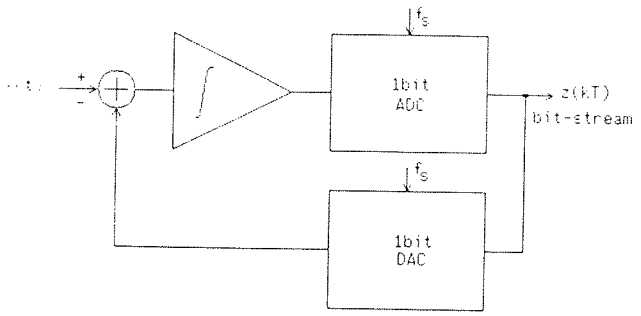

Figure 4: First order ΔΣ modulator - Noise-Shaping Coder

2.2. Modulator

Let us take a simple first order modulator shown on figure 4 to describe the principles of operation. The summing node adds input signal *x(t)* and feedback signal which is coming from the D/A converter. The difference is integrated and the result is D/A converted (usually 1 bit). Output signal is a bit-stream whose average represent the input signal. The averaging process is performed by a decimation digital filter. In general the amplitude resolution of the converter increase when oversampling ratio is increased. Oversampling ratio *D* is defined as the ratio of oversampling frequency f_s to the Nyquist frequency f_n $D=\frac{f_s}{f_n}$. The quantization noise in the baseband is reduced by the use of a feedback in the modulator.

Prediction modulators (figure 5) and noise shaping modulators (figure 4) are basically in useto reduce the quantization noise in baseband (1). The predictive or differential coder works in such a way that the value of the present sample is used to calculate the next value while the difference between actual value and the estimation is quantized by 1 bit converter. These quantized value is stored in H(z) which is a simple integrator for

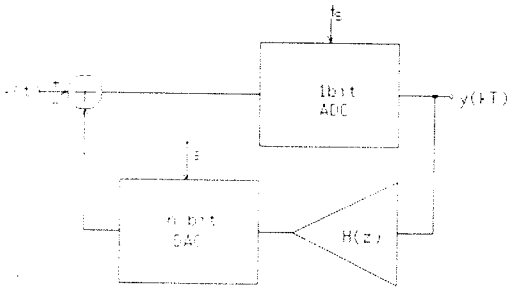

Figure 5: Predictive Coder

the first order modulator. In this way it really reduces the level of the quantization noise in the baseband.

The noise shaping coder shapes the power spectrum density of the quantization error and moves the noise energy towards the higher frequency. If the sampling frequency of the modulator is much higher than the Nyquist rate then this high frequency quantization noise can be attenuated by the use of digital filtering.

It seems that the number of analog components needed is smaller for predictive coders; in reality it requires multibit precision DAC (1) which is not easy to built, while nonidealities introduced by the integrators limit the linearity of such modulators. Besides these two problems, the decimation filter for the predictive coder requires multibit multiplier, while for simple noise shaping coder multiplier in decimation filter is not needed since the output of the modulator contains only 1 bit. All these reasons oblige the use of noise shaping modulator for A/D converter.

Higher order modulators can be built by the use of multiple integrators and appropriate feedbacks. Figure 6 shows comparison of quantization noise spectrum densities for the first and the second order modulator. It is evident that in the passband bigger S/N ratio can be achieved with a second order modulator for the same oversampling ratio. While higher than second order modulators would provide even further improvement in the S/N ratio in the passband these modulators are more sensitive to component inaccuracy, stability restrictions etc.

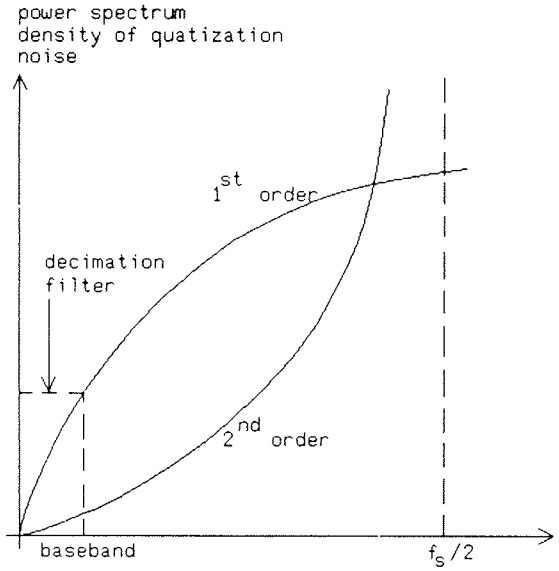

Figure 6: Power spectrum density for first and second order modulators

Theoretical simplified analysis of ΔΣ modulators can be performed with the assumption that quantizer can be modeled as a linear summing or gain element for which power spectrum density of the quantization noise is calculated. Simplified analysis of a second order modulator (figure 7) gives Y(z) as a function of input samples and quantization noise: (equation 1)

$$Y(z) = \frac{X(z)k_1 k_2 + \varepsilon(z)(z-1)^2}{z^2 + z(k_2-1) + k_1 k_2 - k_2 + 1} \qquad (1)$$

The dynamic range of A/D converter is defined as the ratio of the output power for full scale sinusoidal input to the output power for a small input signal whose signal to noise ratio is 0 dB (1). If the quantizer is modeled as a linear gain element with the additive white noise source, then the dynamic range *DR* can be calculated by equation 2 (1).

$$DR = \frac{3}{2}\frac{2L+1}{\pi^{2L}} D^{2L+1} \qquad (2)$$

where L is the order of ΔΣ modulator and D is the oversampling ratio f_s/f_n. The resolution or the number of bits can be calculated with:

$$N_{bits} = \frac{\frac{S}{N}[dB] - 1.76}{6.02} \qquad (3)$$

Figure 8 shows the relation between oversampling ratio and resolution or the number of bits taking order of the modulator as a parameter for idealized first and second order modulator with the quantizer modeled as a linear gain element and quantization noise modeled as white noise source. This equation is valid for maximum input voltage. In reality these assumptions are too optimistic which will be shown in the next subsection. Multibit quantizer and/or D/A converters as well as several other higher order structures are possible.

2.3. Description of oversampling D/A converters

Figure 9 shows block diagram of a typical oversampled D/A converter. The sequence of N-bit digital words is processed by a digital interpolation filter with the Nyquist rate f_n. The interpolation filter performs filtering of image components, interpolation, and upsampling of the digital signal with the oversampling frequency. In this way the word length is reduced from N bits to M bits (usually *M* = 1), while sampling frequency is increased. The interpolation filter removes the sidebands which are the result of sampling with low frequency and interpolates

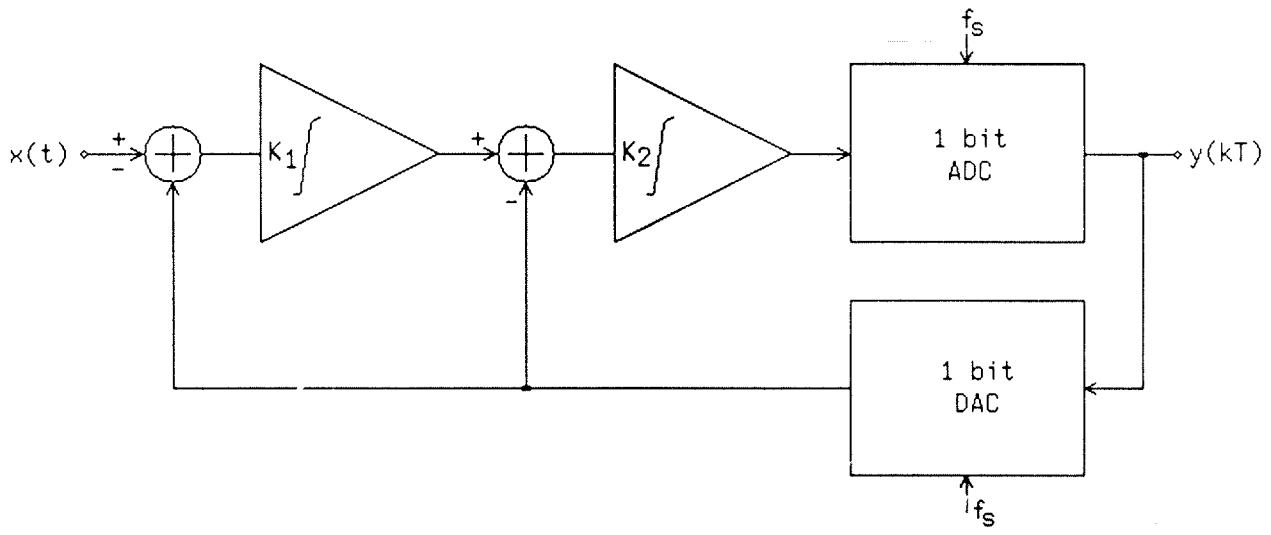

Figure 7: Second order modulator

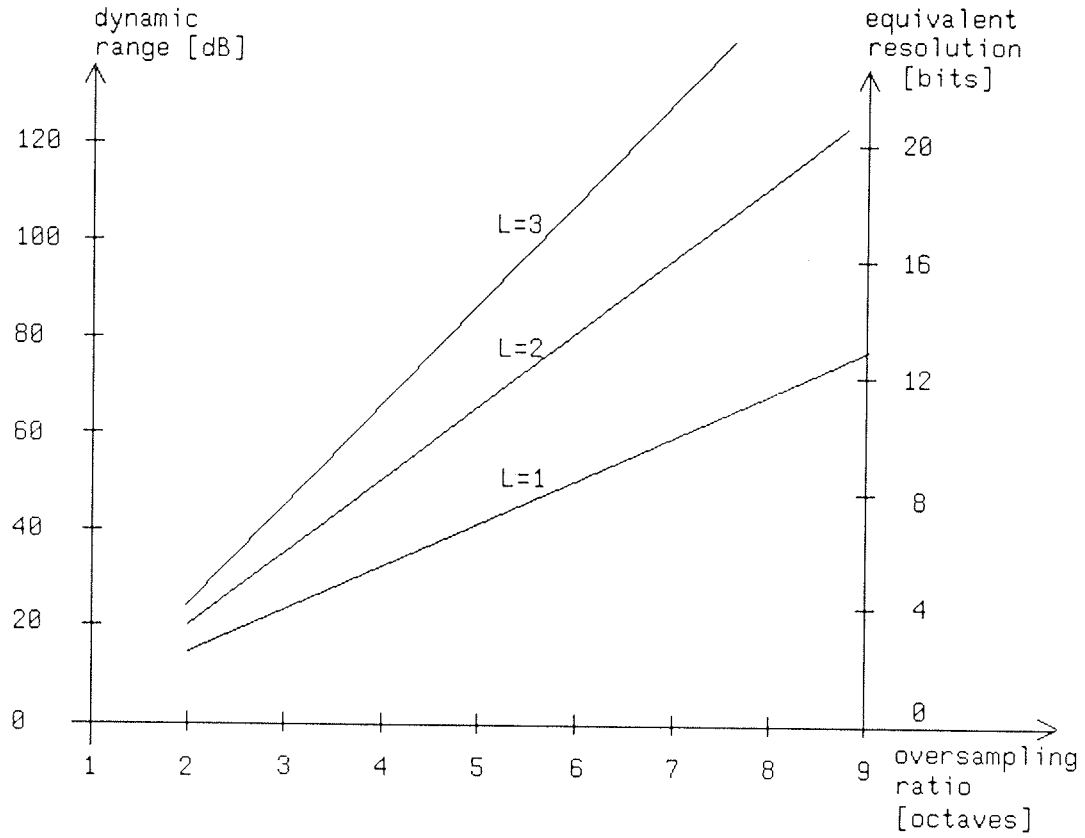

Figure 8: Dynamic range and number of bits

values between samples. The function of digital modulator is to reduce M bit oversampled signal to usually 1 bit signal and to shape the quantization noise to higher frequencies outside the baseband. The actual D/A conversion is performed by 1 bit D/A converter using charge packets generated by switched capacitor network or current sources. Last block in the chain is analog continuous time or sampled data filter whose task is to reduce the quantization noise. Although the performances are theoretically defined by the oversampling ratio and number of bits, the most critical component for the implementation are 1bit D/A converter and analog filter.

The design and implementation of these two blocks will be explained below.

Figure 10 shows simplified block diagram of digital demodulator which performs noise shaping and reduction of word length, while figure 11 interprets the principles of interpolation and upsampling of incoming stream of digital words.

The amount of filtering necessary to attenuate shaped out-of-band quantization noise is dependent on the application, but general rule of thumb is to have analog or

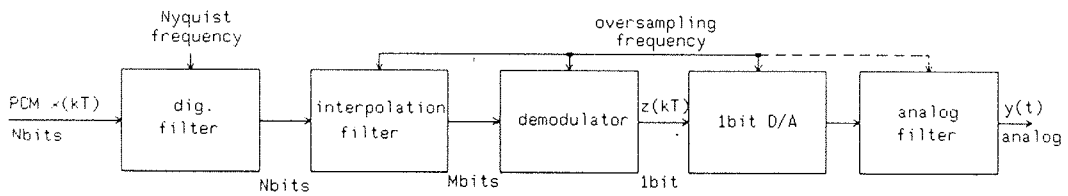

Figure 9: Oversampled D/A converter block diagram

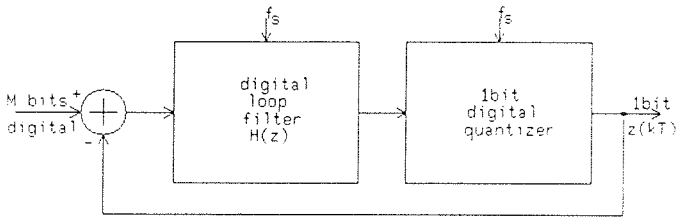

Figure 10: Block diagram of digital demodulator

sampled data filter which must be 1 order higher than the corresponding demodulator; for a second order demodulator 3rd order filter is recommended. For some applications lower order analog or sampled data filtering is sufficient. S-C filter is running with high oversampling frequency, followed by simple continuous time smoothing filter which attenuates images around f_s.

3. Analysis and Design of Low voltage Second Order ΔΣ A/D Converter

For the application of low voltage oversampling ΔΣ A/D converter second order modulator was chosen because the required resolution is 13 bits which can be achieved by the oversampling ration of 128 and second order modulator topology. Figure 12 shows implementation of the second order modulator used in our converter. Because of the low voltage operation, a fully differential structure is needed to increase the $\frac{S}{N}$ ratio and to decrease coupling of digital noise from DSP part of the chip. The simulation of idealized modulator shows (figure 13) that maximum resolution which is possible to achieve for this design is close to 13 bits and not close to 15 bits as predicted by the theory. The reasons for a difference are the simplification of the quantizer and the white noise model of the quantization noise which is just an approximation.

Scaling of the modulator is possible because of the characteristics defined by capacitor ratios. Amplitude distribution of the signals in both integrators must be

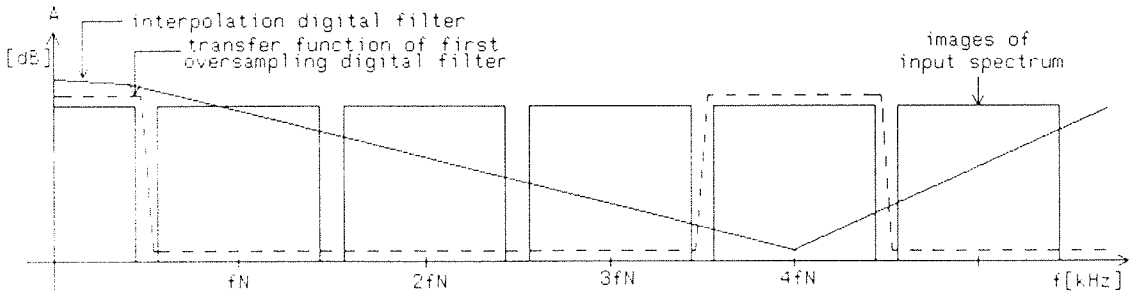

Figure 11: Function of interpolation filter

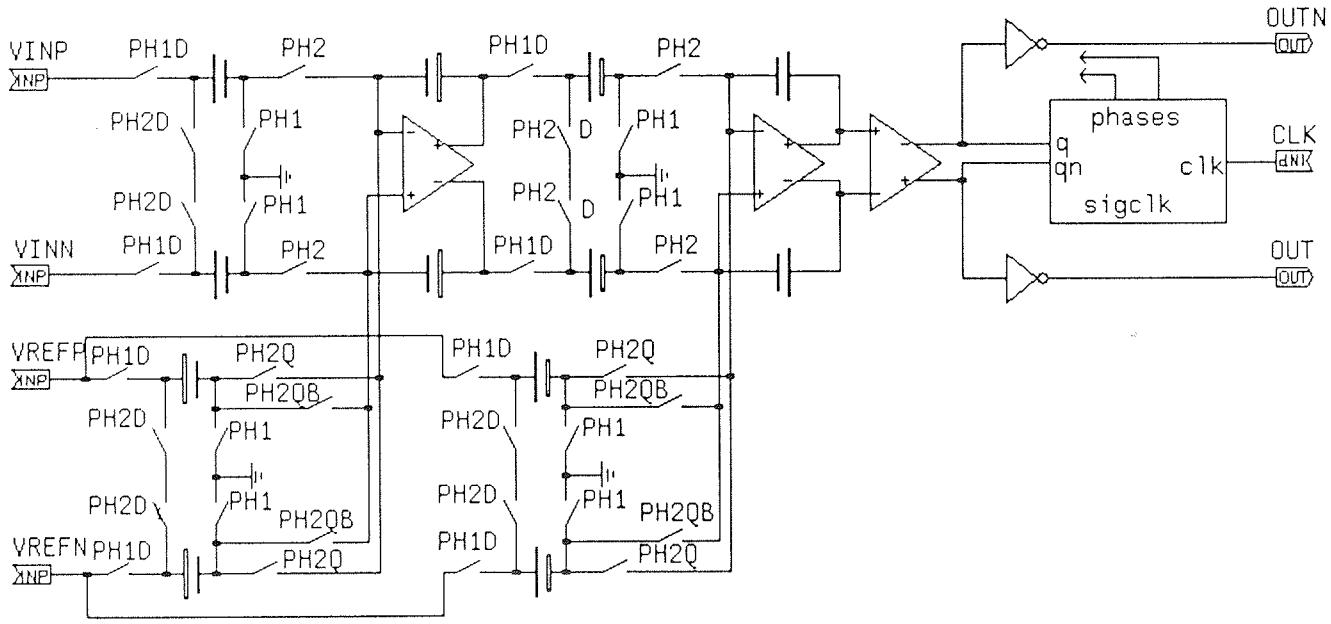

Figure 12: Simplified schematics of 2nd order modulator

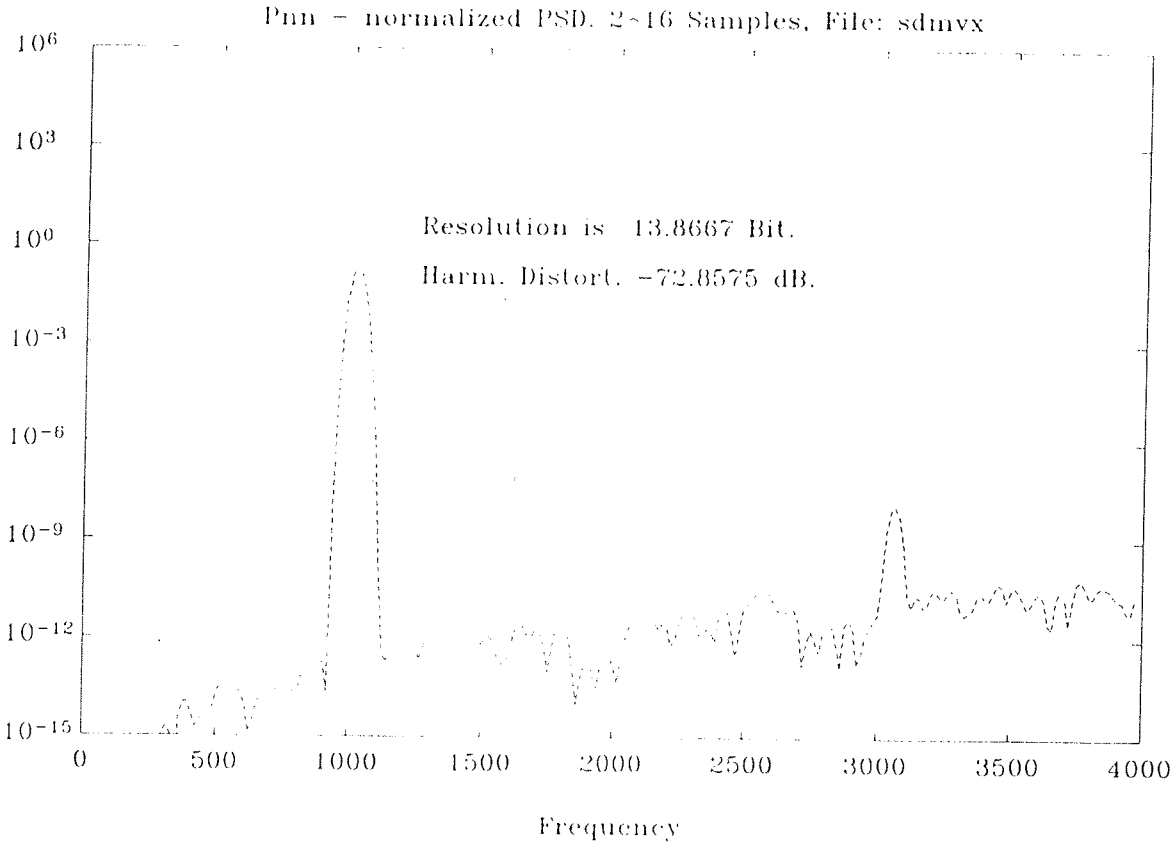

Figure 13: Spectrum of idealized modulator

such that the dynamic range of the converter can be maximum. The noise requirement is especially important for the first opamp because it's noise power enters the loop with no attenuation.

The operational amplifier used in these application is shown on figure 14 together with some of its important characteristics: linearity, gain, offset, noise, settling time, slew rate and gain bandwith. It was proved by the simulation that influence of nonidealities of the opamp as defined on figure 14 are negligible.

A very careful design is needed for the switches and the clock form generator (figure 15). The charge injection

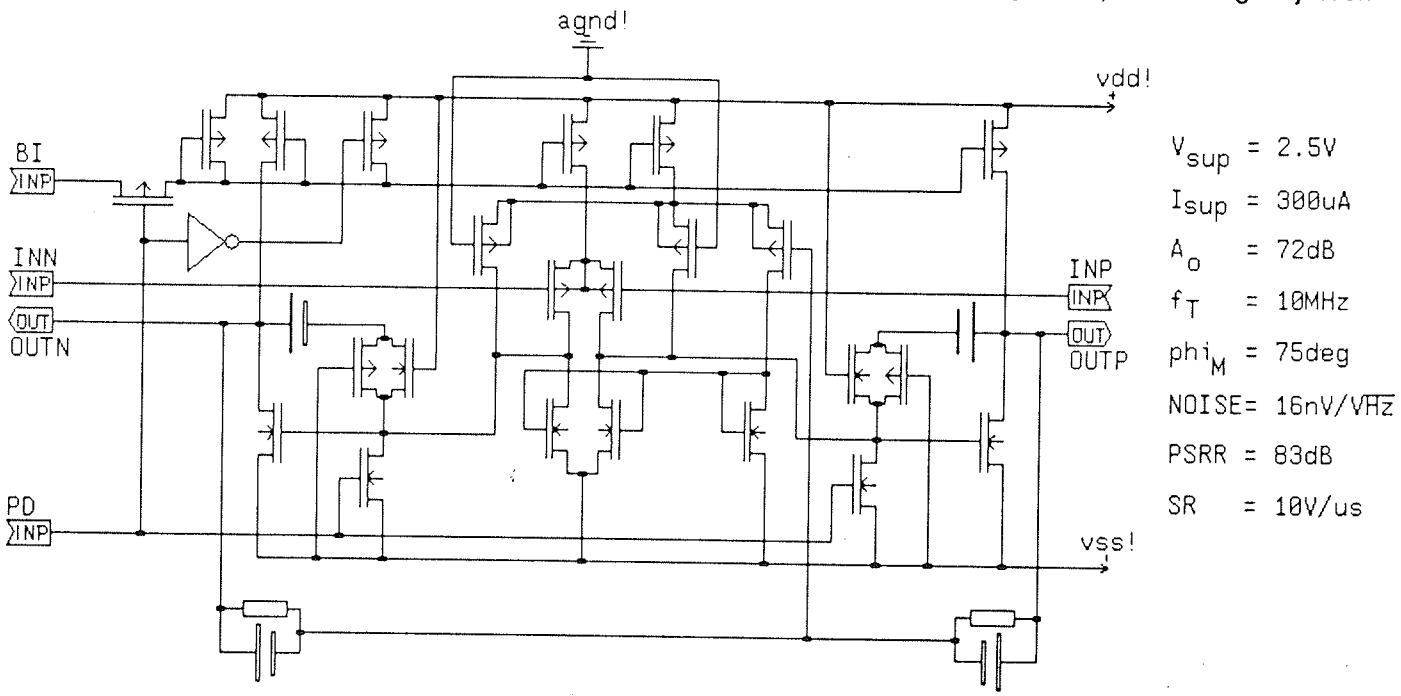

Figure 14: Opamp used in modulator and its parameters

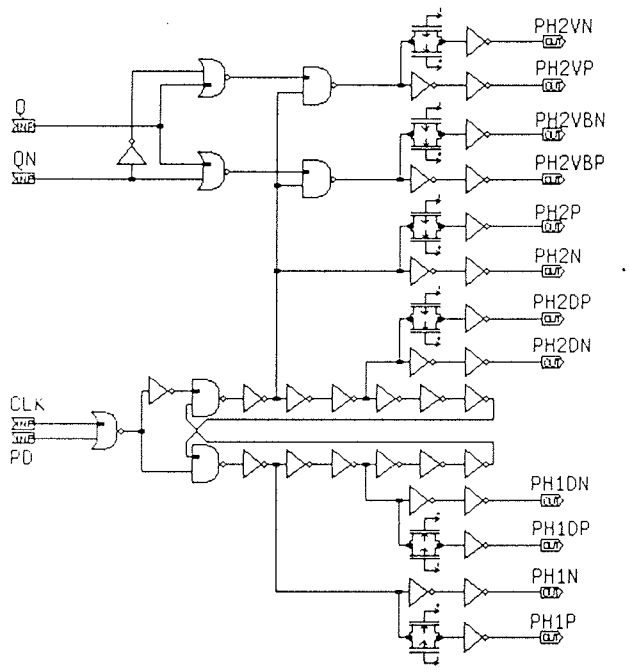

Figure 15: Clock form generator

adds common mode signal which is partially cancelled by the differential structure and the common mode feedback circuit. Signal dependent charge injection (8) is reduced by driving some of the switches with the delayed clocks marked with letter D in the figure 15.

The layout of analog and digital modules needs special technique to prevent coupling of digital noise into analog modules via common substrate and parasitic capacitances. It is reduced by separated connection of substrates and sources in analog and digital modules, and by the extensive use of shielding in sensitive analog nodes. Figure 20 shows layout of the second order modulator.

Figure 16 shows the typical measured power spectrum density as a function of frequency for a second order modulator which is used in the calculation of the number of effective bits of the A/D converter.

4. Analysis and Design of Low Voltage Oversampled D/A Converter

For the D/A conversion a digital modulator is used (figure 10) to perform noise shaping and reduction to 1bit bit-stream. This solution is used because of low supply voltage and inherent linearity of 1 bit D/A converters which is the most critical block of the whole D/A. It is built by a switched capacitor circuit as an input stage of a third order Chebishev S-C ladder filter, which was designed

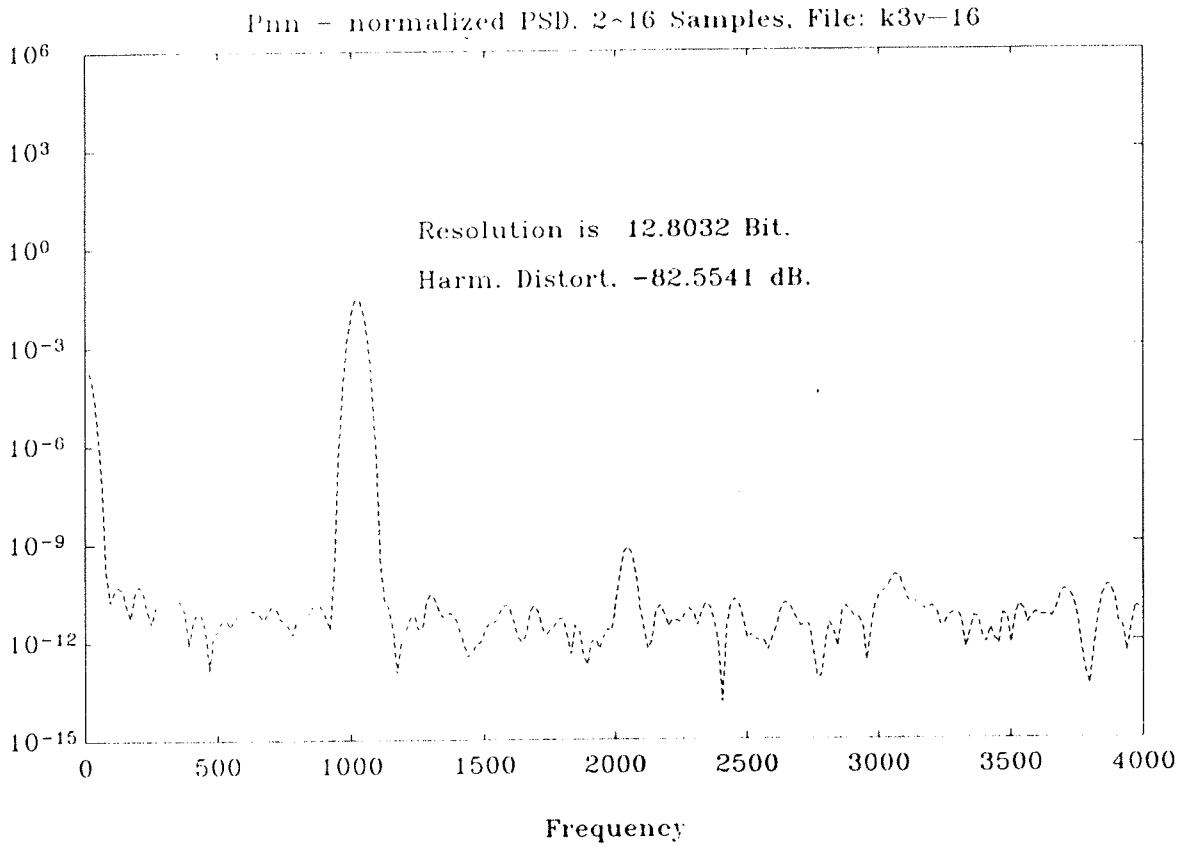

Figure 16: Power spectrum density of measured modulator

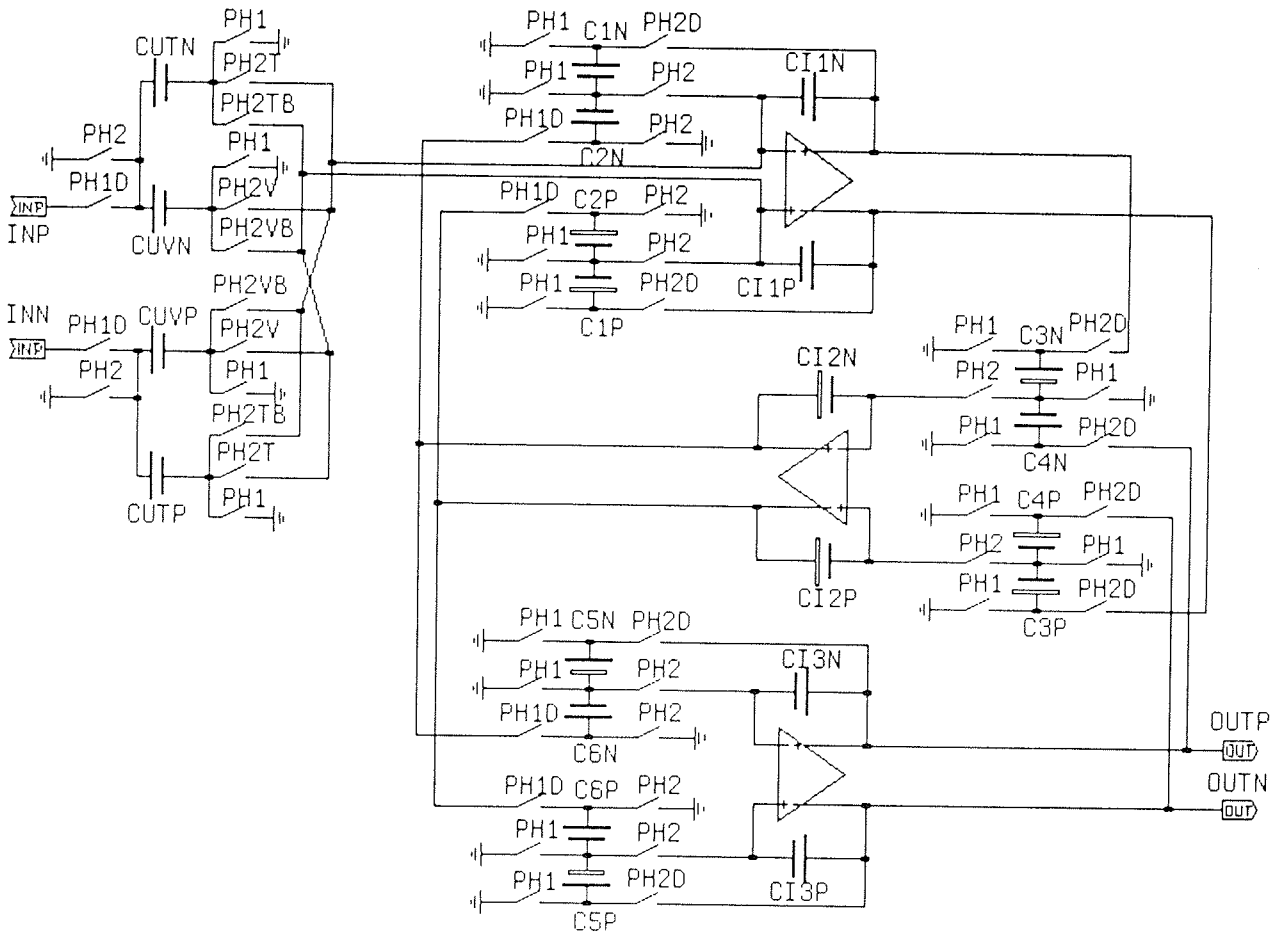

Figure 17: 1 bit D/A converter and filter circuit

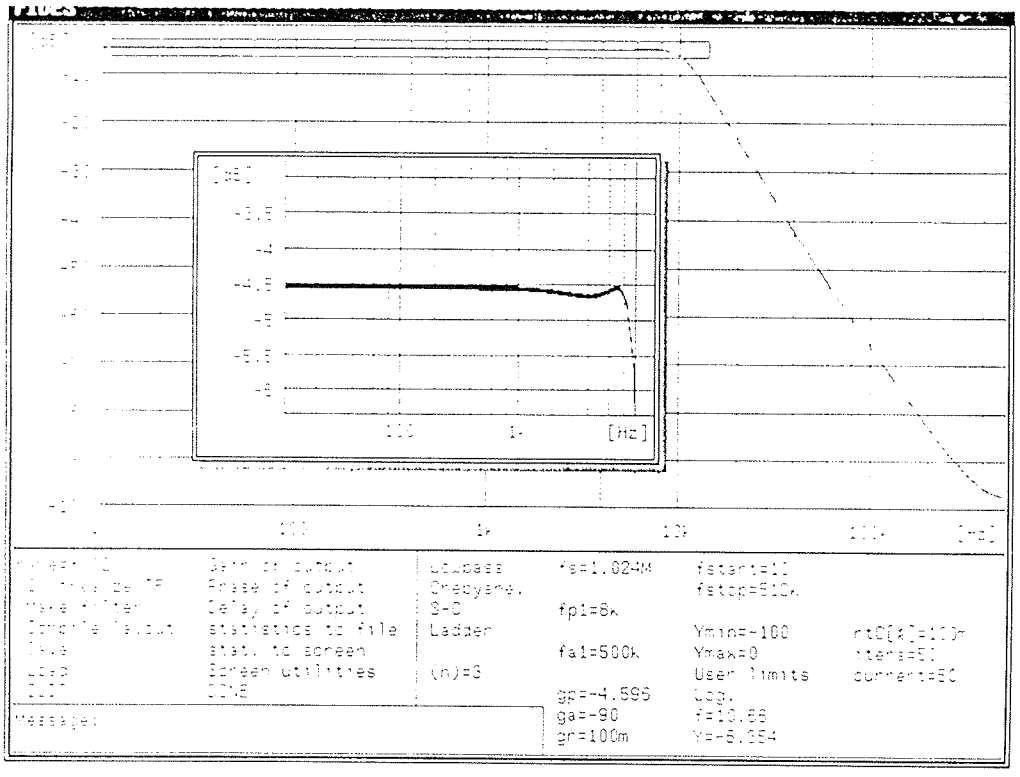

Figure 18: Frequency characteristics of Ladder filter

using FIDES (9). Figure 17 shows a schematic diagram of 1 bit D/A converter and corresponding S-C filter. Figure 18 shows frequency domain characteristics and the definition of filter requirements. Fully differential structure is used to reduce the common mode parasitics signal injection and to increase the dynamic range. A similar opamp as in modulator is used for S-C filter with the only difference in higher gain. The opamp is optimized for noise, which is less than $15\frac{nV}{\sqrt{Hz}}$ at 100 Hz. The flicker noise is reduced by increasing the area of differential stage.

$\frac{KT}{C}$ noise of S-C filter is further reduced by the use of high capacitance of the unit capacitor of about 1pF. 1 bit D/A converter is built as a replacement for the input switched capacitor driven by the appropriate clocks. The circuit is actually composed of two 1-bit D/A converters whose bit-streams are added at the input of the S-C filter; one with the voice information and the other with the signaling information. Digital portion of the D/A converter uses a variation of the clock form generator shown on figure 15. The same circuit and layout design technique were used for D/A converter as for the modulator block.

Input bit-stream generated by digital demodulator is connected to the clock form generator which drives the 1 bit D/A converter and resulting signal is then filtered by the 3rd order Chebishev filter.

The signal to noise ratio in voice band is: $\frac{S}{N} = 85\ dB$ and is calculated from the figure 19 which represents the power spectrum density of the signal at the output of the filter.

Figure 20 shows a layout of analog portion of a second order modulator, 1bit D/A converter circuit and corresponding S-C filter.

Conclusions

In this article overview of oversampling technique used in A/D and D/A converters is given with necessary design steps for the analog portions of both converters to achieve required resolution of 13 bits and low voltage operation. Second order modulator was introduced along with some theoretical and simulation results. It was proved, that real resolution of second order modulator is slightly less than 13 bits and not 15 bits as predicted by the theory and the reasons are shortly explained. The required resolution is possible for oversampling ratio of 128 if basic modules are designed appropriately. The results of measurements of test-chip modulator are in good agreement with the predictions.

1 bit D/A S-C converter and 3rd order S-C filter followed by first order smoothing filter was used for the analog portion of the D/A converter chip. The simulation shows

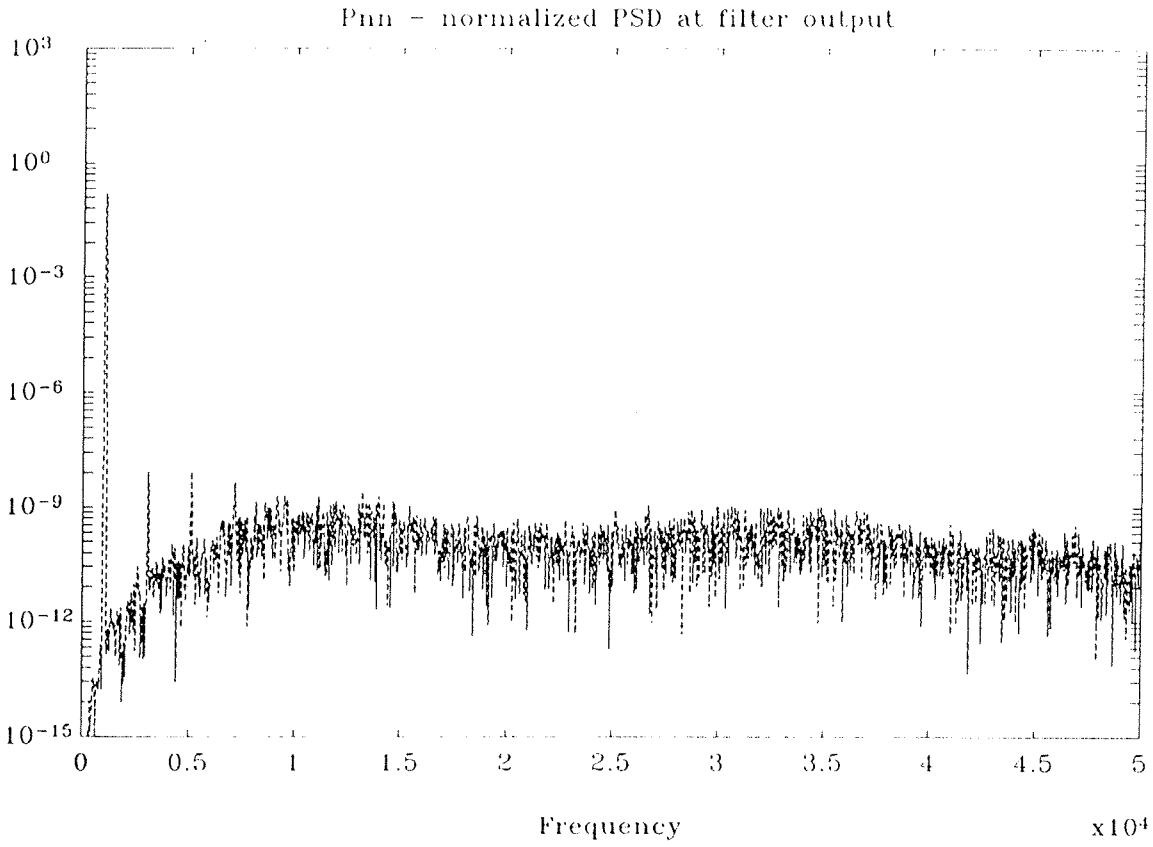

Figure 19: Power spectrum density at the output of the filter

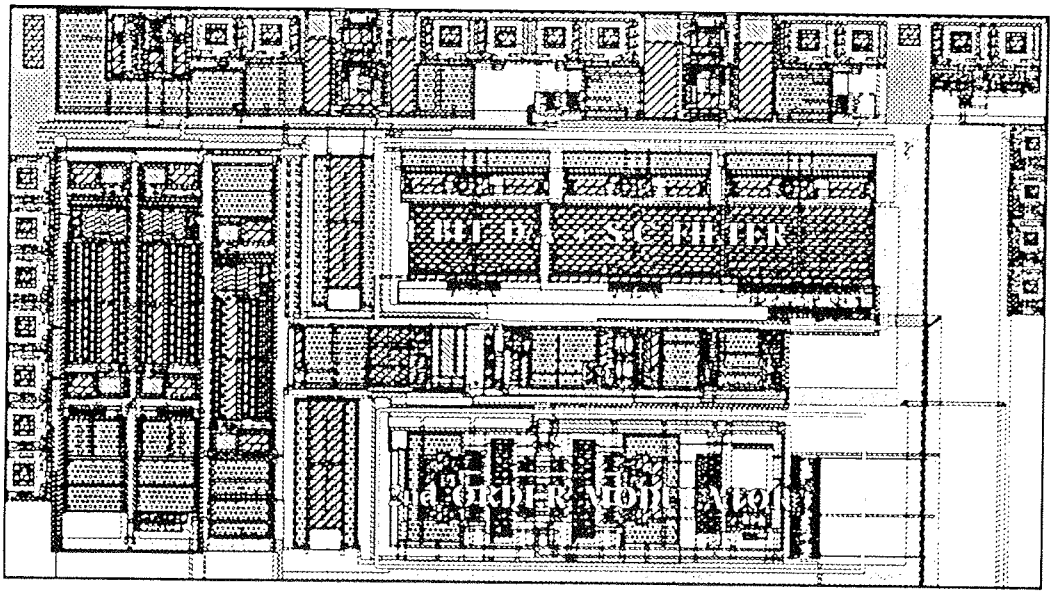

Figure 20: Layout of analog part of A/D and D/A converter

a good differential linearity. Measured results were not available at the time of publication of this article.

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