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SPIN-ON-GLASS PLANARIZATION OF DEVICE TOPOGRAPHY

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ABSTRACT: In this paper materials, methods, and processing of the spin-on- glasses (SOG) for planarization of wafer topography in integrated circuit fabrication are reviewed.

Postopki planarizacije s centrifugalnim nanašanjem siloksanskih stekel

KLJUČNE BESEDE: mikroelektronika, vezja integrirana, proizvodnja mikroploščic, planarizacija topografije, SOG spin-na-steklu, stekla siloksanska, nanašanje centrifugalno

POVZETEK: V preglednem članku so opisani materiali, metode in tehnološki postopki za centrifugalno nanašanje planarizacijskih plasti siloksanskih stekel v mikroelektronskih proizvodnih procesih.

1. Introduction

Device planarization, the reduction of distances between topography extremes in the direction normal to the wafer plane and the reduction of the side-wall slopes in order to facilitate subsequent processing steps, came into the technology forefront as lateral geometries began to shrink. Planarization is most critical during the final processing steps in IC fabrication, where metalization and dielectric layers are used. In double metal IC fabrication processes planarization is used primarily to enhance the step coverage of the top metal layer. Also, it is much easier to image fine line geometries on nearly planar surfaces and to etch lithographic patterns into a film if the resist does not cover severe topography /1,2/.

Flow of the dielectric film will smooth device topography if the temperature of the dielectric is raised to the point where the surface tension of the film becomes the dominant force acting on the film /2,3,4/. The temperature at which the flow occurs depends on the dopants included in the film (e.g. phosphorus and boron) and the details of the process, and lies between 500 deg C and 1000 deg C. This temperature range is acceptable for use of this planarization technique over conductors such as polysilicon and silicides, but too high for use over aluminum.

A common method of planarization is the etch-back process, where a thick dielectric layer (eg. 3 μm) is deposited over the first metal level, rounding its shoulders and filling the trenches between metal lines. The dielectric is then etched back to approximately 1 μm. Even though there are no temperature constraints associated with this process, planarization of topography over closely spaced lines may form a void at the bottom of the trench, causing severe problems during subsequent processing and with the reliability of the device. Variations of the technique (eg. using TEOS or APCVD instead of PECVD oxide) seem to overcome some of the problems mentioned above.

The sacrificial layer etch-back technique involves the deposition of a relatively thick layer with good planarizing properties (eg. photoresist, polyimide, spin-on-glass) over the dielectric. This layer is first smoothed and then etched untill none of it remains on the wafer. If the etch rates of the sacrificial film and the underlying dielectric are the same, or in plasma etching, if the ratio of the etch rates for both films is selected to take account of the microloading effects, the smoothed top surface of the sacrificial layer will be transfered to the dielectric. This technique, though relatively simple in principle, is very demanding regarding maintaining the proper etch rates, with all the complications associated with plasma etching of polimer films. In planarizing trenches with high aspect ratios (trenches deep relative to their widths) there may remain some of the sacrificial material in them, which can not be allowed with polymer sacrificial film and may be undesirable with spin-on-glass.

There are now available several materials that find application as planarization layers either by replacing dielectric films or being used over a thin dielectric film.

Such materials are polyimide and non-etch-back spin-on-glass, and their use is based on the planarization effect of a spun-on film of low viscosity.

In this paper planarization techniques utilising a spin-on-glass sacrificial layer are reviewed and described in some detail.

2. Spin-on-glass material

Spin-on-glass planarization techniques combine the planarization effect on spun-on films with the oxide-like material characteristics on SOG, resulting in simple and straightforward processing /5/. As a dielectric layer in multilevel interconnection structures, SOG films offer the following advantageous properties:

- high thermal/oxidative stability,
- etch characteristics similar to those of CVD oxides,
- good adhesion to silicon, oxides, aluminium, etc,
- can be doped,
- low trace metal contamination levels.

Thus, SOG materials are compatible with materials and processes of the IC fabrication technology, and SOG processes are easily integrated into existing process flows.

Spin-on glass liquids consist of Si-O chain polymers dissolved in commmon organic solvents, such as alcohols, ketones, and esters. The polymers are prepared through the same basic chemistry as that employed in sol-gel technology. Commercially available SOG materials are of four major types, listed in Table 1.

Polymer	Film Composition
Silicate	(SiO_2)
Phosphosilicate	$(SiP_xO_y)n$
Siloxane	$(R_xSiO_y)_n$
Phosphosiloxane	$(R_xSiP_yO_z)_n$

Table 1. Types of SOG materials

The nature of the siloxane or silicate polymer is determined by the reaction conditions, such as molar ratio of H_2O to polymer, pH, concentration of the solution, etc. Unlike sol-gel technology in which the goal is to form dense gels quickly, the reaction conditions in SOG synthesis are chosen such, that the polymers are stable toward molecular weight increase for periods of several months. Since gelation time is a strong function of concentration, the equivalent silica (SiO_2) content of most commercial SOG products is typically 10 percent or less. Therefore the SOG film thickness is usually limited to a few hundred nanometers.

The properties of ther SOG materials can be modified by incorporating a substituted alkoxysilane with methyl or phenyl radical, or a dopant such as phosphorus or boron, during the hydrolysis reaction.

The material characteristics of SOG films are fundamentally similar to those of sol-gel glasses. However, there are two important distinctions:

1. The first one stems from the fact that a SOG film is always formed on a substrate toward which it exhibits good adhesion. When such a film is dried and cured, shrinkage can occur only in the direction perpendicular to the substrate plane, since the film is constrained to remain adhered to the surface. This results in buildup of tensile stress paralel to the surface. Consequently, SOG films have a propensity for cracking, and the spin-on process has to take account of it. This tendency for cracking is somewhat reduced by organic groups introduced into the SOG polymer.

A study /6/ shows, that the tensile stresses in SOG films are below 10^9 dyne/cm^2. Due to the film shrinkage, the tensile stress after a 450° C bake is higher than the stress in a film baked at 200°C. Higher annealing temperatures are required to rearrange the bond angles to relieve the stress. After 920°C annealing, the thermal stress overcomes the tensile stress, resulting in a compressive film, after cooling it to room temperature. Oxygen annealing gives a lower stress than nitrogen annealing, but the reduction is very limited.

2. In IC fabrication the maximum temperature at which a SOG film can be cured is often limited to 450°C because of the presence of aluminum interconnects. After such low temperature cures the SOG film is far from being completely densified and contains significant amounts of silanols, ≡Si-OH, and adsorbed water. If the SOG film can be densified at high temperature, typically at 800°C to 900°C, a silanol- and water-free film is obtained, as demonstrated by IR spectroscopy /5/. The elimination of the silanols and water from SOG films after the high temperature cure is accompanied by a drop in the wet etch (HF) rate of the film to that of thermal SiO_2, implying complete densification. However, complete loss of water and silanol after a high-temperature cure does not guarantee complete densification, and the actual extent varies - particularely among siloxane-type SOG films.

Thickness measurements and other observations indicate that the SOG, as deposited and dried, is somewhat porous and one of the effects of subsequent processing is to reduce the porosity. Experiments suggest /7/ that the porosity is not completely removed by high temperature (900°C) processing. Cured SOG films placed in high vacuum and heated to approximately 500°C will desorb H_2O, a process which takes about 250 sec. After desorption the films can be refilled by placing them close to an open beaker of water for 12 hours. This suggests that the desorption is due to water coming out of pores in the SOG, rather than from reaction by-products. The source of the H_2O that is desorbed is simply ordinary ambient air.

The dielectric properties of a cured SOG film are, to a great extent, determined by its silanol and water content (8). For instance, the dielectric constants of silicate films after curing at 425°C and 900°C are found to be about 9 and 4, respectively. The high dielectric constant indicates the presence of a significant amount of polarisable meterial in these SOG films. This polarisable species is H_2O that is adsorbed into the microporous structure of the SOG film. Due to reversible adsorbtion/desorbtion of H_2O variations in the dielectric constant value occur. The dielectric properties of the films densified at 800°C become quite comparable to those of thermal SiO_2. It is interesting to note thet the dielectric constant of the densified SOG film, i.e. 4.2, is somewhat lower than that of a densified CVD SiO_2 film /9/.

The resistivity of the SOG film, which has a low value that can be compared to that of thermal SiO_2, is attributed to ionic, specifically proton conductivity.

Physical properties of the two examples of the SOG materials, Allied Chemicals Accuglass series 204, and 211 are listed in Table 2.

product	Accuglass 204	Accuglass 211
product type	phenylsiloxane	metilsiloxane
silanol/water content[1]	high	negligible
dielectric constant[2]	9 - 10	< 5
thermal stability	excellent	good
film shrinkage[3], %	10 - 12	8 - 10
resistance to cracking	medium	high
thickness uniformity, %	< 2	
film density, g/cc	2,1 ± 0.1	
resistivity, Ωcm	10^{12} (400° cure)	
breakdown field, V/cm	10^6	
refractive index	1,43 ± 0.01	
pinhole density, 1/cm^2	< 1	
particulate density, 1/cm^2	< 1	

1. after 350° cure
2. after 400° cure
3. between 150°C/60 s bake and 425°C/60 min cure

Table 2. Physical properties of SOG material

3. Planarization

Processing techniques for SOG planarization are basically similar to what is being used in IC processing; while the deposition and curing of SOG are analogous to photoresist processing, the etching of SOG films closely resembles the methods employed for etching CVD oxyde film. However, the most common types of problems encountered in the use of SOG films, particulate contamination, cracking of dielectric layer, poor adhesion, are associated with the deposition and curing of the SOG films, and special spin-on techniques and equipment are used to eliminate them. Spin-on coaters designed specifically for SOG are available commercially.

SOG planarizaton layers have been successfully used in multilayer interconnection processing. Etch-back processes in which most of the SOG layer coated over a CVD dielectric layer is etched away, leaving only a small amount of the SOG meterial in the crevices between metal lines, are firmly established. Conversely, non-etch-back SOG planarization techniques have become more common only recently.

The limited film thickness of the available SOG materials, though not sufficient to allow their use as a stand-alone intermetal dielectric layer, is adequate for planarizing or smoothing a wide range of substrate topographies. The effect of a thin, 3,000 A SOG film on the step (space) profiles at two different structure densities is shown in conceptual illustration, Figure 1.

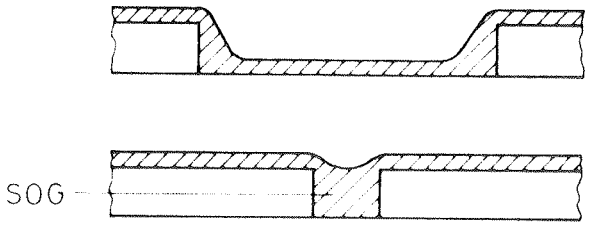

Fig. 1: Conceptual illustration of smoothing and planarization by a thin, 3000 A SOG film deposited over sparse (top) and dense (bottom) structure.

Detailed descriptions of the planarization properties of the spun-on thin films, as important as they are for the integrated circuit processing, are simply not available because of the complexity of the phenomena encountered. One of the most difficult aspects is the effect that the surrounding topography has on planarization. Change in the position, size of topological features, and chemical nature of the underlying films can change the polymer film thickness on adjacent features. To calculate SOG planarization properties from first principles is a difficult rheological problem that has not yet been solved. However, a semi-empirical approach to simulate the spun-on film planarization properties is available /10/ in which the spun-on film is considered to be a low-pass filter for the topography. There is also an extensive literature in which planarizing properties of the SOG films are treated exprimentally /5, 6, 11/. Based on this a qualitative picture of the SOG planarization process, as described below, can be established.

Very little planarization, defined as percent reduction in step height, is obtained over isolated lines or lines separated by 3 to 4 μm wide spaces. However, the 90

degree angle of steps is reduced to about 45 to 60 degrees. This smoothing of the vertical-walled features is quite suitable for conformal deposition of subsequent layers with a high degree of step coverage. At smaller geometries, where the aspect ratio of the space between lines approaches unity, a high degree of planarization is produced by similarly thin SOG films. At such geometries, a mere smoothing effect would not be acceptable. In either case the SOG thickness above the lines is too small to provide interlevel insulation (Figure 2).

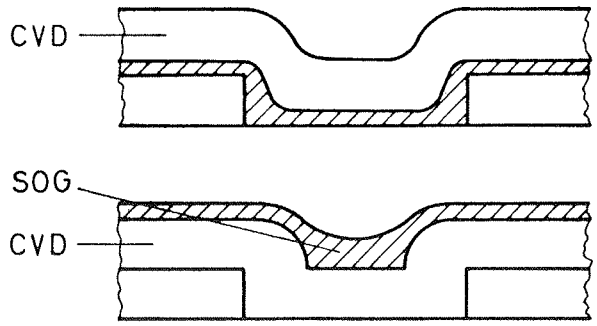

Fig. 2: Two-layer CVD / SOG dielectric structure.

Thus, the SOG planarization processes in use today employ SOG films primarily as a planarizing agent, with the bulk of the dielectric insulation functions provided by the CVD oxide layers. In some schemes, SOG films are used as a sacrificial planarization layer. Four of the more common schemes for planarization with SOG are /11, 12, 13, 14, 15, 16, 17/:

i) CVD / SOG two-layer dielectric
ii) CVD / SOG / CVD sandwich dielectric
iii) Partial etch-back of SOG in a sandwich structure
iv) Total etch-back of SOG

The two layer CVD / SOG dielectric structure shown schematically in Figure 2 is the simplest process of the four. Since the SOG layer is in direct contact with the interconnects in these structures, the SOG must exhibit very good dielectric characteristics. At polysilicon level, this can be ensured by carrying out a high temperature (800° to 900°C) cure of the SOG film, but the structure can not be used as an intermetal dielectric because of the problems associated with the possible chemical reaction between the metal layer and the H_2O emanating from the SOG layer. The order in which the SOG and CVD layers are deposited is a function of the geometry, and the nature of the underlying dielectric layer. In MOS IC fabrication the use of a phosphorus containing SOG material is common for Na^+ gettering purposes.

The use of a CVD / SOG / CVD sandwich structure, illustrated in Figure 3, relaxes the requirements on the dielectric properties of the SOG layer. Moreover, the bottom CVD layer serves to buffer the SOG from the effect of the relatively large thermal expansion of aluminum lines during thermal processing, and, vice versa, protects the aluminum lines from the the oxidizing effects of the SOG. Under certain conditions, as will be discussed later, the presence of the SOG within the via holes etched through the composite dielectric is a potential cause of high via contact resistance. In the partial etch-back sandwich process, shown in Figure 4, the problem is avoided by etching back the SOG layer to a point where it clears the top of the interconnect lines.

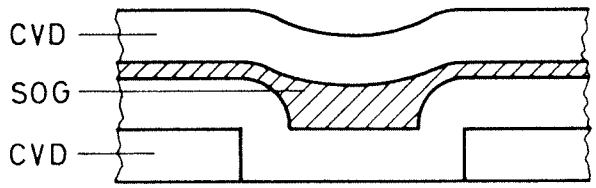

Fig. 3: CVD / SOG / CVD sandwich structure.

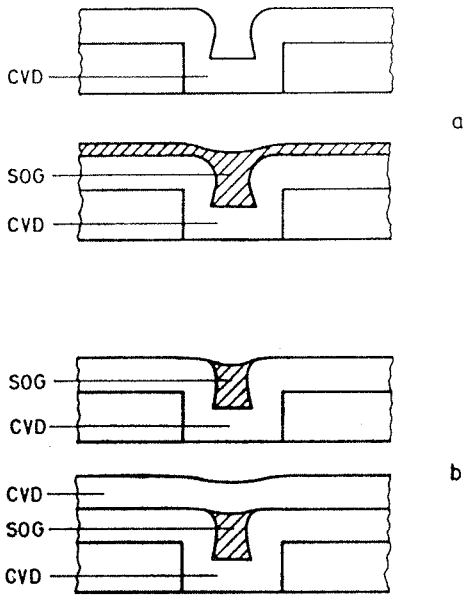

Fig. 4: SOG partial etch-back process; before plasma etching (a), after plasma etching and second CVD oxide deposition (b).

The process is particularly useful at very small geometries, where it is difficult to fill the narrow spaces with SOG material without cracking, or void formation. In such cases a SOG material with low shrinkage characteristics is necessary. The partial etch-back approach allows the use of such a material regardless of its effect on the via contact resistance.

The SOG etch-back process is a sacrificial layer etch-back technique. The use of a SOG as the sacrificial planarization layer offers several advantages compared to, e.g. a resist layer, particularly in the etching step. The etch rates of CVD oxide and SOG are easily matched through simple adjustments of the plasma chemistry. The process control is greatly improved as the plasma loading effects are minimized and the etch chamber is free from organic residues and deposits. The thinner SOG planarization layer does not accumulate excessively in low-lying areas of the chip, thus minimizing via depth variations in the planarized dielectric layer.

The selection of an optimal SOG material and planarization scheme in a given application is dictated by a number of factors including: device geometry, nature of the underlying interconnect, post planarization thermal processes, sensitivity of the device to mobile ion contamination, conformality of the CVD process, and thermal budget available for the SOG cure.

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