UDK 621.3:(53+54+621+66), ISSN0352-9045 Informacije MIDEM 24(1994)1, Ljubljana

COMPARISON OF DIFFERENT MOSFET THRESHOLD VOLTAGE DEFINITIONS*

Prepared from the paper presented on the Symposium MEET '93 (MIPRO), Opatija, May 1993.

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Key words: semiconductors, MOSFET transistors, threshold voltage, theoretical analysis, Poisson's equation, strong inversion, weak inversion, response characteristics

Abstract: Theoretically MOSFET threshold voltage is defined with the surface inversion and can be calculated using the MOS structure technological data. Device current-voltage characteristics are used to define threshold voltage in practice. In this paper both definitions are described and the connection between them has been determined in the example of real MOS structure.

Usporedba različitih definicija napona praga MOSFET-a

Pripremljeno prema referatu prezentiranom na Savjetovanju MEET '93 (MIPRO), Opatija, Svibanj 1993.

Ključne besede: polprevodniki, MOSFET transistorji, napetost pragovna, analiza teoretična, Poisson enačba, inverzija močna, inverzija šibka, karakteristike odzivne

Sažetak: Teorijski se napon praga MOSFET-a definira inverzijom površine silicija i može se računati iz poznatih tehnoloških podataka MOS strukture. U praksi se napon praga određuje iz strujno-naponskih karakteristika elementa. U radu su opisane obje definicije napona praga i određena je njihova veza na primjeru realne MOS strukture.

1. INTRODUCTION

Electrical characteristics of integrated circuits can be designed by fitting the individual electronic devices' parameters. One of the most important parameters, in MOS integrated circuits' design, is MOSFET threshold voltage U_{GS0}. Theoretical analysis of MOS structure determines the threshold voltage U^t_{GS0}. As the operation of integrated circuits is defined with the threshold voltage U^c_{GS0} obtained from the MOSFET current-voltage characteristics, connection of this parameter with the value of theoretically calculated threshold voltage U^t_{GS0} is needed. Both threshold voltage definitions are compared in this paper in the example of n-channel MOSFET.

2. THEORETICAL CALCULATION OF THRESHOLD VOLTAGE

Figure 1 shows the cross-section of the n-channel MOSFET. The device substrate (B) is a p-type silicon. The MOS structure, between two n^+ regions of source (S) and drain (D), consists of silicon substrate, thin silicon oxide layer (SiO_2) and the gate (G) material. For MOSFET operation, silicon surface under the oxide layer must be inverted and n-channel between source and drain must be formed. This is obtained electrically, by connection the voltage U_{GS} between gate and source. The voltage U_{GS} needed for surface inversion is the threshold voltage U_{GS0}.

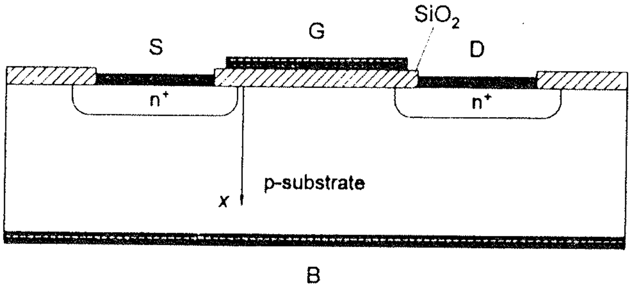

Fig. 1: *Cross-section of n-channel MOSFET*

Before channel formation, voltage U_{GS} decreases majority concentration of holes on the substrate surface,

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* This paper is part of the scientific project "2-07-266 Electronics and Microelectronics" supported by "Ministry for Science" of the Republic of Croatia.

producing the thin depletion layer under the oxide. Potential distribution in the depletion layer, along the x coordinate perpendicular to the substrate surface (Fig. 1), determines the Poisson's equation /1/

$$\frac{d^2u}{dx^2} = \frac{q}{\varepsilon_{Si} \cdot U_T}(n - p - N), \tag{1}$$

where u is the normalized electrostatic potential ψ, $u = \psi/U_T$, n, p and N are electron, hole and net doping concentrations, q is the elementary charge, ε_{Si} is the silicon permittivity and U_T is the thermal voltage. If Fermi potential is chosen as reference potential, $\varphi = 0$, then in the case of low injection the majority hole concentration is

$$p = n_i \cdot exp\ (-\ u). \tag{2}$$

The minority electron concentration n is changed with the external potential /2/

$$n = n_i \cdot exp\ (u + u_V). \tag{3}$$

At the source end of the channel, normalized external potential u_V is the result of the voltage U_{BS} applied between bulk and source, $u_V = U_{BS}/U_T$. In the previous equations n_i is the intrinsic carrier concentration.

Generally, net doping concentration N is the difference between donor N_D and acceptor N_A concentration and corresponds to the difference between equilibrium carrier concentrations of electrons n_b and holes p_b in the bulk, far from the surface

$$N = N_D - N_A = n_b - p_b = n_i \cdot exp(u_b) - n_i \cdot exp\ (-u_b). \tag{4}$$

The doping concentration in the substrate of the n-channel MOSFET with homogeneously doped channel is acceptor concentration $N = -\ N_{AB}$, and this concentration is equal to the bulk majority hole concentration p_b. According to (4), normalized bulk potential is

$$u_b = -\ln\left(\frac{N_{AB}}{n_i}\right). \tag{5}$$

Depletion layer surface charge per unit area Q_{SD} is defined with Gauss's law

$$Q_{SD} = -\varepsilon_{Si} \cdot U_T\left(\frac{d\,u}{d\,x}\right)\Bigg|_s, \tag{6}$$

where index s designates the silicon surface. Integration of Poisson's equation (1) yields

$$\begin{aligned} Q_{SD} = -\sqrt{2 \cdot q \cdot \varepsilon_{Si} \cdot U_T \cdot n_i} \cdot \Big[&\exp\left(u_s + u_V\right) - \\ &- \exp\left(u_b + u_V\right) - \exp\left(-u_s\right) - \exp\left(-u_b\right) - \\ &- 2 \cdot \left(u_s - u_b\right) \cdot sh\left(u_b\right)\Big]^{1/2}. \end{aligned} \tag{7}$$

The voltage U_{GS} is the result of potential distributions in the MOS structure,

$$U_{GS} = -\frac{Q_{SS} + Q_{SD}}{C'_{ax}} + \psi_s + \Delta\psi + U_{BS}. \tag{8}$$

In (8) Q_{SS} is the fixed surface charge per unit area in the oxide layer, and ψ_s is the surface potential, $\psi_s = u_s \cdot U_T$. The term $\Delta\psi = \phi_{MS} - \psi_b$ includes the work-function difference between gate and bulk ϕ_{MS} and the bulk potential $\psi_b = u_b \cdot U_T$. C'_{ox} is the oxide capacitance per unit area, $C'_{ox} = \varepsilon_{ox} / t_{ox}$, where ε_{ox} is the permittivity of SiO_2 and t_{ox} is the oxide layer thickness.

Theoretically, the threshold voltage U^t_{GS0} is defined as the voltage U_{GS} that produces surface minority electron concentration equal to the bulk majority hole concentration, $n_s = p_b$. That is the case of strong inversion. The values of surface potentials $u_s = u_{s0} = -\ u_b - u_V$ and $\psi_s = \psi_{s0} = -\psi_b - U_{BS}$ included in (7) and (8), define the surface charge Q_{SD0} and the threshold voltage U^t_{GS0}.

Surface inversion begins when surface minority electron concentration reaches the intrinsic carrier concentration, $n_s = n_i$. This case of weak inversion determines the surface potentials and $u_s = u_{si} = -u_V$, and $\psi_s = \psi_{si} = -U_{BS}$, corresponding charge Q_{SDi} and voltage U^t_{GSi} are obtained from (7) and (8).

3. THE THRESHOLD VOLTAGE FROM CURRENT-VOLTAGE CHARACTERISTICS

In practice, the threshold voltage U^c_{GS0} is determined from the MOSFET current-voltage characteristic. The voltage U^c_{GS0} is defined as the voltage U_{GS} that breaks the flow of drain current I_D and can be read easiest from the MOSFET transfer characteristic $I_D = f(U_{GS})|U_{DS}$. The problem is that the current I_D flow break is the continuous change and does not appear sharp at voltage $U_{GS} = U_{GS0}$. Namely, in subthreshold region, for voltages $U_{GS} < U_{GS0}$, there is a finite current I_D flow between source and drain that decreases exponentially with the voltage U_{GS}. Because of that the threshold voltage U^c_{GS0} is determined graphically, from extrapolation of the transfer characteristic and the coordinate with $I_D = 0$ /3/.

If the MOSFET operates in linear region, for voltages $U_{DS} \leq U_{GS} - U_{GS0}$, the drain current is

$$I_D = K \cdot \left(U_{GS} - U_{GS0} - \frac{U_{DS}}{2}\right) \cdot U_{DS}, \tag{9}$$

where K is the proportionality constant. At small voltages U_{DS}, the term $U_{DS}/2$ can be neglected. The current I_D changes linearly with voltage U_{GS}, and the transfer characteristic $I_D = f\ (U_{GS})|U_{DS}$ is the line.

In saturation region, for voltages $U_{DS} \leq U_{GS} - U_{GS0}$, the current is

$$I_D = \frac{K}{2} \cdot \left(U_{GS} = U_{GS0}\right)^2, \tag{10}$$

and the transfer characteristic $I_D = f(U_{GS})|U_{DS}$ is the parabola.

4. THE RESULTS OF CALCULATIONS

The comparison of two different definitions of the threshold voltage has been performed on the example of n-channel MOSFET. The homogeneously doped MOS structure, with the substrate acceptor concentration $N_{AB} = 10^{15}$ cm^{-3} and the oxide thickness $t_{ox} = 0{,}1$ μm, has been chosen. The oxide layer charge $Q_{SS} = 5 \cdot 10^{10}$ cm^{-2} and n-type oxide polysilicon layer have been supposed. Besides for those parameters, the threshold voltage has been calculated as the function of the concentration N_{AB}, the oxide thickness t_{ox}, and the bulk voltage U_{BS}.

The two values of threshold voltage have been determined with the theoretical approach: U^t_{GSO} for strong inversion and U^t_{GSi} for weak inversion. Current-voltage characteristics have been calculated numerically, using the MINIMOS device simulator /4/. The MOSFET with described MOS structure, and with the sufficiently large channel dimensions (the length $L = 10$ μm and the width $W = 10$ μm) has been analyzed to avoid short and narrow channel effects. The definition of the threshold voltage U^c_{GSO}, for the chosen parameters of MOS structure, is represented in Fig. 2a and 2b. Fig. 2a shows the transfer characteristics in linear region, calculated for small voltage $U_{DS} = 50$ mV. The transfer characteristic in saturation region (Fig. 2b) has been determined for voltage $U_{DS} = 5$ V. In order to maintain the linear relationship, as in the linear region, the square root of the current I_D, versus the voltage U_{GS}, has been drawn in Fig. 2b. In both Figures the straight line has been pulled through the MINIMOS data minimizing the root mean square error. The threshold voltage U^c_{GSO} has been determined by extrapolation of transfer characteristics to the current value $I_D = 0$.

The results of threshold voltage calculations, as the function of several technological and electrical quantities, are represented in Figures 3-5. According to Figure 3, the threshold voltage U_{GSO} increases with the substrate concentration N_{AB}. In the bulk the equilibrium majority hole concentration p_b increases and the equilibrium minority electron concentration n_b decreases with increase of concentration N_{AB}, so higher voltage U_{GS} is needed to equalize the surface electron concentration n_s with the hole concentration p_b. The enlargement of the oxide layer thickness t_{ox} increases, according to Figure 4, the threshold voltage U_{GSO}. The thicker oxide reduces the effectiveness of the gate electrode. The results of threshold voltage change with the bulk voltage U_{BS} are shown in Figure 5. As the higher voltage U_{BS} decreases the electron concentration n_b, the higher voltage U_{GS} is needed for channel inversion.

In all three Figures 3-5 the results of theoretical calculations U^t_{GSO} and U^t_{GSi} are compared with the voltages U^c_{GSO} obtained from current-voltage characteristics. As the smaller voltage U_{GS} is needed to increase the sur-

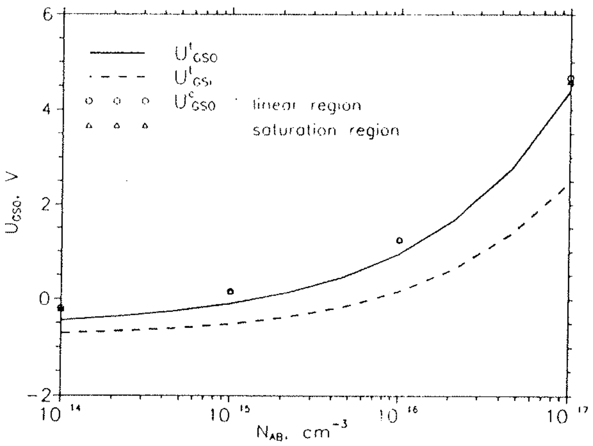
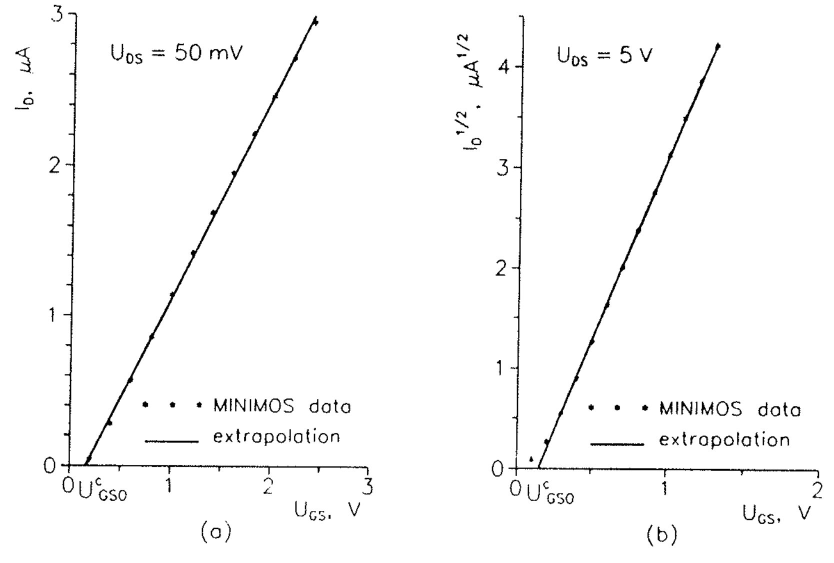


Fig. 3: Threshold voltage U_{GSO} versus bulk acceptor concentration N_{AB}



(a) (b)

Fig. 2: MOSFET transfer characteristics: (a) in linear region, (b) in saturation region. MOS parameters are: $N_{AB} = 10^{15}$ cm^{-3}, $t_{ox} = 0{,}1$ μm and $U_{BS} = 0$V.

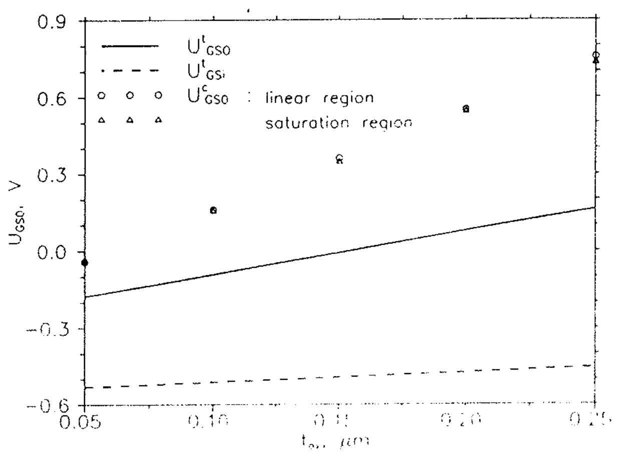


Fig. 4: *Threshold voltage U_{GS0} versus oxide thickness t_{ox}*

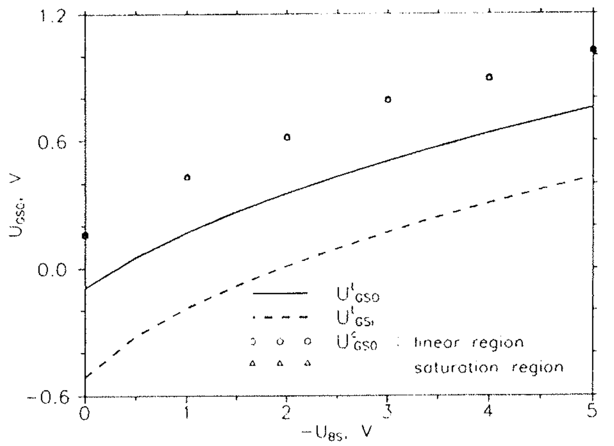


Fig. 5: *Threshold voltage U_{GS0} versus bulk voltage U_{BS}*

face electron concentration n_s to the value of intrinsic concentration n_i, than to the equilibrium hole concentration p_b, the theoretical threshold voltages U^t_{GS0} in weak inversion are lower than the threshold voltages U^t_{GS0} in strong inversion. The voltages U^c_{GS0} agree mutually regardless as they are obtained from transfer characteristics in linear or in saturation region. Also the voltages U^c_{GS0} show the better agreement with the values of the theoretical voltages U^t_{GS0} in strong inversion.

In Fig. 3 and Fig. 5 the voltages U^c_{GS0} are higher than the voltages U^t_{GS0} for practical the same value of 0,24 V. On the other hand, the voltage difference $U^c_{GS0} - U^t_{GS0}$ in Figure 4 changes proportionally with the oxide thickness t_{ox}. The obtained values of voltages U^c_{GS0} can be calculated theoretically, including the correction factor

$$U^c_{GS0} = U^t_{GS0} + k \cdot t_{ox} = -\frac{Q_{SS} + Q_{SD0}}{C'_{ox}} - \psi_b + \Delta\psi + k \cdot t_{ox}, \qquad (11)$$

with the constant $k = 2{,}4$ V / μm.

5. CONCLUSION

The threshold voltage values U^t_{GS0} from theoretical analysis of MOS structure and U^c_{GS0} from current-voltage characteristics have been compared for typical example of n-channel MOSFET. The changes of threshold voltage U_{GS0} with basic technological and electrical quantities have been determined. Although the voltages U^t_{GS0} and U^c_{GS0} have been calculated for the same structure and with the application of the equal physical constants, the difference between the values U^t_{GS0} and U^c_{GS0} has been observed, and the dependence of the difference on the oxide layer thickness t_{ox} is described with the equation (11). The obtained relation is useful, because the threshold voltage can be technologically adjusted in accordance with the results. U^t_{GS0} from theoretical analysis, and the value U^c_{GS0} from current-voltage characteristics is essential for circuit application. More different examples must be analyzed to prove the generality of the equation (11).

REFERENCES

/1/ P. Biljanović: "Mikroelektronika - integrirani elektronički sklopovi", Školska knjiga, Zagreb, 1983.

/2/ S.M. Sze: "Physics of Semiconductor Devices" John Willey, New York, 1981.

/3/ P. Antognetti, G. Massobrio: "Semiconductor Device Modeling with SPICE" McGraw-Hill, New York, 1988.

/4/ S. Selberherr, A. Schötz, H. Pützl: "Two Dimensional MOS-Transistor Modeling" in: P. Antognetti, D. A. Antoniadis, R. W. Dutton, W. G. Oldham: "Process and Device Simulation for MOS-VLSI Circuits", Martinus Nijhoff, The Hague, 1983.

Prispelo (Arrived): 21.07.93 ***Sprejeto (Accepted): 01.02.94***

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