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DEVICE MODELING AT LOW TEMPERATURES

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Keywords: semiconductor devices, device modeling, semiconductor resistors, junction diodes, MOS capacitors, low temperatures, evaluation of results, calculation results, measurement results, testing results, comparison of results

Abstract: Device modeling at low temperatures is performed for several basic semiconductor devices (resistors, PN diodes, MOS capacitors). For the purpose of validation of calculated results, test structures were fabricated and characterized. The comparison of measured and calculated results indicates certain disagreement at low temperatures (< 30K).

Modeliranje elementov pri nizkih temperaturah

Ključne besede: naprave polprevodniške, modeliranje elementov, upori polprevodniški, diode junction, MOS kondenzatorji, temperature nizke, vrednotenje rezultatov, rezultati izračuna, rezultati meritev, rezultati preskušanja, primerjava rezultatov

Povzetek: V prispevku je predstavljeno modeliranje elementov pri nizkih temperaturah za nekatere osnovne polprevodniške strukture (upori, PN dioda, MOS kondenzatorji). Izračunani rezultati so bili preverjeni z meritvami na izdelanih testnih strukturah. Primerjava izmerjenih in izračunanih rezultatov kaže na določeno odstopanje v področju nizkih temperatur (< 30 K).

I. INTRODUCTION

Low temperature operation of semiconductor devices is gaining more and more attention in the semiconductor community. This is the consequence of several improved material properties at low temperatures that are crucial for the forthcoming solid state circuits with scaled-up complexity and performance.

At low temperatures, reduced carrier scattering results in higher carrier mobility and consequently in faster circuits. Better thermal conductivity allows greater power dissipation and therefore higher packing density and complexity. Degradation processes are scaled down many orders of magnitude leading to improved reliability and higher circuit complexity. Integration with superconducting structures is a challenge.

Excellent review papers were published recently /1,2/ giving insight into the important effects that determine device properties at low temperatures. Incomplete impurity ionization at low temperatures is still a demanding problem, especially in the case of high doping /3-8/. Carrier mobility variation with temperature is important effect for accurate modeling /9-12/. Several carrier generation-recombination effects, not very influent at room temperatures, should be taken into account at low temperatures to explain device behavior /13-16/. Internal barrier effects appearing at low temperatures are becoming important /17/. Selfheating effects can explain anomalies in electrical characteristics /18/.

In this work, the possibilities for device modeling at low temperatures were studied. For this purpose, basic test structures (resistors, junction diodes, MOS capacitors) were fabricated and measured from room temperatures to 20K. Device modeling was performed with device simulator MEDICI1.1 and process modeling with process simulator SUPREM3, both provided by TMA. Calculated results are compared with measurements and discussed.

II. RESISTORS

Resistors are interesting semiconductor devices for low temperature studies because they are relatively simple devices (Fig.1), revealing therefore clearly the important effects such as temperature dependence of mobility and impurity freeze-out.

Experimental. To study low temperature effects test resistors with three different doping levels were fabricated, measured and modeled: low-concentration (l_c) resistors, transition- concentration (t_c) resistors and high-concentration (h_c) resistors. Resistor impurity profiles are shown in Fig.2.

Resistors with *lc* and *hc* profiles were made on P-Si substrate, <100>, 16Ωcm Boron doped. Low concentration N-type resistors (*lc*) were made by ion implantation (Phosphorus, Energy 180keV, Dose 2.0e12cm-2), followed by drive-in (T = 1150°C, t=15h, ambient O2 dry).

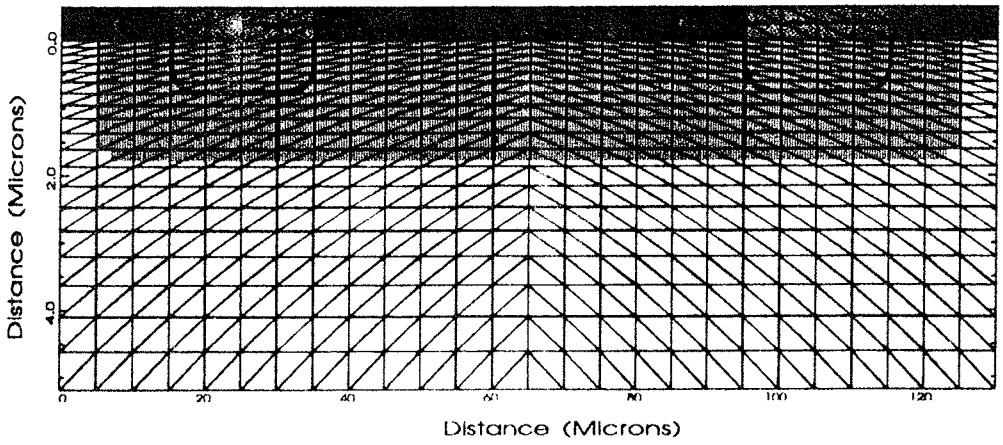

Fig. 1: Resistor structure and modeling grid

High concentration P-type resistors (h_c) were made into previously described l_c profile by an additional ion implantation (Boron, Energy 60keV, Dose 4.0e15cm-2), followed by drive-in (T = 975°C, t = 85min, ambient N2). Both profiles were measured by spreading resistance technique. The input profiles for device modeling, calculated and fitted by SUPREM3, are shown in Fig.2 as l_c and h_c profiles.

Transition-concentration P-type resistor (t_c) was made on N-type Si substrate, <100>, 10 Ωcm Phosphorus doped. Predeposition (BN975 solid diffusion source, T = 830°C, t=120min, ambient N2) was followed by drive-in (T = 1075°C, t = 120min, ambient O2 dry). The input profile for device modeling, obtained by SUPREM3 and fitted to the measurements (surface profile, sheet resistance), is shown on Fig.2 as t_c profile.

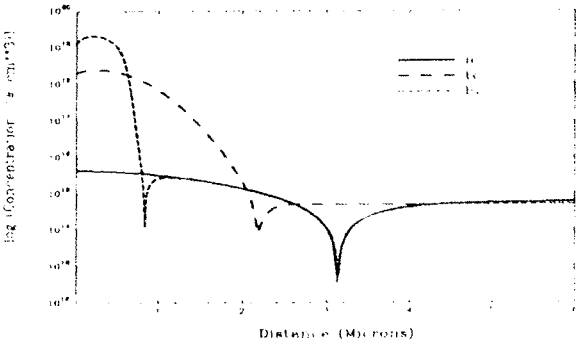

Fig. 2: Resistor impurity profiles

Mobility model. Resistance vs. temperature for different mobility models from room to low temperatures was calculated and compared with measured results (Fig.3). Different mobility models applied were /19/: concentration dependent mobility (CONMOB), analytical model introduced by Caughey and Thomas and improved by Selberherr (ANALYTIC), analytic model of Arora, et al. (ARORA), carrier- carrier scattering mobility model by Dorkel, et al. (CCSMOB), interface and bulk mobility model of Lombardi, et al. (LSMMOB), and Phu mobility model (PHUMOB).

The influence of different mobility models on the calculated resistance vs. temperature dependency can be observed from Fig.3. Variation of modeling results for different mobility models is considerable, illustrating the importance of good low temperature mobility model. It is concluded that the resistance variation with temperature (Fig.3) is best described with the model of Selberherr /20/, as shown separately in window on Fig.3a (scale unchanged). This mobility model will therefore be adopted for future calculations in this work.

Impurity freeze-out effect. The limitations of incomplete impurity ionization model is the next question of importance. Since the temperature dependency of incomplete ionization model directly influences the carrier freeze-out, it seems to be most important model for accurate device modeling at low temperatures. Therefore a brief description of possibilities for the incomplete impurity ionization modeling is given. Standard expressions for ionized impurity concentration ND^+, NA^- in the incomplete impurity ionization model are /19/

$$N_D^+ = \frac{N_D}{1 + GCB\exp\frac{E_{Fn} - E_D}{kT}} \quad (1)$$

$$N_A^- = \frac{N_D}{1 + GVB\exp\frac{E_A - E_{Fp}}{kT}} \quad (2)$$

where N_D, N_A are total donor and acceptor impurity concentrations, E_{Fn}, E_{Fp} Fermi electron and hole levels, E_D, E_A donor and acceptor energy levels, and GCB,GVB degeneracy factors for conduction and acceptor bands, respectively.

It is well known /3/ that (1) and (2) do not describe the deionization of impurities in the heavily doped regions correctly. Application of (1) in the heavily doped N^+

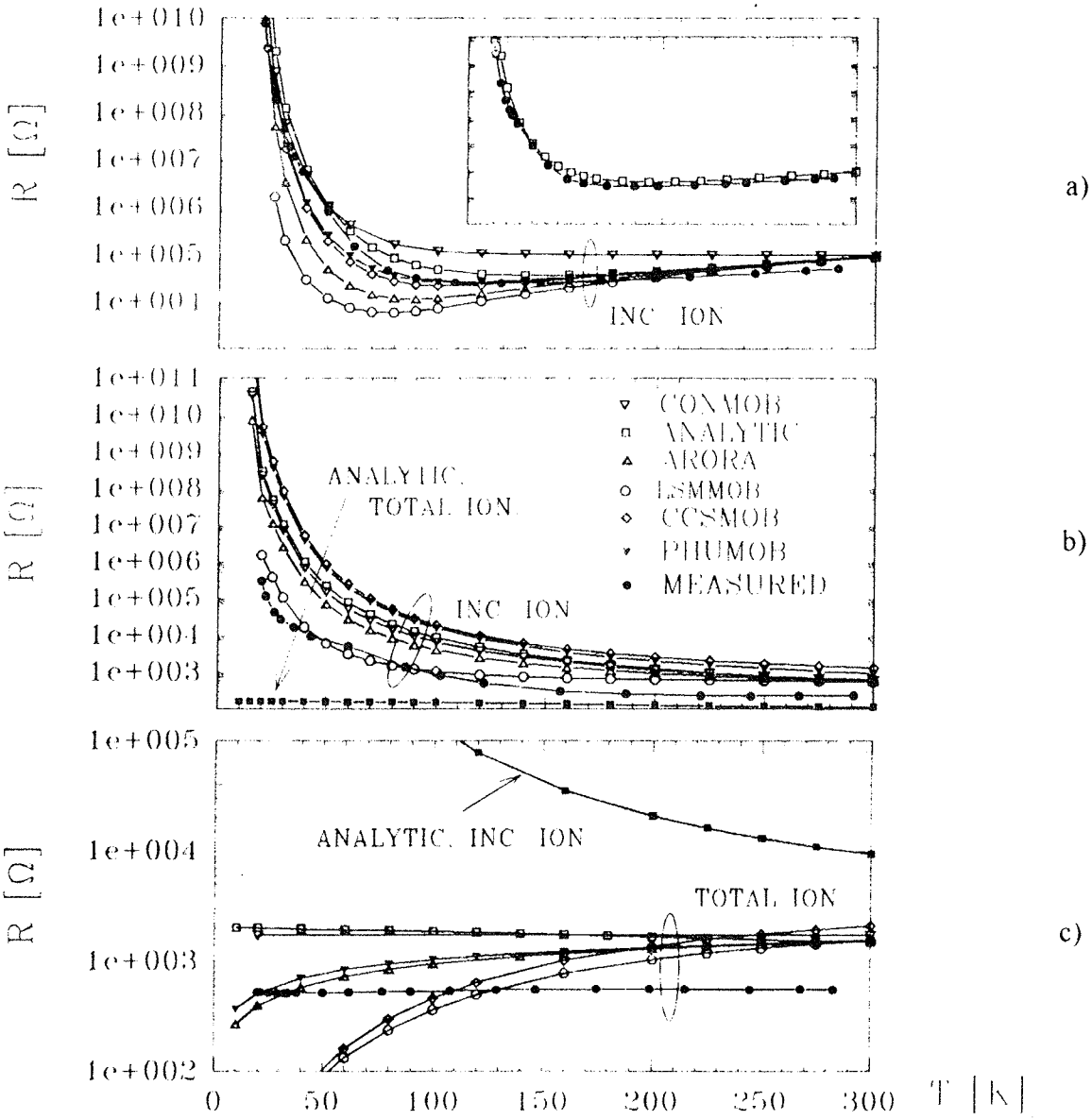

Fig. 3: Measured and calculated resistance vs. temperature for lc(a), tc(b) and hc(c) resistor

region modeling leads to significant discrepancies between actual N_{D+} and calculated ND+ /22/. Regions of lower doping concentration (< 1e18cm-3) can be described adequately with (1) and have therefore semiconductor nature of freeze-out. Regions of higher doping concentration (> 1e19cm-3) are metallic in nature, not revealing any impurity freeze-out even at low temperatures, and therefore are better described with the total ionization assumption /8,21/. Modeling in the transition region (1e18 - 1e19 cm-3) is not straightforward. Actual ND+ probably lies somewhere between ND+ as calculated by (1) and ND. By decreasing the temperature, the uncertainty of N_{D+} in the transition region even increases. Similar conclusions hold for P^+ regions. This model inadequacy results in inaccurate low temperature modeling of devices with dominant transition concentration region.

It can be seen from Fig.3 that for lower doping concentrations standard model for incomplete impurity ionization (1,2) performs well resulting in reasonable agreement between measured and modeled values (Fig.3a). For transition region of doping concentrations (1e18-1e19 cm-3), the model for incomplete impurity ionization (1,2) fails to give adequate results (Fig.3b). The model fails completely at high doping concentrations above 1e19cm-3 where the only possibility to get correspondence between measured and modeled results is to assume total impurity ionization (Fig.3c).

III. JUNCTION DIODES

Experimental. To study low temperature behavior of junction diodes, N^+P structures with impurity profile shown in Fig.4 were fabricated. Impurity predeposition step (BN975 solid diffusion source, T=930°C, t=40min, ambient N2) was followed by drive-in (T=850°C,

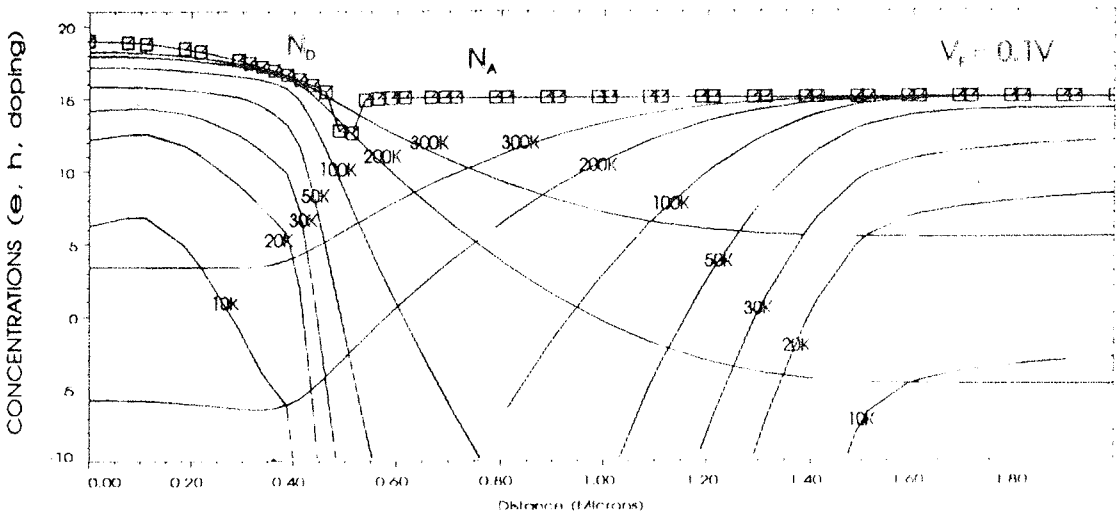

Fig. 4: Incomplete impurity ionization at low temperatures (freeze-out)

t=60min, ambient O2 dry). Input impurity profile for device modeling was obtained by SUPREM3 simulation fitted to measured values (junction depth, sheet resistivity, surface profile).

Modeling. Simulation of PN junction at low temperatures with standard ionization model (1) was performed. Calculated free carrier concentrations are shown on Fig.4. Strong carrier freeze- out effect calculated in highly doped region is unrealistic as described in ch.II. Therefore the device was divided into two regions: high concentration region (> 3.8e18cm-3) with total ionization assumption and low concentration region (< 3.8e18cm-3) where standard impurity ionization model (1) was preserved. Transition concentration between regions (3.8e18cm-3) suggested in /21/ was applied.

Resulting free carrier concentrations, based on regional impurity ionization approach, together with standard calculation result for comparison, are given in Fig.5. Regional approach gives more reasonable profiles and seems to be the best solution in absence of exact model for impurity ionization.

Forward I/V junction diode characteristics was measured and modeled from room to low temperatures (Fig.6). The correspondence is reasonable for higher temperature (> 50K) and lower current (< 1mA). The reason for disagreement at higher current, where ohmic drop due to the series resistance plays most important role, is probably in inaccurate modeling of series resistance. This is the consequence of simplifications related to the front contact topology of the device, influencing accurate modeling of series resistance significantly.

Disagreement at low temperatures (< 50K) seems to arise from the underestimated carrier concentration calculated by simulator. This leads to the necessity for the improvement of incomplete ionization model or for the addition of other carrier generation models at such low temperatures /16/.

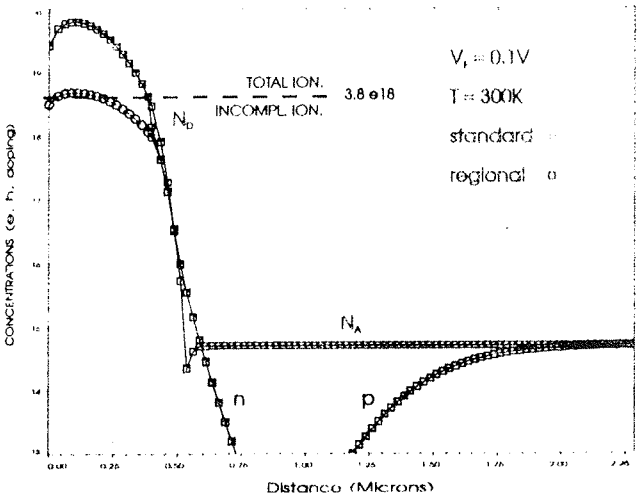

Fig. 5: Incomplete impurity ionization (regional approach)

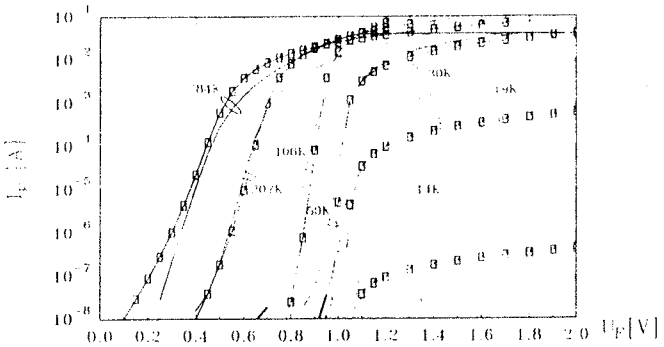

Fig. 6. PN diode forward IV characteristics (measured,modeled)

IV. MOS CAPACITORS

Experimental. Test MOS capacitors (tox=96nm) were fabricated on P-type 16Ωcm Si substrate. Necessity for front contacting of the bulk region led to high series resistance of the bulk even at room temperatures. High frequency (1MHz) CV plots were measured by HP 4280A C meter. Even at temperatures not much bellow 300K true high frequency CV curves could not be obtained due to the extremely slow formation of inversion layer under the gate. Therefore, deep depletion (DD) curves were measured even at slow sweep rate (< 0.1 V/s).

Modeling. Modeling DD CV plots with Medici is not possible since AC analysis cannot be performed in conjunction with transient analysis. Therefore direct comparison of whole calculated and measured curves is not possible as well. Measured and calculated capacitance and conductance in strong accumulation as a function of temperature are presented in Fig.7. Incomplete ionization model (2) and ANALYTIC mobility model /19/ were applied for the simulation. Since the temperature dependence of bulk series resistance is a dominant mechanism that affects capacitance and conductance of the sample /23/, reasonable agreement between calculated and measured curves is obtained.

Another comparison between experiment and simulation is related to the majority carrier freeze-out at the edge of depletion region. In order to determine the majority carrier concentration at the edge of depletion region, $1/C^2$ curves with slope directly proportional to the majority carrier concentration /24/ were plotted for different temperatures /23/. Even at temperatures bellow 70K, the same carrier concentration was obtained as at room temperature. This result, suggesting that no carrier freeze- out is present in the depletion region, has already been observed by other authors /25/. In contrast with experiment, lower (regularly frozen-out) majority carrier concentration was calculated at the edge of depletion region (Fig.8). Since this is an indirect comparison between experiment (capacitance) and simulation (majority carrier concentration) the question remains whether the extraction of majority carrier concentration from measured capacitance at low temperatures can be adequately described by conventional formulae /24/. If these formulae for doping profiling still hold at low temperatures, then the incomplete ionization model (1,2) seems not to be valid at the edge of depletion region, or some other carrier generation mechanisms are important. However, additional work on this subject is necessary for answering these questions.

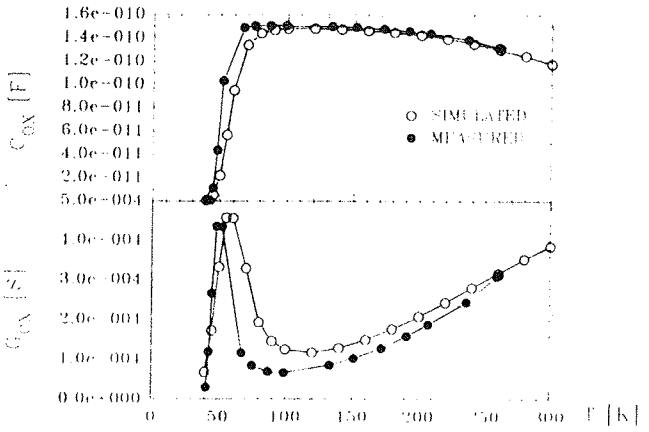

Fig. 7: Measured and calculated MOSC capacitance and conductance

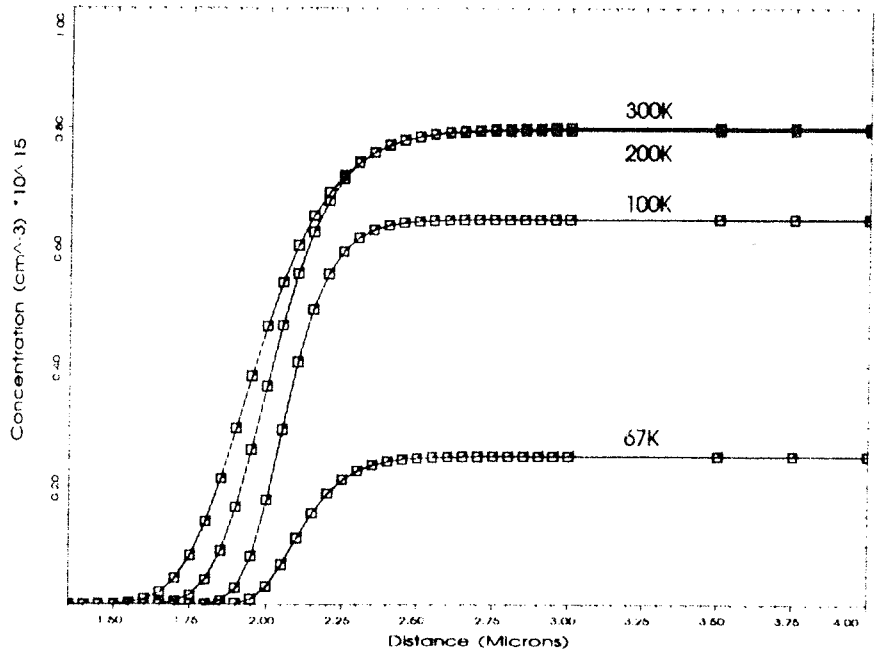

Fig. 8: Calculated freeze-out in the depletion region of MOS capacitor

V. CONCLUSION

Several basic semiconductor devices (resistors, PN junction diodes, MOS capacitors) were fabricated, measured and modeled.

For devices with sufficiently low doping concentrations (low concentration resistor) reasonable agreement was obtained down to 20K. Lack of a general model for incomplete impurity ionization, valid for all doping concentrations, causes several problems for low temperature modeling of devices with highly doped regions.

Modeling of PN junction diodes with properly selected models is in reasonable agreement for temperatures down to 50K. At lower temperatures calculated currents are lower then measured that is probably due to inadequate low temperature behavior of impurity ionization model and possibly to additional carrier generation mechanisms present in measured device.

In MOS capacitor, regularly frozen-out majority carrier concentration was calculated at the edge of the depletion region. Assuming the validity of expressions for doping profiling at low temperatures points to the inaccuracy of incomplete ionization model or presence of additional carrier generation mechanisms at the edge of depletion region.

Finally, due to ohmic drops in the frozen-out regions, increasing importance of actual device geometry for low temperature modeling was detected.

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