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SILICON RADIATION DETECTORS FOR HIGH RESOLUTION X-RAY SPECTROSCOPY

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Abstract: Radiation detectors fabricated on high resistivity silicon substrates are optimum devices for high resolution X-ray spectroscopy in the energy range 1-20 keV. In this paper the principles of operation of pin diode detectors, strip detectors, and drift-chamber detectors are presented. The most important factors that limit their energy resolution are outlined. Different technologies of fabrication are compared, and preliminary results concerning X-ray detectors fabricated at the Institute of Research Science and Technology (IRST) of Trento-Italy, are reported.

Silicijevi detektorji sevanja za spektroskopijo X žarkov z visoko ločljivostjo

Ključne besede: detektorji sevanja, X-žarki spektroskopija, ločjivost velika, tehnika diagnostike, ločljivost energijska

Povzetek: Detektorji sevanja, izdelani na silicijevem substratu z visoko specifično upornostjo, so idealni elementi za spektroskopijo X žarkov z visoko ločljivostjo v energijskem območju 1 - 20 keV. V tem prispevku obravnavam osnove delovanja "pin", "strip" in "drift chamber" detektorjev. Posebej poudarim najpomembnejše dejavnike, ki omejujejo njihovo energijsko ločljivost. Nadalje primerjam različne tehnologije za njihovo izdelavo, na koncu pa podam preliminarne rezultate tovrstnih detektorjev izdelanih na IRST, Institute of Research Science and Technology, v Trentu, Italija.

INTRODUCTION

X-ray spectroscopy is widely used as a diagnostic technique in many fields of fundamental and applied research. For any specific application, the core element of the spectroscopic system, i.e., the X-ray detector, has to satisfy different requirements. For example, cosmic X-ray spectroscopy requires a very good energy resolution, say less than 10 eV /1/, while synchrotron radiation experiments find benefit from both good energy resolution and high count rate capability (>1 MHz). In high energy physics experiments (Matter and Antimatter Colliders) large area silicon detectors are needed with position resolution better than 0.1 millimeters. X-ray computed tomography (ICT), when used as a tool for nondestructive evaluation of large objects such as automobile engine blocks and solid fuel rocket motors, requires detectors with absorption lengths of few centimeters /2/. Automatic X-ray inspection systems are used to detect solder-joint defects on PCB assemblies with components down to a 20-mil pitch, including components with hidden solder joints, such as ball-grid arrays. X-ray detectors are used for dosimetry, nuclear radiation spectroscopy, and computed tomography in medical applications. More recently, portable X-ray fluorescence spectrometers are gaining an increasing interest for in-situ quantitative analysis of concrete materials, soil contamination, waste management and environmental control /3/.

PRINCIPLES OF OPERATION

Solid state ionization detectors are based on the principle that when a radiation of energy E impinges on a target material with ionization energy $E_{ion} < E$, it is absorbed by atomic ionization, a process called photo-ionization or photoelectric effect. The amount of almost-free charge produced is proportional to the energy of the incident radiation, and is determined by collecting and measuring the photo-induced current. In semiconductors, the electric current is carried by either electrons and holes. The average number of electron-hole pairs generated by a photon of energy $E=h\nu$ is $<N>=E/\varepsilon$, where ε is the energy loss per electron-hole pair production. The ionization energy of a semiconductor is somewhat related to the band gap energy, so that it is slightly temperature dependent. In Si ε = 3.62 eV at 300 K, while ε = 3.76 eV at 77 K; in Ge ε = 2.96 eV at 77K /4/. In principle, low band gap semiconductors are more suitable as ionization detectors, because they would give rise to a higher photocurrent signal. In practice, low band gap semiconductors are prone to a higher thermal generation of carriers which, in turn, means higher leakage current, more noise, and ultimately, lower energy resolution. For this reason Ge photodetectors are usually operated at Liquid Nitrogen Temperature (LNT). Assuming a Poisson statistical distribution for the process of electron-hole pair generation, the fluctuation in the number of carriers produced by a single event is $\sigma = \sqrt{N}$. In practice, since the processes that give rise to the formation of each individual charge

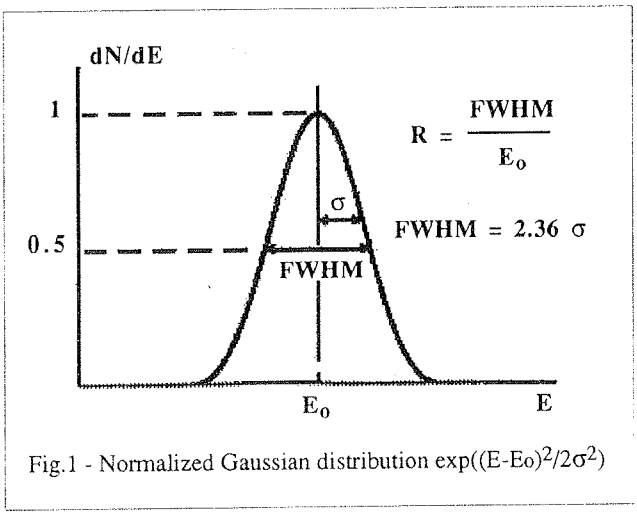


Fig.1 - Normalized Gaussian distribution $\exp((E-Eo)^2/2\sigma^2)$

carrier are not independent, the actual observed fluctuation is lower than the expected one by a factor $\sigma = \sqrt{FN}$, where F, called the Fano factor, is the ratio between the observed variance in N and the Poisson predicted variance ($\sigma^2 = N$). For Si F can be assumed equal to 0.14 /5/. If all the generated carriers are collected and the corresponding current is measured, then the resulting peak height is proportional to the energy E. The average measured energy is: $\langle E \rangle = \langle N \rangle \varepsilon$, and the statistical distribution of E is gaussian. The energy resolution R can be quoted as either: 1) ΔE_{FWHM} (FWHM = Full Width at Half Maximum) in units of energy [eV], or 2) R (= $\Delta E_{FWHM}/\langle E \rangle$) as percentage. Recalling that FWHM = 2.36 σ, (see figure 1), we have for the energy resolution:

$$\Delta E_{FWHM} = 2.36\ \sigma\ \varepsilon \propto \sqrt{N}\ [eV], \text{ or}$$

$$R = \Delta E_{FWHM}/E = 2.36\ \sqrt{F/N} \propto 1/\sqrt{N}$$

These expressions show that the energy resolution is a function of the incident energy E. For this reason it is preferable to quote R at some specified energy (ex: R=300 eV @ 6 keV, or R=5% @ 6 keV). The penetration depth of a radiation of energy E into an absorbing material is determined by Beer`s law of absorption:

$$I(x) = I_o \exp(-\lambda x)$$

where I_o is the intensity of the incident beam (photons/cm^2), $\lambda(Z,E)$ = linear absorption coefficient in units of [cm^{-1}] is a parameter which depends upon the absorbing material, the absorption process, and the radiation energy. $1/\lambda$ is a characteristic absorption length that corresponds to the depth of penetration at which the primary beam is attenuated by 66% ($I/I_o = 1/e$). As a reference, a list of typical absorption lengths for X-ray photons in silicon is reported in table I.

As can be seen, a 0.5 mm thick silicon wafer can absorb almost entirely a 10 keV X-ray, while only about 63% of a 16 keV perpendicularly incident beam is absorbed. In case of a single photon event, 1-exp(-λx) represents the probability that the photon escapes from the absorber. Another mechanism of escape is re-emission of X-rays by the excited absorbing atoms after K or L atomic shell decay /4/.

Table I. Selected linear absorption coefficients for X-ray photons in silicon.

X-ray Energy [keV]	Absorption coeff. [cm^{-1}]	Absorption length [μm]
6	341	29
10	78.6	127
16	19.86	503
20	10.35	966

PIN DIODE DETECTORS

Pin diodes are realized on single crystal Ge or Si wafers of thickness ranging from 200 to 3000 μm. One side of the detector is p+ doped, the other side is n+ doped, whilst the bulk is of intrinsic type. The intrinsic semiconductor is obtained by the Lithium ion drift process /4,6/. The acronyms pin stands for p-type-intrinsic-n-type (or p-i-n type) doping. One disadvantage of Li-drifted detectors is that they are quite instable at room temperature, so that they have to be operated, and preferably stored, at Liquid Nitrogen Temperature. Current state-of-the-art Si(Li) detectors have an energy resolution of about 150 eV @ 5.89 keV (^{55}Fe K_α line) and they are used primarily in microanalysis systems combined with Scanning Electron Microscopy (SEM). Radiation detectors operating at room temperature are preferably realized in ultra pure, electronic grade, silicon crystals obtained by Float Zone (FZ) refinement. As grown, ultra pure silicon ingots turn out to be not absolutely intrinsic, but slightly p-type doped. They can be slightly n-type doped with careful fabrication techniques or by neutron transmutation doping (NTD). Typically, the bulk resistivity can range from 2 to 20 KΩ-cm, and depending on the type of doping, the corresponding diode detector is named p-π-n or p-ν-n. To simplify the cited nomenclature, here after we will adopt the generic acronyms of "pin" diodes for all those p-n junction devices operating in full depletion mode. A schematic representation of a PIN photodiode is reported in figure 2.

When a p-n junction is reverse biased, electron-hole pairs generated inside the depletion region are stripped away from the space charge region and hopefully collected at the p+ and n+ (shallow) contacts. If the junction is operated in full depletion mode, the drift velocity of the almost-free carries is limited only by the saturation velocity of electrons and holes, i.e., about 10^7 cm/s in silicon. As a consequence, the response time of a fully depleted silicon detector is typically of the order of tens of nanoseconds. In practice, not all the generated carries are collected at the p+/n+ contacts. Some of them are lost

because of competitive processes such as charge trapping - which can occur either in the bulk or at the SiO_2/Si interface - and recombination (i.e., electron-hole annihilation) - which can occur either in the depletion region or in the heavily doped p+/n+ regions. Outside the space charge region, electron-hole recombination is predominant and carrier transport occurs by diffusion. Therefore, ionization events occurring outside the depletion region contribute to decrease the detector efficiency and to increase the response time.

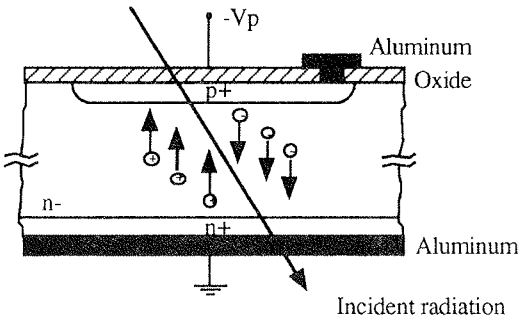


Fig.2 Schematic representation of a PIN diode detector

Owing to the fact that the depletion width W of an abrupt p-n junction is proportional to the inverse square root of the applied potential V ($W = \sqrt{2\varepsilon V/qN}$, where ε is the dielectric constant = 1.04 pF/cm in Si, q is the elemental charge = 1.602×10^{-19} C, and N is the substrate doping in units of cm^{-3}), it turns out that, in order to deplete a 500 μm thick, >5 kΩ-cm in resistivity (<10^{12} dopant atoms/cm^3) π-type silicon wafer, the p-n junction must be reverse biased at a voltage > 150 V. Hence, the pin diode must sustain a high breakdown voltage while keeping the reverse leakage current low. To accomplish these specifications it is necessary to use guard-ring layout structures, and, concurrently, to have a fabrication process that does not degrade the properties of the ultra-pure starting material, i.e., an appropriate technology. For the guard ring topology there are several possibilities. The one adopted in the design of X-ray detectors at IRST is a series of floating rings which sustain a potential degrading from the front center electrode - which defines the active area of the device - towards the outermost front-side electrode, which can be eventually biased at the same potential of the backside contact. More details on the fabrication technology and on the detector layout will be given in the following sections.

STRIP DETECTORS

Strip detectors are very similar, in principle, to pin diodes, as they are fully depleted devices realized on high resistivity silicon substrates /7/. The main difference is that, instead of having a single collecting electrode, the anode is segmented in a series of microstrips a few tens of microns wide. An example of detector layout is reported in figure 3. Each microstrip is connected to an electronic readout channel. In this way a lateral resolution of less that 0.1 millimeters can be achieved. In more advanced designs, the back side of the wafer is processed so as to realize microstrips of the same dimensions, but orthogonal, to those of the front side. In this way three-dimensional devices are obtained, with a pixel, granularity resolution of less than 0.05 mm in x-y direction, and 0.2-0.3 mm in the z coordinate. After signal processing, these devices can achieve a position resolution of less than 10 μm /8/.

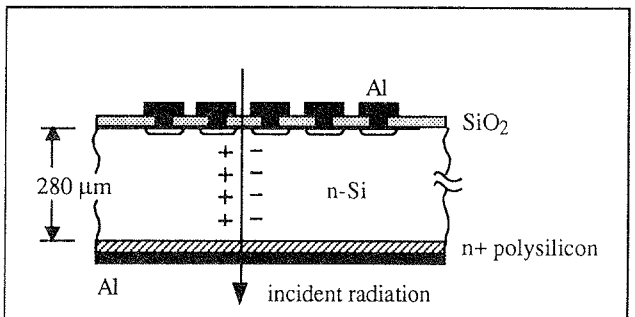


Fig.3 - Silicon strip detector cross-section.

One disadvantage of strip detectors is the necessity of a great number of readout electronic channels, that makes the total electronic system quite complicated. Another disadvantage is the high capacitance of the microstrip, that imposes the use of very low noise preamplifiers. Another problem is that, since the electric charge generated inside the detector by the interaction with the incident radiation is not completely localized, the signal is spread out over two or more adjacent strips. For these reasons it is customary to connect one readout channel every group of four or more strips, and to sequentially scan the channels with analog multiplexing.

The primary advantage of strip detectors is the possibility to realize detectors with very large active area (several cm^2) while preserving a very good position resolution (<0.1 μm). Strip detectors are used primarily as vertex detectors in nuclear physics experiments where high energetic beams are made to collide in a specific point of space. When used for soft X-ray spectroscopy, silicon strip detectors can achieve an energy resolution of 350 eV FWHM @ 5.9 keV, and 2 μs peaking time, when cooled at -5°C /9/.

DRIFT DETECTORS

The silicon drift detector (SDD, also called Semiconductor Drift Chamber, SDC) was first proposed by Gatti and Rehak in 1984 /10/. SDD is a fully depleted device made on high resistivity n-type silicon wafers with rectifying p+ junctions implanted on both sides. The detector is fully depleted of mobile electrons by a suitable potential applied on both sides of the wafer. An electrostatic potential parallel to the surface is superimposed to the depleting vertical one by means of resistive voltage dividers. A schematic view of a drift detector is reported in figure 4. The resulting potential distribution inside the detector drift

region is shown in figure 5. While holes are swept away by the p+ electrodes close to the point of interaction, electrons generated inside the volume of the detector are drifted along the bottom of the potential valley toward a small collecting anode located to one side, or placed at the center of the detector area in case of circular geometry. In this way the signal produced by the drifting electrons is induced at the anode only when they arrive to a close proximity, so that the collecting time can be very short /11/. Moreover, the drift time of electrons measures the radial coordinate of the interaction point, as the electric field E and the drift velocity ($v_d=\mu E$) are known. The drift time for a few millimeter wide detector is of the order of microseconds, and the radial position resolution that can be achieved is less than 10 μm /12/.

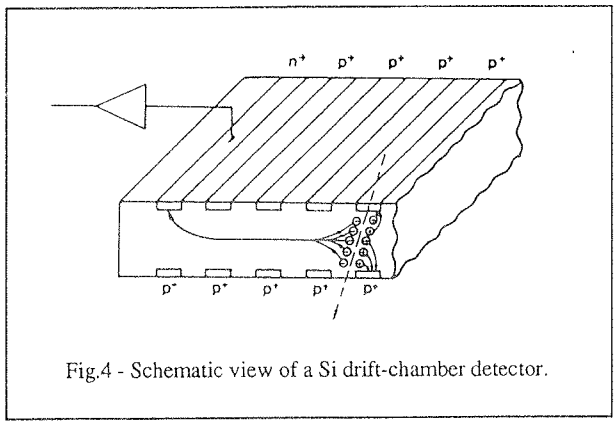


Fig.4 - Schematic view of a Si drift-chamber detector.

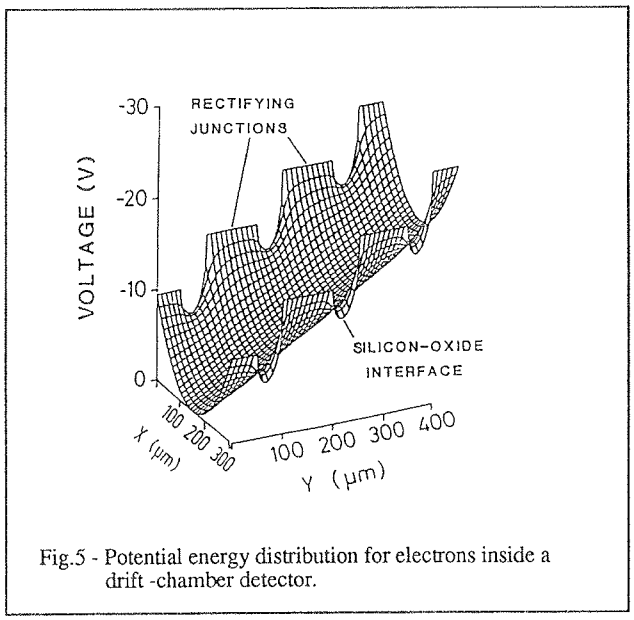


Fig.5 - Potential energy distribution for electrons inside a drift -chamber detector.

The advantages of silicon drift detectors are: i) they require a much lower bias to achieve full depletion of the silicon bulk as compared with pin diodes; ii) the anode capacitance is much lower than that of standard junction detectors of the same dimensions. As a consequence, the electronic system noise can be reduced to a much lower level, and the detector can operate with higher energy resolution, higher counting rate, and at higher temperatures. One disadvantage of silicon drift detectors is the rather complicated bias electronic circuitry necessary to distribute the longitudinal parallel potential through the p+ electrodes. One possible solution is to use a single spiral electrode, instead of concentric rings, as reported in reference /13/.

ENERGY RESOLUTION

The energy resolution of semiconductor detectors depends on two factors: i) the fluctuation in the number of electron-hole pairs generated by the incident radiation, and ii) the fluctuation in the amount of charge effectively collected and detected by the readout (front-end) electronic system. The first factor is inherent with the physics of conversion of radiation energy into electric charge, is described by the Poisson statistics, and poses an intrinsic limit to the energy resolution equal to $(FWHM)_{Statistical} = 2.36\sqrt{F\varepsilon/E}$. The second factor is inherent with the physics of electric charge transport and measurement, is determined by the "electronic noise" present in the system, and poses an extrinsic limit to the energy resolution which depends on the circuits and devices employed in the readout electronic system. If each source of fluctuation is independent, then the overall FWHM is the quadrature sum of the FWHM values for each individual source:

$$(FWHM)^2_{total} = (FWHM)^2_{statistical} + (FWHM)^2_{noise} + + (FWHM)^2_{drift} + ...$$

where the ...dots stand for any other independent source of fluctuation.

In the field of radiation detection and measurement, the energy resolution due to electronic noise is customarily expressed in terms of equivalent noise charge (ENC) instead of $(FWHM)_{noise}$. ENC is defined as the amount of charge which, if applied suddenly to the input terminals of the system, would give rise to a signal to noise ratio S/N=1, i.e., to an output signal equal to the root mean square (r.m.s.) level of the output due only to noise. Recalling that FWHM = 2.36 σ and $E_{noise} = \varepsilon ENC$, we have for silicon at room temperature:

$$(FWHM)_{noise} = (2.36) \times (3.6)\ ENC = 8.5\ ENC$$

where $(FWHM)_{noise}$ is expressed in units of eV, and ENC is expressed in units of "electrons r.m.s.". In figure 6, the calculated intrinsic and extrinsic limits to the total energy resolution of silicon detectors at room temperature are reported for different values of the electronic noise.

The detector equivalent noise circuit is reported in figure 7. Since the time scale for the release of radiation energy to the absorber is the order of 10^{-12} seconds, the detector can be represented by a current source giving a pulse of intensity $Q\delta(t)$, where $\delta(t)$ is the delta-Dirac function. The contributions to the noise sources are /14/:

1) the detector leakage current I_D, represented by a parallel, white noise, current generator;
2) the dielectric loss, represented by a parallel, frequency dependent, noise current generator;

3) the preamplifier thermal input noise, represented by a series, white noise, voltage generator;
4) the 1/f device noise contribution, represented by a series, 1/f, noise voltage generator.

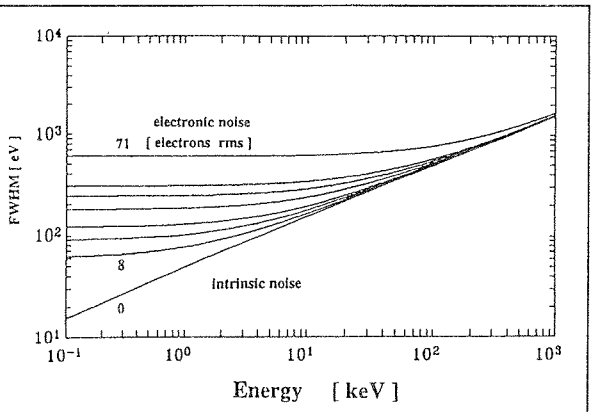


Fig.6 - Calculated energy resolution vs incident radiation energy of a silicon detector at 300K.

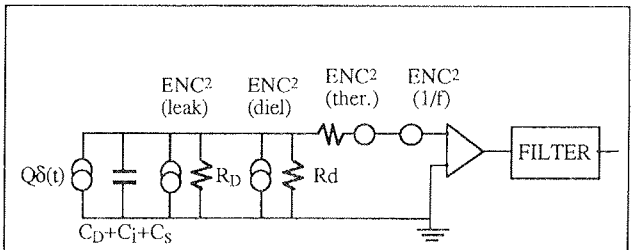


Fig.7 - Detector Noise Equivalent Circuit.

The total Equivalent Noise Charge present at the input of the preamplifier will be the quadrature summation of all the contributions:

$$(ENC)^2_{total} = (ENC)^2_{leak} + (ENC)^2_{diel} + + (ENC)^2_{thermal} + (ENC)^2_{1/f}$$

After pre-amplification, the noise and the signal must be filtered in order to optimize the signal-to-noise ratio. The purpose of filtering is to eliminate the low and high frequency components of the signal, while preserving the most important information, i.e. amount of generated charge. The output of the filter would be a voltage pulse whose height is proportional to the energy of the incident radiation. Each pulse is then discriminated and processed by a multi-channel analyzer (MCA). Theoretically, the best signal-to-noise ratio is attainable if the signal pulses are shaped to the form of an infinite cusp /15/. Practical filters implements Triangle, Gaussian, Semi-Gaussian, or other shaping functions that exhibit signal-to-noise ratios only slightly worse than the theoretical limit /16/. The time constant of the shaping function poses a limit to the time resolution of the detector, which in turn defines the maximum pulse count rate.

The energy resolution is affected by parameters which concern both the detector and the front-end electronics. They are: i) the output capacitance of the detector C_D, ii) the input capacitance of the pre-amplifier stage Ci, and iii) the time constant of the shaping function. Gatti and Manfredi /17/ have shown that to a first approximation, neglecting the frequency dependence of dielectric losses and the 1/f spectral power density in the series generator, the electronic equivalent noise charge can be expressed as:

$$(ENC)_{electr} = (2qK_BT/\pi)^{1/4} (I_DC_D/f_T)^{1/4} ((C_D/C_i)^{1/2}+(C_i/C_D)^{1/2})^{1/2} \text{ [Coulomb r.m.s.]}$$

where K_B is the Boltzmann constant, f_T is the cut-off frequency of the input stage of the preamplifier ($f_T = g_m/(2\pi C_{FET})$ in case of a single JFET). The corresponding optimum filter shaping time constant is:

$$\tau_{opt} = (K_BT/(2\pi q))^{1/2} (C_D/f_TI_D)^{1/2} ((C_D/C_i)^{1/2} + + (C_i/C_T)^{1/2})$$

The optimum resolution can be achieved when the mismatch factor: $(C_D/C_i)^{1/2}+(C_i/C_D)^{1/2}$ is equal to one, i.e., when the output capacitance of the detector matches the input capacitance of the preamplifier. It is worth noting that in these conditions $ENC_{opt} = \sqrt{2}I_D\tau/q$ [el. rms]. This expression outline the direct dependence of the noise from the leakage current of the detector and from the time constant of the shaping function.

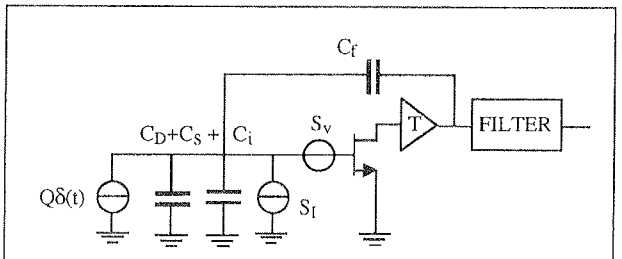


Fig.8 - Detector noise equivalent circuit, including feed-back. T = transimpedance amplifier.

In principle, a current pulse Q(t) would give rise to an ideal voltage signal V=Q/C, when applied to an ideal capacitor C. In practice, C is the total capacitance seen at the detector terminals (including strays), and it may even not be constant during the integration time of the signal. In order to preserve the basic information carried by the magnitude of the generated charge Q, the most common configuration of the input preamplifier is that of a charge sensitive amplifier (CSA). The input stage of the amplifier is preferably a silicon JFET for better 1/f noise performance. The corresponding noise equivalent circuit is reported in figure 8. The feed-back capacitance, the test capacitance, and the parasitic (stray) capacitance are also taken in consideration. As outlined by Radeka /14/ the noise sources can be categorized into those that are effectively in parallel with the input and those that are in series with the signal source. In figure 8 all the noise sources are included in the series and parallel noise generators with spectral power densities /18/:

$$S_V = \alpha\, 2K_BT/g_m + a_f/f \quad [V^2/Hz]$$

$$S_I = q(I_D + I_G) + 2K_BT/R_f + b_f f = q\, I_L + b_f f \quad [A^2/Hz]$$

where g_m is the input FET transconductance, α is a coefficient ranging from 0.5 to 0.7 depending on the FET operating point, f is the frequency, a_f is the FET 1/f noise coefficient, q is the electron charge, I_D is the leakage current of the detector, I_G is the FET gate leakage current, R_f is the feedback resistance (if used in the charge amplifier), and b_f is the dielectric noise coefficient. I_L is the total equivalent leakage current associated with the white parallel noise. The electronic noise of the system can be expressed in terms of equivalent noise charge as /19/:

$$(ENC)^2_{electr} = A_1\, C^2_T 4K_BT\, 2/(3g_m\,\tau) + A_2\,(2\pi a f C^2_T + b_f/2\pi) + A_3\,(2qI_L)\tau$$

where C_T is the total capacitance seen at the detector terminals, i.e., the sum of detector output capacitance C_D, the FET input capacitance C_i, stray capacitance of the connection C_s, the test capacitance C_t, and the feedback capacitance C_f. In deriving the above expression, it has been assumed that the series noise source is given by the thermal noise of the FET channel and by the 1/f-term with power density $a_f/|f|$, and that the parallel noise source is given by the shot noise of the leakage current I_L and by a term taking into account dielectric losses with a power density $b_f\,|f|$. τ is the shaping time constant. A_1, A_2, and A_3 are parameters which depend on the type of shaping /20/. In some designs, a test capacitance C_t is also integrated on the same chip and is used to calibrate the system response to a known pulse. In that case, C_t must be included into the value of C_T. In more advanced designs, the feedback resistor R_f is removed from the feedback loop in order to achieve the lowest noise /21/.

In summary, the most important factors which affect electronic noise are: 1) the detector reverse leakage current; 2) the detector-preamplifier capacitance mismatch; 3) the input JFET channel transit time (affecting $f_T = g_m/2\pi C_{FET}$); 4) the dielectric losses. Dielectric losses are due to the parasitic capacitance associated with the package and the assembly . The dielectric loss contribution to the total ENC can be expresses as follows:

$$(ENC)^2_{diel} = e^2/\pi\, K_BT\, DC_d$$

where e=2.718.., D is a loss factor given by the ratio between the imaginary part and the real part of the dielectric constant, and C_d is the capacitance of the dielectric. The dielectric loss factor can range from $D=2x10^{-2}$ (standard dielectric) to $D<10^{-3}$ (good dielectric) until $D=5x10^{-5}$ (best dielectric). As an example, the contribution to the electronic noise from a "best dielectric" parasitic capacitance of 5 pF at room temperature (R.T.) is about ENC = 10 electrons rms, corresponding to a FWHM = 85 eV. It is obvious that a proper choice of the package material and the care taken into assembling the whole system are of primary importance. An unavoidable contribution to the stray capacitance comes from the bonding wires connecting the detector to the input stage of the pre-amplifier. Integration of the detector with the readout electronics is foreseen as a possible solution to this problem.

PROCESS AND TECHNOLOGY OF FABRICATION

The leakage current of reverse biased p-n junctions is the technological parameter that mainly determine the detector intrinsic noise level, and therefore limits the energy and position resolution. In the last decade different detector designs have been proposed and realized. Besides microstrips and drift chambers, fully depleted CCDs are worth mentioning /22/. All these devices are characterized by leakage current densities of the the order of 1 nA/cm^2. Two different strategies have, so far, been proposed to obtain such a low level of leakage current. One relies upon the minimization of high temperature steps, as they can lead to carrier lifetime degradation through defect activation. The other exploits extrinsic gettering techniques to preserve long carrier lifetimes by counteracting the detrimental effect of contaminants. The first approach has been proposed by J.Kemmer /23/, who has developed an ad-hoc process in which, after an initial oxidation at 1030°C with HCl, the wafer sees only a 30 min dopant activation anneal at 600°C. On the other hand, S.Holland /24/ has adopted more conventional fabrication procedures with the purpose of obtaining a CMOS compatible detector technology. This second approach seems to be irrenounceble if the final goal is the integration of the detector with the read-out circuitry on the same chip. By embracing this latter strategy, we have started to develop fully-depleted PIN (actually p-ν-n) silicon radiation detectors with on-chip JFET devices. A preliminary process has been defined, featuring different extrinsic gettering techniques. Small area radiation detectors, as well as several other test-structures, have been fabricated and electrically characterized. Figure 9 shows the layout of a typical high voltage pin diode with concentric guard rings.

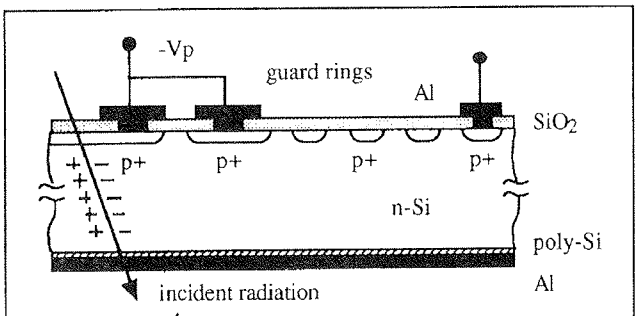


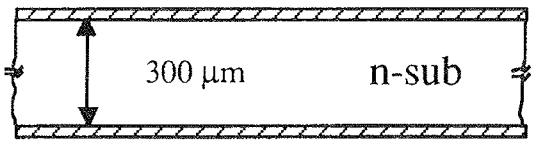
Fig.9 - Half PIN diode cross-section.

Devices were processed using 4 inch diameter Float Zone (FZ), 280 μm thick, <111> oriented, phosphorus doped silicon substrates, with nominal resistivity of 2 kΩ-cm, corresponding to a donor concentration of about $2x10^{12}$ cm^{-3}. Three different gettering techniques, namely back-side phosphorus implantation, phosphorus diffusion from $POCl_3$ source, and phosphorus-doped polysilicon deposition /25/, were implemented in order to compare their effectiveness in reducing the detector leakage current.

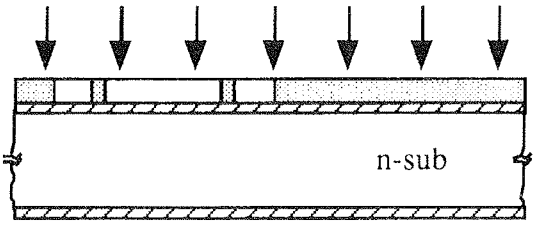
The basic process flow adopted for the wafers implementing the back-side phosphorus implantation can be described as follows. After initial oxidation at 975°C in dry

Si - PROCESS FLOW CHART

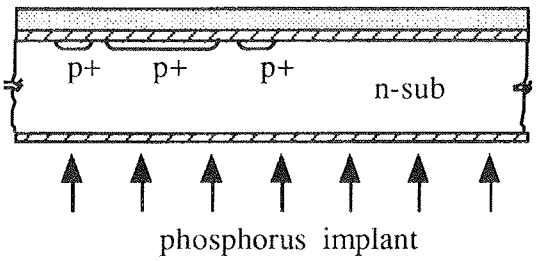
1.Screen oxide (dry O_2, 975°C, 45 nm)



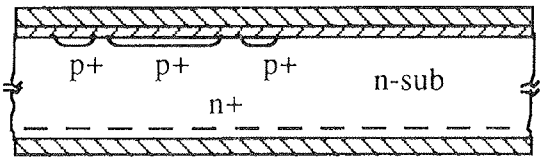
2. Mask. Implant B, 30 keV, 5E14/cm^2



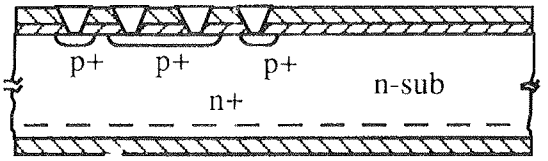
3. Back-side implant P, 120 keV, 5E15/cm^2



4. Post-implant anneal 700-850°C, N_2



5. Mask. Contact opening.



6. Aluminum deposition and patterning.

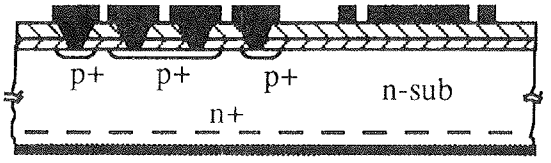


Fig.10 - Silicon detector's process flow chart.

O_2, the p+ regions were formed by ion implantation of boron (5.0x10^{14} atoms/cm^2, 30 keV), using photoresist as a barrier. Having protected the front side with photoresist, the back-side was uniformly implanted with phosphorus (5.0x10^{15} cm^{-2}, 120 keV), ensuring a good ohmic contact and providing the first type of gettering. A Low Temperature Oxide (LTO) layer was then deposited at 450°C and the post-implant annealing was performed (60 min. in N_2 at 850°C). After that, contacts were opened in the oxide and aluminum-silicon (1% Si, 600 nm) was deposited at 400°C and patterned. The back-side of the wafers were then cleaned and a cold aluminum deposition (500 nm) was performed. Finally wafers were sintered in forming gas (5 min. at 400°C). The whole process flow chart is depicted in figure 10.

The same basic process sequence was adopted also for wafers to be treated with $POCl_3$ and polysilicon. However, these two gettering techniques required some additional preliminary step to be performed. In fact, after having protected the front side of the wafer with a thick layer of LTO (600 nm), the back-side was treated with a $POCl_3$ predeposition (20 min. at 920°C) followed by a 40 min drive-in at 975°C. Alternatively, an undoped, 200 nm thick, polysilicon layer was deposited at 625°C and then doped by using the same $POCl_3$ predeposition. After getting rid of the excess phosphorus glass, the back-side was protected by a thick layer of LTO, and the front-side passivation layer were removed. From this point on, the process steps coincide with the already described sequence, except, of course, for the back-side phosphorus implantation.

EXPERIMENTAL RESULTS

Figure 11 shows the measured reverse leakage current of 1.8 mm^2 area PIN diodes processed with the three different gettering techniques adopted. The mean leakage current density at 100 μm of depletion with (about 20 V of reverse voltage), averaged over ten samples belonging to the same wafer, is reported, along with the corresponding standard deviation values. As can be seen, extremely low leakage current densities, in the order of 0.1 nA/cm^2 as well as good on-wafer process uniformity, were obtained in the case of P-doped polysilicon gettering. It is worth noticing that, also for the other two gettering techniques, mean leakage current densities lower than 1 nA/cm^2 were measured. By correlating the reverse I(V) characteristics of a PIN diode with the C(V) curve of the same device, it was possible to estimate the generation lifetime of the three devices. The results are reported in table II.

Table II. - Reverse leakage current density (J_{dark}) and minority carrier lifetime of 1.8 mm^2 PIN diodes fabricated with different gettering techniques.

Gettering technique	J_{dark} [nA/cm^2]	life-time [ms]
P - implant	0.46+/-0.19	52
$POCl_3$ diffusion	0.40+/-0.19	60
P-doped poly-Si	0.14+/-0.019	172

More detailed analysis of the experimental results, combined with computer simulation of the layout structures /26/, lead to the conclusion that efficiency of the guard ring structure was partly affected by the presence of an accumulation layer at the SiO_2/Si interface. This accumulation layer is induced by a fixed positive charge in the oxide of density $4x10^{11}$ cm^{-2}, a value inferred from experimental C(V) curves obtained on MOS capacitors built on the same test-chip. The presence of such accumulation layer at the Si/SiO_2 interface can produce a premature breakdown in some weakest devices, as reported in figure 12.

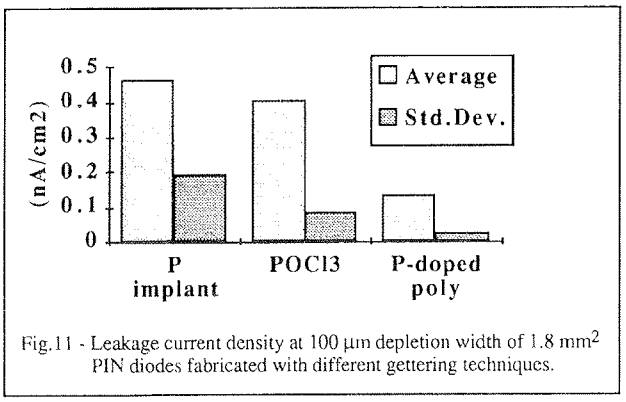


Fig.11 - Leakage current density at 100 μm depletion width of 1.8 mm^2 PIN diodes fabricated with different gettering techniques.

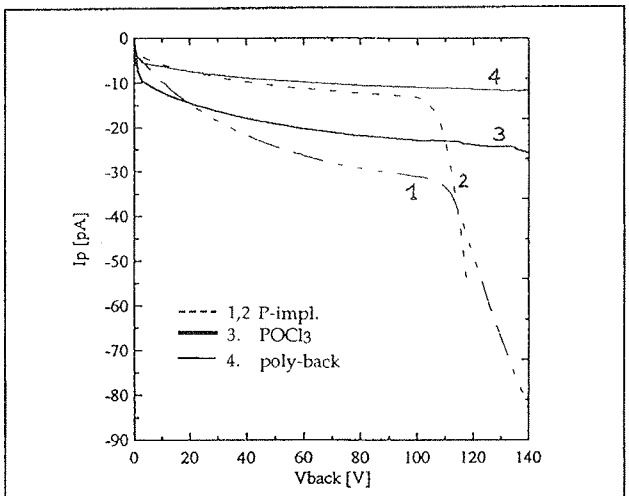


Fig.12 - Reverse leakage current of 1.8 mm^2 PIN diodes fabricated with different gettering techniques.

These preliminary results indicate that, with the use of the silicon technology currently available at IRST, it is possible to realize radiation detectors that meet the desired specifications of high breakdown voltage and low reverse leakage current density. Further work is in progress to optimize the device layout structure, and to realize silicon JFETs on the same high resistivity substrate, with the aim to integrate the detector and the first stage of preamplification on the same chip.

CONCLUSIONS

Conventional Lithium-drifted X-ray silicon detectors (Si(Li)) have been used as diagnostic tools in microanalysis systems for many years. Present state-of-the-art Si(Li) detectors exhibit a fairly good energy resolution (150 eV @ 5.9 keV), but they need to be operated at 77K (Liquid Nitrogen Temperature). The requirement of detectors with higher energy resolution and/or able to work at higher temperature has driven the research in the field of silicon radiation detectors in two directions. One is the realization of thermal detectors that operate at very low temperature (<1K). These are called "microcalorimeters" and can achieve an energy resolution ΔE_{FWHM} <10 eV @ 5.9 keV /27/. The second is the development of "ionization" detectors that work at room temperature, or at temperatures that can be easily and inexpensively achieved with an electric Peltier cooler (-30°C). In this paper we have presented the principles of operation and the technology of fabrication of the three most common types of ionization detectors - namely pin diodes, microstrip detectors, and drift chambers. All of them are realized on ultra pure (FZ) - high resistivity - single crystal silicon, and are based on the same principle of operation, i.e., the collection of electron-hole pairs generated inside a fully depleted bulk region. Two fabrication technologies have been developed, one based on low temperature processing, and one more CMOS compatible. The energy resolution that can be achieved by these detectors strongly depends on two parameters: i) the reverse leakage current of the detector itself, and ii) the matching of the detector impedance with the readout electronics. Present state-of-the-art silicon technology allows to obtain devices with carrier lifetime of several milliseconds, corresponding to reverse leakage current density of less than 1 nA/cm^2. This fulfills the first requirement of having a good energy resolution. Integration of the detector with the readout electronics would in principle meet the second requirement, i.e., matching the detector with the readout electronics. However, this latter solution is still rarely implemented because of the difficulty to preserve the high quality of the starting material along the entire sequence of a whole CMOS process. Recently, promising results with PIN-diode-based detector arrays featuring an integrated readout circuitry on high resistivity Float-Zone silicon have been reported /28/. More recently, Peltier cooled X-ray PIN detectors with energy resolution of 250 eV @ 5.9 keV at -30°C have been made commercially available /29/. In table III some characteristics of various detectors are reported for comparison.

Table III. - Energy resolution of silicon X-ray detectors @ 5.89 keV (^{55}Fe K_α line).

Detector type	Area [mm^2]	ΔE_{FWHM} [eV]	Temperature	τ_{shape} [μs]	Reference
bolometer	1	<10	<0.1K	1,000	/1/
Si(Li)	12	150	77K	16	/30/
microstrip	0.1x96	350	-5°C	2	/9/
drift chamber	1.5	229	-30°C	6	/19/
pin diode	7	250	-30°C	12	/29/

In this paper, we have focused our attention on the performance of silicon radiation detectors for soft X-ray spectroscopy. However, it is worth mentioning that ioni-

zation detectors are sensitive to any kind of ionization radiation, like for example γ-rays, fast electrons and positrons, α-particles. For this reason silicon radiation detectors are widely employed in nuclear physics experiments, where high energy beams of matter and antimatter are made to collide with the aim to investigate the formation of primitive matter in conditions as close as possible to that of the origin of the universe (the so called big-bang).

For these applications, a considerable amount of detectors is necessary to fill up a volume of some cubic meters. The realization of these experiments, that pose very stringent requirements to the detectors and to the whole electronics involved, is one of the driving force to further developments of high-resistivity silicon device technology, electronic system design and measurements.

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