UDK621.3:(53+54+621+66), ISSN 0352-9045 Informacije MIDEM 25(1995)3, Ljubljana

RADIATION EFFECTS IN SILICON COMPONENTS FOR SPACE APPLICATIONS

C. Claeys, E. Simoen and J. Vanhellemont
IMEC, Leuven, Belgium

Keywords: semiconductors,radiation effects, silicon components, space applications, device physics, radiation hardness, material science, MOS devices, CMOS devices, submicron CMOS, bipolar components, CCD, Charge Coupled Devices, SOI, Silicon-On-Insulator, JFET transistors, defect engineering, gettering, noise performance, ionization damages, displacement damages, semiconductor technologies, bipolar technologies, bipolar devices, Si-SiO_2 interfaces, threshold voltage, silicon technologies, burnout, SEB, Single Event Burnout, MOSFET deficiencies, JFET transistors, TEOS, Tetra-Ethil Ortho-Silicate glass

Abstract: Radiation effects are of crucial importance for space applications, which are a growing niche market of microelectronics. This paper reviews the impact of both ionising and bulk damage effects on the electrical performance of microelectronic silicon components, including Silicon-on-Insulator technologies (SOI), Charge Coupled Devices (CCDs), submicron CMOS, and standard and advanced bipolar components. Beside an overview of the general device characteristics, information will also be given on the underlying physical models. Some measures for obtaining radiation-hard devices are briefly addressed.

Učinki sevanja na silicijeve elektronske sestavne dele namenjeni uporabi v vesolju

Ključne besede: polprevodniki, učinki sevanja, deli sestavni silicijevi, uporaba v vesolju, fizika naprav, odpornost proti sevanju, znanost o materialih, MOS naprave, CMOS naprave, CMOS submikronski, deli sestavni bipolarni, CCD naprave, SOI tehnologije silicij-na-izolantu, JFET transistorji, inženiring hib, getranje, zmogljivost šumna, poškodbe ionizacijske, poškodbe premestitve v mreži atomski, tehnologije polprevodnikov, tehnologije bipolarne, naprave bipolarne, Si-SiO_2 plasti vmesne, napetost pragovna, tehnologije silicija, izgoretje, SEB izgoretje posamično, MOSFET poškodbe, JFET transistorji, TEOS steklo

Povzetek: Učinki sevanja na silicijeve elektronske sestavne dele so bistvenega pomena za uporabo komponent v vesolju, kar postaja vse bolj rastoči trg uporabe mikroelektronike. V prispevku pregledno opisujemo efekte ionizirajočih in notranjih poškodb na električne karakteristike mikroelektronskih sestavnih delov na siliciju vključujoč tehnologije SOI (Silicon-on-Insulator), CCD (Charge Coupled Devices), submikronski CMOS ter standardne in napredne bipolarne tehnologije. Poleg pregleda splošnih električnih karakteristik komponent podajamo tudi ustrezni opis fizikalnih mehanizmov. Na kratko opišemo korake, s pomočjo katerih lahko izdelamo komponente, ki so odporne proti sevanju.

1. INTRODUCTION

About 25% of the Military/Aerospace integrated circuit market is taken by radiation-hard devices, with an increasing importance of the space applications. Major microelectronics applications in a spacecraft are related to telecommunications, scientific instrumentation, data handling, imaging, earth observation, and teledetection. The general microelectronic trends to increase the packing density, to enhance the circuit functionality, and to reduce the power consumption are also becoming important in this field. However, it is well-known that advanced processing steps used in submicron silicon technologies make these technologies more vulnerable to radiation effects so that the required hardness levels can only be obtained by both the implementation of radiation hard process modules and the optimisation at the design level. This paper will mainly focus on the impact of the technological parameters on the radiation hardness.

The space environment consists of a large variety of particles such as electrons, neutrons, protons, heavy particles, X-rays, γ-rays ... with energies ranging from a few keV to GeV. The amount of irradiation encountered by the devices depends on a variety of parameters such as the amount of shielding, the altitude of the polar orbit in combination with the influence of well-known space phenomena such as the Von Allen belts, solar flares, and the South Atlantic Anomalies /1/. Therefore the on-earth simulation of the space environment remains very difficult and is mainly restricted to the simulation of the impact of some dedicated irradiation particles.

Depending on the type of the irradiating particles one has to differentiate between respectively ionising irradiation (e.g. γ irradiations), mainly causing irradiation damage in the silicon dioxide layer and at the Si-SiO_2 interface, and irradiation resulting in displacement damage (e.g. protons, neutrons and electrons) in the semiconductor lattice. In general, the impact of irradiation on the electrical performance will be revealed by a change of the threshold voltage, a reduction of the mobility, a degradation of the transconductance, a reduction of the charge transfer efficiency, a degradation of the current gain, an increase of the leakage current, a reduction of the carrier minority lifetime, single event upsets, latch-up, and an increase of the low frequency noise. Extensive information on these topics is published in the proceedings of the annual IEEE Nuclear and Space Radiation Effect Conference and of the bi-annual European RADECS Conference. A comprehensive compilation of the relevant literature in this field till 1992 can be found in /1/.

This paper will briefly discuss some basic physical phenomena, before discussing more in detail the radiation hardness of different technologies such as Silicon-on-Insulator (SOI), Charge-Coupled Devices (CCD), submicron CMOS, and bipolar technologies. Some alternative technologies will also be briefly addressed. It is an update and extension of a previous review paper by the authors on this topic /2/. Due to space limitations only general trends and some special phenomena will be discussed. Some challenges and future trends will also be highlighted.

2. PHYSICAL IRRADIATION MODELS

Ionising irradiations lead to the formation of defects in the silicon dioxide and at the Si-SiO_2 interface resulting into the generation of the oxide trapped charge and of the interface trap density. This damage will cause a shift in the threshold voltage of MOS devices. A huge amount of publications are dealing with a possible explanation for the involved defect creation mechanism. Presently, two different schools exist /3-4/. On one hand it is believed that due to the irradiation electron-hole pairs are formed in the oxide, whereby the electron is very mobile and the hole moves towards the interface. It is generally accepted that interface traps are trivalent silicon atoms with a dangling bond. After device processing these dangling bonds are saturated due to the hydrogen passivation, so that for modern technologies the interface trap density is very low and in the 10^9-10^{10} cm^{-2} eV^{-1} range. The irradiation-generated holes will lead to broken bonds once they reach the interface, thereby increasing the interface trap density. The oxide traps are believed to be trivalent silicon atoms with an oxygen vacancy and have been identified by electron spin resonance studies. This model is called the trapped-hole model. Another theoretical model, called the hydrogen diffusion model, is based on the fact that during irradiation hydrogen ions throughout the oxide are formed which under positive gate bias may diffuse to the interface and thus creating interface traps according to the following radiochemical reaction /5/

$$\equiv Si\text{-}H + H^+ + e^- \Leftrightarrow \equiv Si\text{-}H + H^0 \Leftrightarrow \equiv Si\text{-} + H_2 \qquad (1)$$

Due to the electron tunneling from the substrate through the oxide, the hydrogen ion is transformed into a hydrogen atom. The hydrogen atom is very reactive and reacts with a saturated silicon bond in order to form an interface trap (dangling bond) and a hydrogen molecule that diffuses away. Although there still exists a lot of controversy about the exact model, more and more experimental evidence is given for the validity of the hydrogen diffusion model.

Detailed studies by Fleetwood and co-workers /6-7/ resulted into a generally accepted nomenclature for the irradiation induced oxide defects. Dependent on the location of the generated traps, distinction is made between bulk oxide traps, border traps and interface traps. This is schematically illustrated in Fig. 1. The reaction time of the generated traps allows a further classification into 'fixed' and 'switching' states. The switching states are those which have an impact on the dynamic operating conditions (e.g. low frequency noise) of the devices. Both states will have an influence on the threshold voltage. Special measurement techniques have been proposed to separate the influence of the oxide and interface trapped charge.

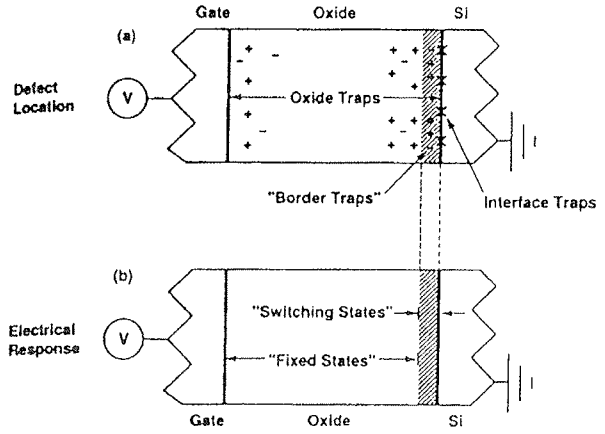

Figure 1: Schematic illustration of the used nomenclature to differentiate between the physical location and the electrical response of the irradiation induced charges, after Fleetwood et al. /7/. 'Border traps' are located in the oxide near the interface and can exchange charge with the Si substrate on the time scale of the measurement.

Dependent on the irradiation conditions a certain amount of energy will be deposited into the silicon material and may therefore result into so-called displacement damage, as reviewed recently /8/. The displacement damage will mainly consist of a variety of defects such as isolated intrinsic defects (self-interstitials and/or vacancies) and defect complexes and defect clusters. In recent years, the authors have used a large variety of electrical and structural analysis techniques (such as TEM, DLTS, infrared spectroscopy, laser scattering tomography, photoluminescence, electrical I-V and C-V measurements, lifetime measurements, low frequency noise spectroscopy) in order to identify and to characterize the electrical behavior of these defects after proton, electron and neutron irradiations /9-11/. Special attention has been given to the impact of the quality of the starting silicon material, i.e. Czochralski (Cz) Si with different interstitial oxygen concentrations - Float Zone - Epitaxial wafers - high resistivity silicon, on the hardness against displacement damage. This study also included the influence of the implementation of gettering treatments, originally intended to reduce the amount of process-induced defects.

3. IRRADIATION HARDNESS OF SILICON TECHNOLOGIES

This section is intended to give an overview of some general features of the radiation hardness of different silicon technologies. Although the irradiation behaviour of several electrical parameters has been extensively studied during the last decade, less attention has been given to the low frequency noise behaviour of devices in a space environment. This topic has recently been reviewed by the authors /12-13/ and will also briefly be mentioned here.

3.1 Silicon-on-Insulator (SOI) Technologies

To improve the total dose irradiation hardness of MOS technologies, Silicon-on-Sapphire (SOS) technologies were introduced around the mid-sixties. The thin silicon film on the insulating substrate (Al_2O_3), in which mesa transistors are fabricated, has a reduced carrier lifetime due to the interfacial lattice mismatch. Although these technologies still have a beneficial irradiation behaviour from a viewpoint of single event upset (SEU) and resistance against so-called gamma-dot upsets caused by solar flares or nuclear explosions, for many space applications SOI technologies have gained a larger market share. It is even so that at the annual IEEE SOS/SOI Technology Workshop only a few papers are still dealing with SOS. For SOI wafers the thin silicon film, which is separated from the silicon substrate by a buried insulator layer, can be obtained by oxygen implantation (SIMOX), wafer bonding and etch back (BESOI) and zone melting recrystallisation (ZMR). The main advantages of using a thin silicon film are latch-immunity, reduced leakage currents, increased SEU thresholds, and the elimination of leakage currents associated with parasitic transistors /14/. For space applications radiation levels between 50 and 100 krad(Si) are sufficient. In addition to several microprocessors, radiation hardened 256k and 1 Mbit SRAMs have also successfully been fabricated on SIMOX material. The trend in device scaling is surely making SOI a winner compared to SOS as for the latter the end-of-life is mentioned to be around the 1.2 μm level.

In SOI devices the irradiation sensitivity is mainly related to the different Si-SiO_2 interfaces associated with the gate oxide, the buried oxide and the isolation oxides respectively. Therefore attention has been given to the impact of both the gate oxide temperature and the isolation scheme used /15/. Hardened devices are obtained by lowering the gate oxidation temperature and by implementing a MESA-LOCOS isolation, whereby a deep trench is etched in the Si film before the sidewalls are oxidized, instead of a standard LOCal Oxidation of Silicon (LOCOS). This is clearly illustrated in Fig. 2, showing that for hardness levels up to 100 krad(Si) a maximum threshold voltage shift of 100 mV is obtained. Also the post-irradiation low frequency noise behaviour is strongly influenced by the isolation scheme as can be seen in Fig. 3 /16/. In strong inversion no difference is observed, while in the subthreshold region the noise strongly increases for the LOCOS device. For the MESA-LOCOS device the noise increase is much smoother. The observed noise spectra are $1/f^n$ like with

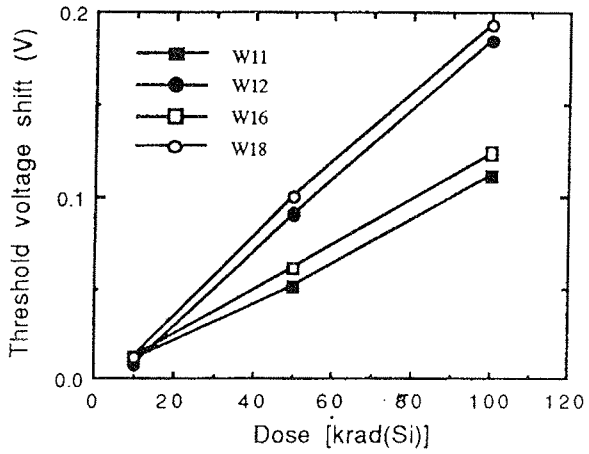

Figure 2: Threshold voltage shift of a SOI nMOST as a function of the total irradiation dose for different isolation schemes and gate oxidation temperatures (W 11: MESA-LOCOS/850°C; W 12: MESA-LOCOS/975°C; W16: LOCOS/850°C: W18: LOCOS/975°C). Irradiations are done for worst case biasing conditions.

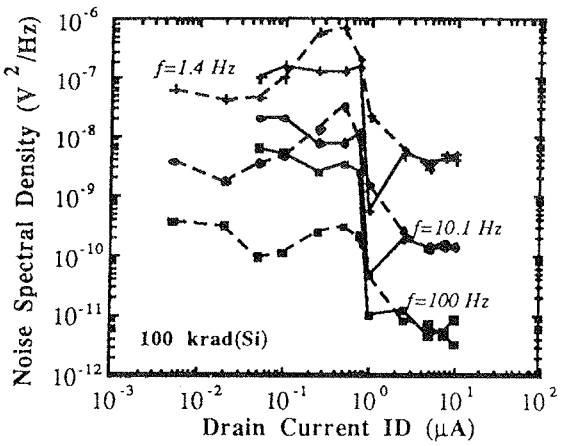

Figure 3: Low frequency noise spectral density of irradiated MESA-LOCOS (dashed lines) and LOCOS nMOSTs for three different frequencies.

n slightly larger than 1. Investigations also pointed out that irradiations have a negligible impact on the excess noise in the kink region of the devices. Hardened SOI technologies are often using an additional boron implantation at the bottom of the silicon film in order to compensate for the irradiation-induced positive charge build-up in the buried oxide as otherwise an inversion layer would be formed /15/. This can only be done for partially depleted devices as fully depleted devices are processed on rather thin silicon films which implies that there is a coupling between the front- and back interfaces.

Other measures to increase the irradiation hardness of SOI devices are either design related, such as e.g. the use of body ties and/or edgeless transistors, or modifying the transistor concept. An example of the latter is to use Gate-All-Around (GAA) or dual gate MOSTs, whereby there is a thin oxide all around the gate /17/. These GAA devices allow total dose levels up to 30 Mrad(Si) /18-19/. An interesting feature is that while the threshold voltage shows a serious rebound after Mrad(Si) irradiations, the low frequency noise has a turn-around behaviour for increasing irradiation doses. The maximum transconductance is a decreasing function of the total dose. The rebound effect is associated with a compensation of the near-interface oxide traps by the interface traps and can be reduced by optimizing the radiation hardness of the gate oxide /19/.

3.2 Charge Coupled Devices (CCD)

CCDs are frequently used for imaging purposes on board of spacecrafts and orbital satellites, so that extensive research has been performed during the last decade. For these devices not only ionizing irradiation but also irradiation-induced bulk damage have a strong impact on the electrical performance and reliability of the devices. In Europe extensive research in this field has been performed by EEV (UK), Thomson (F), IMEC (B) and research groups such as e.g. SIRA, Brunell and Leicester University (UK). For reducing the dark current a dithering technique, a multiphase pinned (MPP) or a virtual phase CCD technology are often used. The ionization damage causes charge build-up in the gate oxide layers resulting in a shift of the threshold voltage, while the generation of interface traps leads to an increase of the surface dark current. In addition transient effects may be observed. Displacement damage produces trapping centres in the silicon substrate, which in turn leads to a reduction of the charge transfer efficiency and the production of dark current spikes and a Random Telegraph Signal (RTS) behaviour.

Systematic studies have been performed in order to investigate the impact of technological parameters on the total dose radiation hardness /20-22/. The standard IMEC n-type buried channel, triple poly and double metal 3 μm CCD technology was evaluated up to 73 krad(Si) and it was observed that i) there is a 3x increase of the dark current density, ii) a high hole trapping factor of 0.6, iii) a high subthreshold leakage, and iv) severe reverse annealing effects after irradiation /20/. By technological modifications such as replacing the solid-source doping at 950°C by an ion implantation, reducing the thermal budget after gate oxidation by restricting the maximal temperature to 800°C, and changing the plasma enhanced CVD reflow oxide in the back end by a tetra-ethyl ortho-silicate glass (TEOS), the radiation hardness level has been increased to 100 krad(Si) /21/. Some typical results are shown in Fig. 4. The modified process is characterized by a threshold voltage shift of 14 mV/krad(Si), a hole trapping factor of 0.04, a dark current increase of less than 2 times, and an increase in interface trap charge of about 2×10^9 cm^{-2} eV^{-1}. A different behaviour of the storage and image region of a Frame Transfer CCD has also been observed /22/. Due to the presence of a metal light shield on the

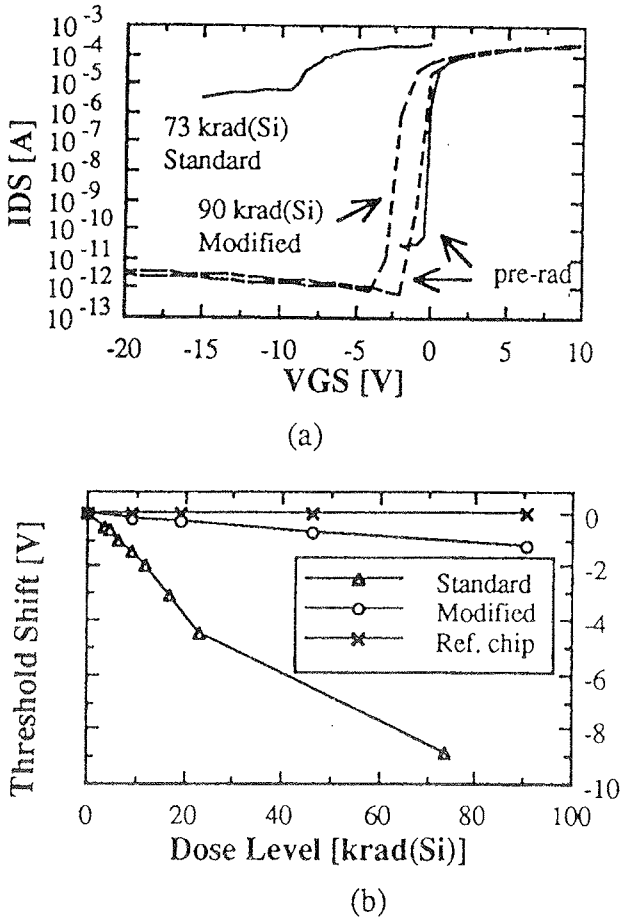

Figure 4: Typical subthreshold (a) and threshold voltage shift (b) as a function of irradiation dose level for the standard and the radiation-hardened CCD process.

storage region, the sintering step in forming gas leads to a large amount of active hydrogen-containing species in the oxide layers. The latter results in a pre-irradiation reduction of the interface trap density, but is at the same time responsible for a higher interface trap density build-up during ionizing irradiation, in agreement with the hydrogen model discussed in section 2 and characterized by eq. (1). This phenomenon is illustrated in Fig. 5, giving the evolution of the average interface trap density during irradiation and subsequent annealing for a CCD device with the sintering step before or after etching the Al light shield.

As already mentioned, CCDs are also very sensitive to irradiation-induced bulk damage. Therefore the authors have studied in detail the impact of the quality of the substrate material and some technological parameters on the radiation hardness of the devices /9-11/. A variety of proton, ^{252}Cf and electron irradiations resulted into the following main conclusions. The oxygen content of the starting material has a strong impact on the radiation resistance, and the best results are obtained for low oxygen wafers and epitaxial material. The degrading impact of the oxygen content has been confirmed by

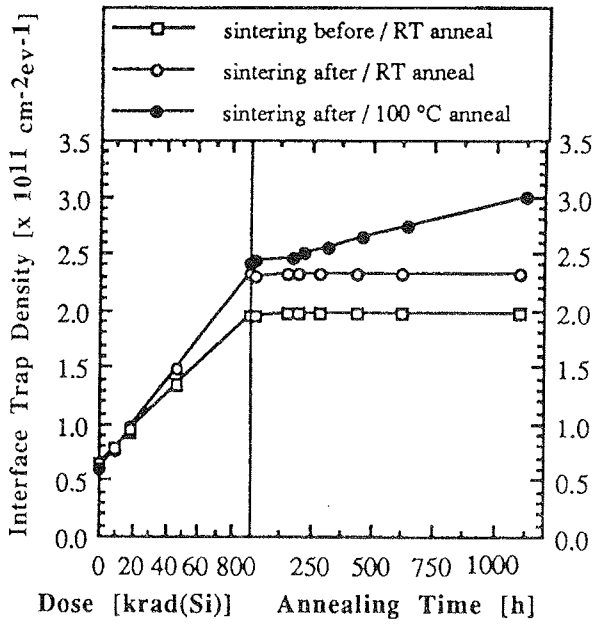

Figure 5: Average interface trap density determined from charge pumping measurements on gate oxide transistors of the radiation hardened CCD process as a function of the accumulated dose level and the subsequent annealing time. A difference is made between a sintering step before or after etching of the Al light shield.

electrical characterizations of diodes, TEM analysis, photoluminescence measurement, and DLTS analysis. The SiO_x precipitates and their associated dislocations are responsible for minority carrier traps in p-type silicon, characterized by two deep levels at E_C-0.17 and E_C-0.43 eV, leading to an increase of the leakage current. While in irradiated p-type silicon the majority traps related with carbon (interstitial carbon-substitutional carbon C_iC_s or interstitial carbon-interstitial oxygen C_iO_i complexes) dominates the leakage current, in n-type irradiated silicon this is the case for majority traps associated with vacancies (E-centres or di-vacancies). The implementation of an internal gettering step may also have a beneficial impact on the radiation hardness. The technological importance of these conclusions are for the moment being validated by evaluating the radiation hardening of a 1024x1024 CCD processed in a 1.25 µm CCD-CMOS technology.

Reduction of the bulk damage is important for the use of CCDs in a near-Earth space environment. A systematic study by Hopkinson /23/ concerning the radiation-induced dark current increase points out that the surface dark current increase due to ionization damage is bias dependent and shows a large reverse annealing effect, while the bulk damage generates dark current spikes and may introduce temporal fluctuation similar as RTSs. These RTSs, which have time constants up to 1 hour, are believed to be due to bistable lattice defects, i.e. defects with two stable configuration, corresponding to a different charge state.

It is also important to mention that beside technological modifications the radiation hardness can further be improved by optimizing the design. In addition, the radiation sensitivity also depends on the device operating conditions (e.g. operating bias, operating temperature, in-situ annealing affects).

3.3. Submicron CMOS Technologies

Bulk CMOS technologies are inherently more radiation sensitive than SOI technologies. However, typical features of commercial bulk CMOS devices are: total dose hardness >1 x 10^6 rad(SiO_2), dose rate upset hardness to 1 x 10^9 rad(Si)/sec, dose rate survivability to 1 x 10^{12} rad(Si)/sec, SEU hardness for flip-flops and SRAMs to 1 x 10^9 -1 x 10^{10} upsets/bit/day, and neutron fluence hardness to 1 x 10^{14} cm^{-2} /24/.

A further scaling of the devices to the deep submicron region requires the implementation of several advanced processing steps which will have an impact on the radiation hardness. Some of these technological process modifications are briefly discussed. The switching to so-called ultraclean processing in order to maintain the stringent material specifications concerning defects and contamination of the starting silicon has a beneficial impact on the radiation hardness. The use of thinner gate oxides results in a strong improvement of the radiation hardness as in general the irradiation-induced threshold voltage shift ΔV_t follows a power law with the gate oxide thickness t_{ox} /1/:

$$\Delta V_t \approx t^n_{ox} \qquad (2)$$

with n ranging between 1 and 3, depending on the oxide growth conditions. Ultrathin oxide (10-30 nm) have been reported to be harder than predicted by eq. (2), which

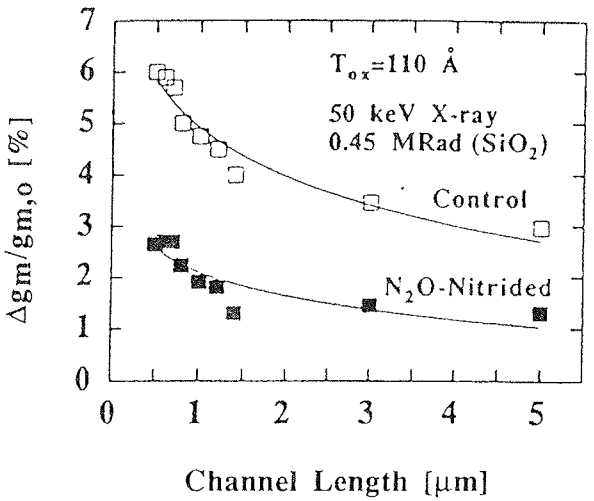

Figure 6: Comparison of the X-ray irradiation sensitivity of a standard and a N_2O-nitrided oxide. The normalized degradation of the peak transconductance is shown as a function of the effective device length /26/.
(dose rate 10 krad(SiO_2)/min).

might be due a compensation of the oxide trapped holes by tunnel electrons. For a complete picture one also has to take into account the impact of additives to the oxide growth ambient (e.g. Cl, F, Ar, N ...), the oxide growth temperature and the post-oxidation anneal conditions. Recent work even seems to indicate that threshold voltage shift due to oxide trapped charge is less oxide thickness dependent (n = 2.8) than the shift caused by the interface trapped charge (n = 4.3) /25/. Another beneficial influence on the radiation hardness of the gate oxides is the use of N_2O-nitrided (NO) /26/ or reoxidised nitrided (RNO) structures /27/, as illustrated in Fig. 6 for a NO oxide. Field oxides can be hardened by sandwich structures such as a P- or As-doped deposited oxide on a thin thermal oxide /28/. Modern transistors concepts such as Lowly Doped Drain (LDD) surely impacts the radiation hardness. Especially in the spacer regions irradiation-induced charge can be trapped.

3.4 Bipolar Devices

Irradiations degrade the common emitter current gain β of bipolar junction transistors by increasing the base current without significantly impacting the collector current This is caused by either displacement damage in the bulk reducing the minority carrier lifetime or by ionizing irradiation of the oxide covering the emitter-base junctions, whereby the oxide trapped charge results in a spreading of the field induced depletion layer in the base region and the interface traps increase the minority carrier surface recombination velocity /29/. The decrease in effective doping of the base of NPN transistors will be less pronounced for relatively heavy base doping as well as a very narrow base width. The effective surface recombination velocity versus the ionizing dose rate is illustrated in Fig. 7 /30/, showing very clearly that the surface recombination velocity not only increases with the total dose but also depends on the dose rate. While the highest values are observed for a low dose rate, there is a tendency to level off at high dose rates. A similar behaviour is noticed for the excess base current. Fig. 8 gives a typical behaviour of the current gain characteristics for various total dose levels /31/.

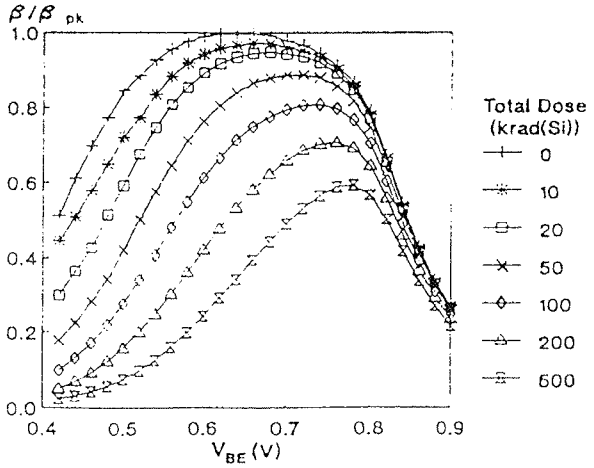

Figure 8: Typical common emitter current gain characteristics for various levels of total dose. The post-irradiation current gain is normalized to the peak pre-irradiation current gain β_{pk}, after Nowlin et al. /31/.

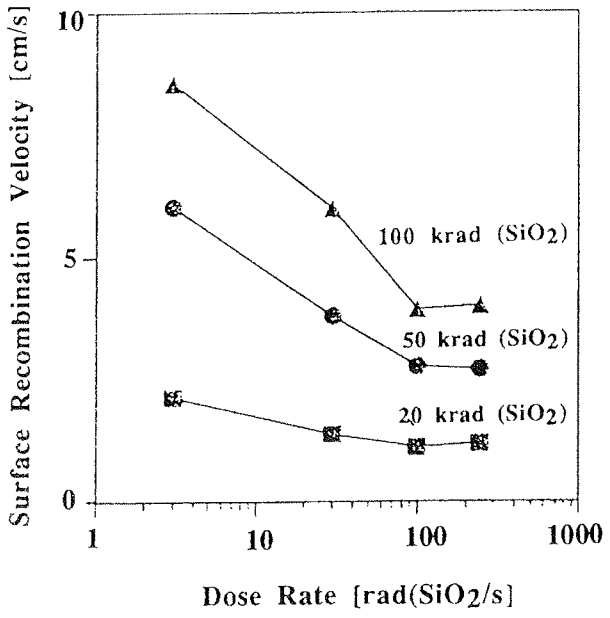

Figure 7: Variation of the effective surface recombination velocity calculated at a 0.6 V base emitter voltage versus the dose rate and for various total dose levels, after Wei et al. /30/.

A systematic study of different modern bipolar technologies leads to the following conclusion /31/: i) NPN transistors degrade more severe than PNP transistors, due to the build-up of positive charge in the oxide covering the base region, ii) devices with small emitter perimeter-to area ratios are less radiation sensitive than devices with a larger ratio, iii) the collector bias has no impact on the gain degradation, iv) the worst case irradiation condition is with a reverse bias on the emitter, v) large base-emitter voltages give a smaller increase in base current, and vi) poly emitter devices are initially harder than standard emitter devices, but are becoming worse at larger total doses. During the last years there is also a strong interest in SiGe HBTs because of their excellent electrical behaviour and their potential for cryogenic applications /32/. Recently, initial irradiation studies have been reported, indicating that up to a total dose of 1 Mrad(Si) these devices are radiation hard both at room temperature and at liquid nitrogen temperature /33/. However, at 77 K the behaviour of the base current is influenced by Poole-Frenkel trap assisted tunneling. Irradiations initially increase the tunnel base current, while there is a decrease for higher dose levels. Irradiations only have a limited influence on the low frequency noise behaviour by a slight increase of the generation-recombination centres resulting in a Lorentzian hump on the 1/f noise.

The authors have performed a systematic study of the impact of the quality of the starting silicon on the radiation hardness of junction diodes after a variety of proton, ^{252}Cf, electron, and neutron irradiations (see e.g./9-11, 34-36/). Some important conclusion have already been mentioned in section 3.2. The impact of different kinds of irradiation on the gated diode characteristics of one particular type of Cz n^+p junction diode is illustrated in Fig. 9. The shift of the gated diode step towards more negative gate voltage indicates a shift in the flatband voltage of the 100 nm thick gate oxide, due to the creation of ionization damage, i.e., trapped holes. The increase in the reverse current step after irradiation indicates the creation of interface traps, while the increase in the back-ground reverse current is mainly due to displacement damage in the substrate. From this figure, one can conclude that γ-irradiations predominantly cause ionization damage and negligible bulk damage, while the high energy particle irradiations (e^-, H^+) cause both.

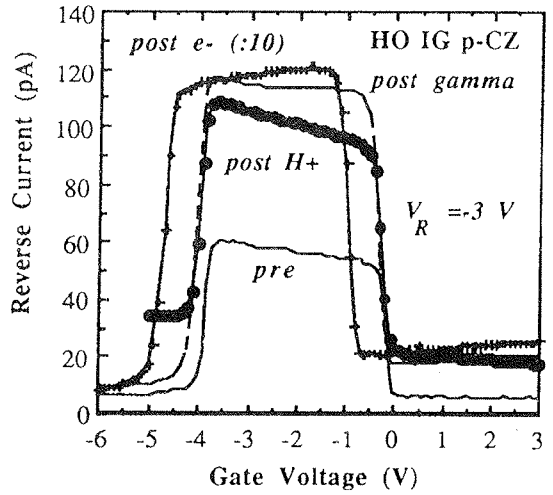

Figure 9: Gated diode characteristics before (full line) and after irradiation with:14 krad(Si) γ- (dash); 10 MeV 2x10^{10} H^+/cm^2 (circle) and 2 MeV 10^{13} e^-/cm^2. The reverse diode bias is -3 V.

In addition it can be stated that ^{252}Cf irradiations have a much higher defect generation efficiency than proton irradiations, but for the interpretation of the data one has to take into account the defect profile in silicon substrate. Detailed noise studies pointed out that the pre- and post-irradiation low frequency noise spectra can be described by a semi-empirical model

$$S_I = C\frac{I_F^B}{f^\gamma} \qquad (3)$$

with for proton irradiations $1.5 < B < 2$ and $0.65 < \gamma < 1.2$ for the diode current noise S_I. More information on the correlation between the irradiation-induced bulk damage and the LF noise performance can be found in /12/. It has to be remarked that the observed noise behaviour can not be explained by the standard available noise models.

The LF noise characteristics of electron irradiated diodes are somewhat peculiar as for FZ material the LF noise at low forward current levels decreases after irradiation. A theoretical model is under development and will take into account the relative importance of the surface G-R noise component and the noise associated with oxygen-related bulk G-R centres.

3.5 Other Technologies

There are still other silicon based technologies which are used for space applications and which have not been discussed here due to page restrictions. Junction field-effect transistors (JFETs) are less sensitive than MOSFETs as it is a bulk type device, with current conduction based on majority carriers. They are less sensitive to ionization bulk damage than bipolars. These devices are of special interest for detector front-end electronics in colliders as they are radiation tolerant and allow monolithic integration. Gamma irradiation levels up to 100 Mrad(Si) and neutron fluences in the range 4x10^{14} n/cm^2 have been reported /37/. Another promising approach for the fabrication of fully integrated pixel detectors is the use of high-resistivity (5-10 kΩcm) SOI wafers whereby the detector diodes are fabricated in the high resistivity substrate, while the CMOS read-out and amplification electronics are located in the thin silicon top layer /38/. A schematic cross-section of such a device is shown in Fig.10.

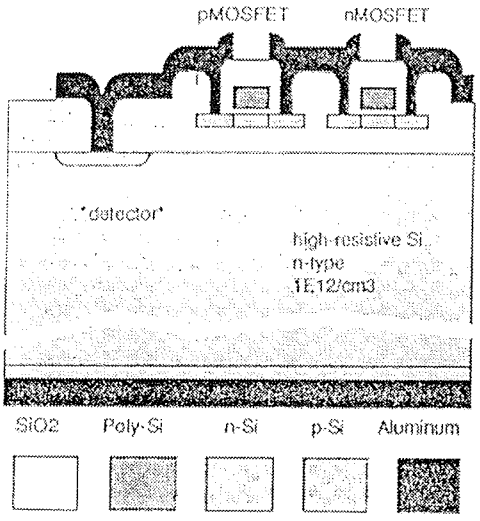

Figure 10: Schematic cross-section of the monolithic integration of CMOS electronics and particle diodes in high-resistiviy SOI wafers.

Special attention should be paid to the use of Power MOSFETs in radiation environments. Beside the standard MOSFETs deficiencies, an important phenomenon is the occurrence of Single Event Burnout (SED) result-

ing in a drain-source and drain-gate short. Important parameters to control are the operating voltages, the operating frequency, the applied voltage in the off state, and the operating temperature. It is essential to differentiate between the static and the dynamic operation of the devices and to take into account the irradiation parameters (e.g. type of particle, energy, stopping power, incident angle ...).

Finally it should be mentioned that there exists an increasing interest in the radiation hardness of sensor and/or microsystems due to their increasing functionality and fields of applicability. A discussion of that topic is out of the scope of the present paper.

4. CONCLUSIONS

It may be stated that silicon components remain the key electronic elements for space applications. This is mainly due to a better understanding of the physical mechanisms underlying the radiation hardness so that radiation resistant devices can be fabricated. This paper has only discussed the impact of technological parameters, but also on the design side there are plenty of measures that can be implemented. Only for dedicated applications, II-VI and III-V technologies are a competitor of the silicon technologies. During the last years the research efforts concerning radiation hardened technologies has been triggered and Europe is playing a more important and leading role.

ACKNOWLEDGMENTS

Part of this work has been performed with financial support from ESTEC, under contract No. 8515/90/NL/PM(SC). Although a large number of people have to be thanked for many stimulating discussion, special acknowledgment is given to J.P. Colinge, I. Debusschere, B. Dierickx, B. Johlander and L. Adams for their input and for the use of co-authored results.

REFERENCES

/1/ A. Holmes-Siedle and L. Adams, Handbook of Radiation Effects, Oxford Sci. Publ., 1993

/2/ C. Claeys, E. Simoen and J. Vanhellemont, Radiation Hardness Studies of Silicon Technologies for Space Applications, Electron Techn., 27, 3/4,1994, pp. 23-42

/3/ T.R. Oldham, F.B. McLean, H.E. Boesch Jr. and J.M. McGarrity, An Overview of Radiation-Induced Interface Traps in MOS Structures, Semicond. Sci. Techn., 4,1989, pp. 986-999

/4/ N.S. Saks and D.B. Brown, The Role of Hydrogen in Interface Trap Creation by Radiation in MOS Devices - A Review, in Proc. The Physics and Chemistry of SiO_2 and the Si-SiO_2 interface, Eds. C.R. Helms and B.E. Deal, Plenium Press, New York,1993, pp. 455-463

/5/ D.L. Griscom, Hydrogen Model for Radiation-Induced Interface States in SiO_2-on-Si Structures: A Review of the Evidence, J. Electronic Mat., 21, 7,1992, pp. 763-767

/6/ D.M. Fleetwood, Border States in MOS Devices, IEEE Trans. Nucl. Sci., NS-39,1992, pp. 269-270

/7/ D.M. Fleetwood, P.S. Winokur, R.A. Reber Jr., T.L. Meisenheimer, J.R. Schwank, M.R. Shaneyfelt and L.C. Riewe, Effects of Oxide Traps, Interface Traps, and 'Border Traps' on Metal-Oxide-Semiconductor Devices, J. Appl. Phys., 73,1993, pp. 5058-5074

/8/ C. Claeys and J. Vanhellemont, Radiation Effects in Bulk Silicon, Rad. Effects & Defects in Solids,127,1994, pp. 267-294

/9/ M.-A. Trauwaert, J. Vanhellemont, E. Simoen, C. Claeys, B. Johlander, L. Adams and P. Clauws, Study of Electrically Active Lattice Defects in ^{252}Cf and Proton Irradiated Silicon Diodes, IEEE trans. Nucl. Sci., 39, 6,1992, pp.1747-1753

/10/ J. Vanhellemont, A. Kaniava, E. Simoen, M.-A. Trauwaert, C. Claeys, B. Johlander, R. Harboe-Sörensen, L. Adams and P. Clauws, Generation and Annealing Behavior of MeV Proton and ^{252}Cf Irradiation Induced Deep Levels in Silicon Diodes, IEEE Trans. Nucl. Sci., 41, 3,1994, pp. 479-486

/11/ J. Vanhellemont, E. Simoen, C. Claeys, A. Kaniava, E. Gaubas, G. Bosman, B. Johlander, L. Adams and P. Clauws, On the Impact of Low Fluency Irradiation with Me V Particles on Silicon Diode Characteristics and Related Material Properties, IEEE Trans. Nucl. Sci., 41, 6,1994, pp. 1924-1931

/12/ C. Claeys and E. Simoen, Low Frequency Noise Diagnostics of Radiation Effects in Silicon Devices, in Proc. 13th Int. Conf. on Noise in Physical Systems and 1/f Fluctuations, Eds V. Bareikis and R. Katilius, World Scientific, Singapore, 1995, pp. 579-584

/13/ C. Claeys and E. Simoen, Noise Performance of Si Devices for Space Applications, in Proc. Int. NODITO Workshop on Noise and Reliability of Semiconductor Devices, Eds J. Sikula and P. Schauer, T.U. Brno, Czech Republic,1995, pp. 74-81

/14/ J.P. Colinge, Silicon-on-Insulator Technologies: Material to VLSI, Kluwer, Boston,1991

/15/ E. Simoen, U. Magnusson, G. Van den Bosch, P. Smeys, J.P. Colinge and C. Claeys, Adaptation of a Standard 1μm Double Layer Metal CMOS SOI Technology to Space Applications, in Proc. ESA Electronic Components Conference EECC'93, ESA Publication Division, Noordwijk, The Netherlands, ESA WPP-063,1993, pp. 295-300

/16/ E. Simoen and C. Claeys, Low-Frequency Noise Characterization of γ-irradiated Siliconon-Insulator MOSFETs, Nucl. Instr. Meth. B, 95,1995, pp. 75-81

/17/ J.P. Colinge, M.H. Gao, A. Romano-Rodriguez, H. Maes and C. Claeys, Silicon-on-Insulator "Gate-All-Around" MOS Device, Tech. Digest IEDM,1990, pp. 595-598

/18/ J.P. Colinge and A. Terao, Effects of Total-Dose Irradiation on Gate-All-Around (GAA) Devices, IEEE Trans. Nucl. Sci., 40,1993, 78-82

/19/ E. Simoen, C. Claeys, S. Coenen and M. Decreton, DC and Low Frequency Noise Characteristics of γ-Irradiated Gate-All-Around Silicon-on-Insulator MOS Transistors, Solid-State Electronics, 38,1,1995, pp.1-8

/20/ A. Simone, I. Debusschere, A. Alaerts and C. Claeys, Ionizing Radiation Hardening of a CCD Technology, IEEE Trans. Nucl. Sci., 39, 6,1992, pp.1964-1973

/21/ I. Debusschere, A. Sirnone, A. Alaerts and C. Claeys, Radiation Hardening of a CCD Technology Through Process and Design Modifications, Proc. ESA Symp on Photon Detectors for Space Instrumentation, ESA SP-356, Noordwijk, The Netherlands, 1992, pp. 281-284

/22/ I. Debusschere, C. Claeys, A. Simone and A. Alaerts, Optimization of the Ionizing Radiation hardness of a CCD Technology, Proc. 2nd ESA Electronic Conference, ESA WPP-063, Noordwijk, The Netherlands,1993, pp. 359-364

/23/ G.R. Hopkinson, Radiation-Induced Dark Current Increases in CCDs, in Proc. RADECS 93, Eds J.L. Leray and O. Musseau, IEEE no. 93TH0616-3,1994, pp. 365-372

/24/ Honeywell 1993 Product and Services Data Book

/25/ I. Yoshii, Radiation Effects on MOS Devices and Radiation-Hard CMOS Technologies, Nucl Instr. and Meth. A, 342,1994, pp.156-163.

/26/ G.Q. Lo, A.B. Joshi and D.L. Kwong, Radiation Hardness of MOSFETs with N_2O-Nitrided Gate Oxides, IEEE Trans. Electron Dev., 40, 8,1993, pp.1565-1567

/27/ Y-L Wu and J-G Hwu, Improvement in radiation Hardness of Reoxidised Nitrided Oxide (RNO) in the Absence of post-Oxidation Anneal, IEEE Electron Dev. Lett.,14, 1,1993, pp.1-3

/28/ K. Neumeier and H.P. Bruenner, Radiation Hard LOCOS Field Oxide, in Proc. RADECS 93, Eds J.L. Leray and O. Musseau, IEEE no. 93TH0616-3,1994, pp. 329-333

/29/ A. Hart, J. Smyth, V. van Lint, D. Snowden and R. Leadon, Hardness Assurance Considerations for Long-Term Effects on Bipolar Structures, IEEE Trans. Nucl. Sci. 25, 6,1978, pp.1502-1507

/30/ A. Wei, S.L. Kosier, R.D. Schrimpf, D.M. Fleetwood and W.E. Combs, Dose-rate Effects on Radiation-Induced Bipolar Junction Transistor Gain Degradation, Appl. Phys. Lett., 65,15,1994, pp.1918-1920

/31/ R.N. Nowlin, E.W. Enlow, R.D. Schrimpf and W.E. Combs, Trends in the Total-Dose Response of Modern Bipolar Transistors, IEEE Trans. Nucl. Sci., 39, 6,1992, pp. 2026- 2034

/32/ J.D. Cressler, Status and Trends in the Cryogenic Operation of SiGe Bipolar Technology, in Proc. Low Temperature Electronics and High Temperature Superconductivity, Eds. C.L. Claeys, S.I. Raider, R.K. Kirschman and W.D. Brown, Electrochem. Soc. Ser., Pennington, PV 95-9,1995, pp.159-177

/33/ J.A Babcock, J.D. Cressler, S.D. Clark, L.S. Vempati and D.L. Harame, The Effect of Ionizing Radiation on SiGe HBTs Operated at 77 K, in Proc. Low Temperature Electronics and High Temperature Superconductivity, Eds. C.L. Claeys, S.I. Raider, R.K. Kirschman and W.D. Brown, Electrochem. Soc. Ser., Pennington. PV 95-9, 1995, pp. 221-231

/34/ J.P Dubuc, E. Simoen, P. Vasina and C. Claeys, The Low Frequency Noise Behavior of High-Energy Electron Irradiated Si n+p Junction Diodes, IEE Electron Letters, vol. 31, no.12,1995, pp.1016-1018

/35/ E. Simoen, J.P. Dubuc, J. Vanhellemont and C. Claeys, Impact of the Starting Interstitial oxygen Concentration on the Electrical Characteristics of Electron-Irradiated Si Junction Diodes, in the Proc. EMRS 95 Meeting, Symp. on "Carbon, Hydrogen, Nitrogen and Oxygen",1995, (in press)

/36/ H. Ohyama, J. Vanhellemont, E. Simoen, C. Claeys, Y. Takami, K. Hayama and H. Sunaga, Substrate Effects on the Degradation of Irradiated Si Diodes, in Proc. RADECS '95, Arcachon, France, Sept.18-22,1995 (in press)

/37/ C. Cesura and V. Re, Effects of γ-Rays and Neutrons on the Noise Behavior of Monolithic JFET Circuits, in Proc. RADECS 93, Eds J.L. Leray and O. Musseau, IEEE no. 93TH0616-3,1994, pp. 349-354

/38/ B. Dierickx et al., Integration of CMOS Electronics and particle Detector Diodes in High-Resistivity Silicon-on-Insulator Wafers, IEEE Trans. Nucl. Sci., 40, 4, 1994, pp. 753-758

Prof. dr. Cor Claeys
Dr. Eddy Simoen
Dr. Jan Vanhellemont
IMEC
Kapeldreef 75
B-3001 Leuven
Belgium
Tel : 3216 281328
Fax : 3216 281214
Claeys@ imec.be

Prispelo (Arrived): 05.09.95 *Sprejeto (Accepted): 03.10.95*