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ASPECTS OF REALIZATION OF BURIED CAPACITORS IN THICK FILM MULTILAYER CIRCUITS

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Key words: electronic circuits, thick film multilayer circuits, buried capacitors, thick film capacitors, miniaturization of electronic circuits, three dimensional circuits, packing density, capacitor properties, high-K dielectrics, multilayer dielectrics, temperature dependence, firing process, refiring, hybrid circuits

Abstract: To improve the position of thick film hybrids against conventional printed circuits built up in fine line technology attention has to be spent to increase the packing density of hybrid circuits by means of further miniaturization of thick film components or by applying multilayer technique.

Besides conductors and insulating layers, passive components like resistors and capacitors can be produced in thick film technique. This paper discusses the properties of different high-K dielectrics applied for capacitors embedded in multilayer structures. The dielectric is usually exposed to multiple firing cycles during the production process. Interactions between the high-K dielectric, the multilayer dielectric, and the electrode have to be expected. Finally, all these effects govern the performance characteristics of the embedded capacitors.

Načini izvedbe pokopanih kondenzatorjev v debeloplastnih večnivojskih hibridnih vezjih

Ključne besede: vezja elektronska, vezja debeloplastna večplastna, kondenzatorji zakriti, kondenzatorji debeloplastni, miniaturizacija vezij elektronskih, vezja trodimenzionalna, gostota pakiranja, lastnosti kondenzatorjev, dielektriki z visokim K, dielektriki večplastni, odvisnost temperaturna, proces žganja, žganje ponovno, vezja hibridno

Povzetek: Standardnim tiskanim vezjem izdelanim z veliko gostoto povezav morajo debeloplastna hibridna vezja konkurirati tako, da stalno povečujemo gostoto elementov na enoto površine. To dosegamo bodisi z nadaljno miniaturizacijo komponent na vezju ali pa z uporabo večnivojskih povezav in pokopanih komponent.

Poleg prevodnih in izolacijskih plasti na hibridnem vezju znamo izdelati tudi debeloplastne pasivne komponente kot so upori in kondenzatorji. V prispevku opisujemo lastnosti različnih dielektrikov, ki jih uporabljamo za izvedbo pokopanih kondenzatorjev v večnivojskih strukturah. Dielektrik je ponavadi izpostavljen večkratnim temperaturnim obdelavam med tehnološkim procesom. Vsled tega lahko pričakujemo interakcije med dielektrikom za kondenzatorje, izolacijskim dielektrikom za večnivojske povezave in elektrodo. V končni fazi določajo vsi ti procesi končne električne lastnosti pokopanih kondenzatorjev.

1. INTRODUCTION

To improve the position of thick film hybrids against conventional printed circuits built up in fine line technology attention has to be spent to increase the packing density of hybrid circuits by means of further miniaturization of thick film components or by applying multilayer technique. Beside conductors and insulating layers, passive components like resistors and capacitors can be produced in thick film technique. Capacitors on the other hand are usually attached as SMDs to the circuit. Thick film capacitors are commonly realized in a plate configuration. Modified ferroelectric materials with low sintering temperature have to be selected as high-K dielectrics for thick film applications. Dielectrics on the base of $BaTiO_3$ or relaxor ceramics are already available appropriate for thick film processing /1,2/. The ferroelectric ceramic material exhibits a high porosity which induces a high sensitivity to humidity. For protection purpose thick film capacitors have to be sealed by a two layered glass or a polymer coating. But the electrical performance of this high-K dielectric is also affected by chemical reactions between the fluxes and the binder system of the applied conductor paste and the ferroelectric phase. These reactions are often reflected by a low K-phase which lowers the effective capacitance. Beyond that a thick film capacitor in a plate configuration covers a larger substrate area than a conventional

chip capacitor of the same capacitance value. Especially the last factor is the reason for the only restricted practical application of thick film capacitors.

As an approach to a further miniaturization of thick film circuits it must be considered to integrate thick film components in the inner layer of multilayers. In this manner the area on the surface of the circuit usually provided for passive components will be reduced. Actually a three dimensional circuit module will be built up. Several papers deal with the integration of resistors inside a multilayer structure. Usually already small deviations from the nominal resistance value are already critical for the circuit performance. The process dependent resistance drift of buried resistors cannot be adjusted by a trimming process as easily as usual. On other side for many applications capacitors of very tight tolerances are not required. With regard to increase the packing density of circuits it seems practicable to bury capacitors inside a multilayer structure. Besides, no additional passivation of the high-K dielectric is necessary. In turn, electrical properties of the high K-dielectric are sensitive to the processing conditions, especially to the firing in the presence of conductors and multilayer dielectrics. According to technical reports it is well documented that the permittivity increases as the silver content of the electrode material increases /1/. This must be related to the lower binder content of Ag-conductors in comparison to conventional PdAg-conductors. To prevent silver migration the application of a buffer dielectric is recommmended often.

This paper discusses the properties of different high-K dielectrics applied for capacitors embedded in multilayer structures. The dielectric is usually exposed to multiple firing cycles during the production process. Interactions between the high-K dielectric, the multilayer dielectric, and the electrode have to be expected. Finally, all these effects govern the performance characteristics of the embedded capacitors.

2. EXPERIMENTAL

2.1 Test structure

Constituents which are not part of the high-K dielectric may diffuse into the embedded capacitor in two ways: One is peripherally from around the electrode, the other through or from the electrode. The sum of these effects affects the properties of the capacitors. The performance of the buried capacitors has to be evaluated with regard to two aspects: The actual capacitance value and the temperature dependent performance of capacitors.

High-K capacitors are usually found in applications where operation is nearer room temperature, a Q as low can be tolerated and the exact capacitance value is not critical. Bypass and many coupling applications, for instance, often need only a minimum capacitance value for proper operation. For some of these applications even Z5U can be used over the full -55°C and 125°C temperature range, as long as their application requires only the minimum capacitance obtained at the temperature extremes. The dielectric constant at these temperature extremes is often still more than that of the more stable but intermediate-K materials.

The topic of this study deals with the specification of parameters affecting the change of performance characterics of high-K thick film dielectrics. Interdigitated capacitor samples overprinted with the selected dielectric have been prepared to eveluate their dielectric behavior /3/. The finger test structure is quite better suited than the conventional plate configuration to specify the contribution of different material interaction effects by means of capacitance measurements. The total capacitance of the interdigital pattern results from stray fields inside the alumina substrate and the applied dielectric. If the dielectric is applied in an appropriate thickness the stray field of the finger capacitor develops inside the layer (Figure 1a) otherwise a certain fraction of the stray field protrudes the surface of the deposited dielectric which reflects a lower total capacitance (Figure 1b).

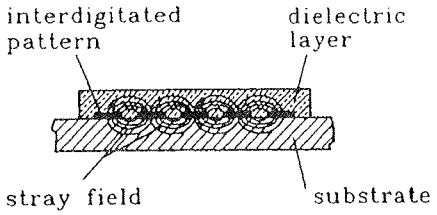


Figure 1a

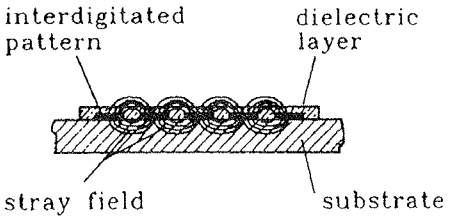


Figure 1b

Fig. 1a-b: Distribution of stray fields

Standard thick film techniques were employed to prepare capacitor test samples on 96% alumina substrates. Table 1 lists the materials used in this study.

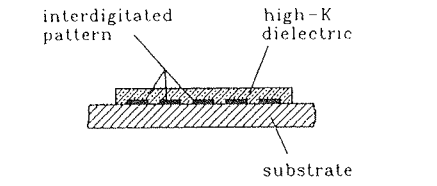
Multilayer system:	Conductor (metal type)	High-K dielectric (K at 1kHz)	Multilayer Dielectric	Buffer
DuPont	QS 170 (AgPt)	5540 (6000)	QM42	5520
ESL	D9516 (AgPt)	4210 (10000)	4913	-

The capacitor structure consists of the interdigital conductor pattern, followed by two, up to four layers of dielectric. Conductors were printed with a 325 mesh screen coated with a 20μm thick emulsion. Dielectrics were applied with a 200 mesh screen with an emulsion

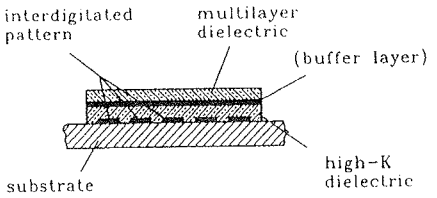
thickness of 30μm. After printing each paste was dried for 10 minutes at 150°C before firing. The firing was conducted in a belt furnace with cycle duration of 60 minutes and 10 minutes at peak temperature of 850 °C. All layers were separately fired. The target fired thickness of the high-K dielectric was 70 to 80 μm. The thickness of the multilayer dielectric was 40 or 80μm respectively.

Due to the geometrical proportions of the gap width between the electrodes (150 μm) and the thickness of the dielectric (80 μm) the total capacitance becomes sensitive to any additionally applied layer with differing permittivity (Figure 1b). To evaluate the influence of multilayer compositions on the performance of the high-K dielectric, batches of different samples with varying sequences of layer deposition have been prepared (Figure 2):

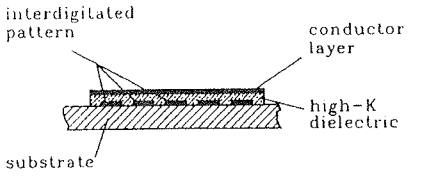
Arrangement A: electrode pattern overprinted by high-K dielectric (thickness: 70-80μm).



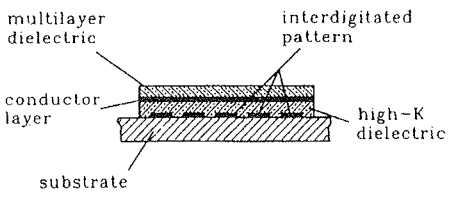
arrangement A



arrangement B



arrangement C



arrangement D

Fig. 2: Arrangement in layers

Arrangement B: structure identical with arrangement A, but overprinted - if necessary - with a buffer-layer (thickness: 20μm) and multilayer dielectric (thickness: 40μm or 80μm).Arrangement C: structure identical with arrangement A, but overprinted with a conductor layer.

Arrangement D: structure identical with arrangement C, but covered with multilayer dielectric (thickness: 80μm).

The printed areas of all applied layers are identical.

2.1.1. Results

Capacitance and dissipation factor were measured with a HP4192A impedance analyser. Measurements were carried out using an automated equipment over the temperature range -55°C -125°C realized by a thermostream (Froilabo).

The performance of dielectrics is characterized by a change on capacitance. In order to specify the interaction effects and to compare the performance of different high-K dielectrics a normalized graphical representation for the capacitance shift at a frequency of 1kHz has been selected. Figure 3 shows the temperature characteristics for the high-K dielectrics under investigation (arrangement A, Figure 2).

The maximum of the capacitance curve (Curie-temperature) shifts from 5°C to 35°C and the curve becomes broader as the high-K dielectric of the Du Pont system

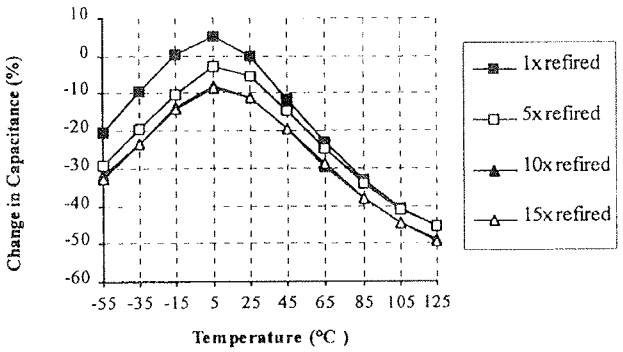


Figure 3a-DuPont

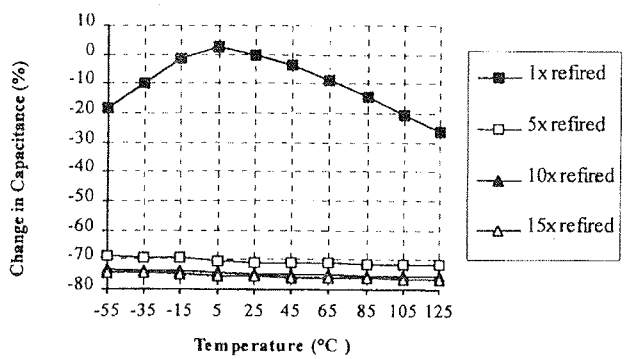


Figure 3b-ESL

Fig. 3: Temperature dependence of capacitance.

is overprinted by the buffer layer as well as by the multilayer dielectric (thickness: 40 μm) according to arrangement B (Figure 2 and Figure 4). Due to the dilution of the ferroelectric phase the capacitance drops slightly (within 10%) if an additional layer of multilayer dielectric (total thickness of multilayer dielectric: 80μm) is applied.

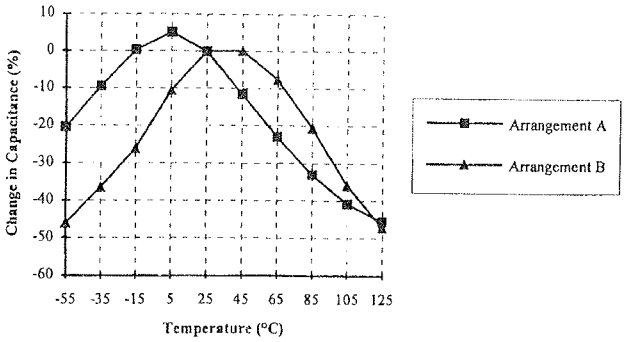


Fig. 4: Influence of buffer and multilayer dielectric on the temperature characteristic of a high-K dielectric.

According to the processing conditions of thick film multilayers test samples with a different arrangement of layers (Figure 2) have been exposed to multiple firing cycles in order to evaluate the sensitivity of the high K-dielectric to refiring. Figure 5 depicts the changes in capacitance versus additional firings.

The ESL high-K dielectric exhibits fairly large shifts especially upon the first five refiring cycles (arrangement A). The considered refire shifts in capacitance are negative. The capacitance response of arrangement D to extra firing must be related to two opposite effects: The refiring process contributes to an increase of capacitance (arrangement C), as well as to a drop of capacitance on behalf of the sensitivity of the high-K dielectric to refiring (arrangement A). The net effect is the sum of these. The sum can be positive or negative depending on their effectiveness. Migration of electrode material during firing might be a plausible reason for the increase on capacitance of the Du-Pont-composition and the ESL paste system because a further densification of the dielectric could not be detected. Measuring the dielectric thickness before and after refiring cycles showed no change.

The temperature characteristic of arrangement B for the Du Pont system shows evidently an interaction between

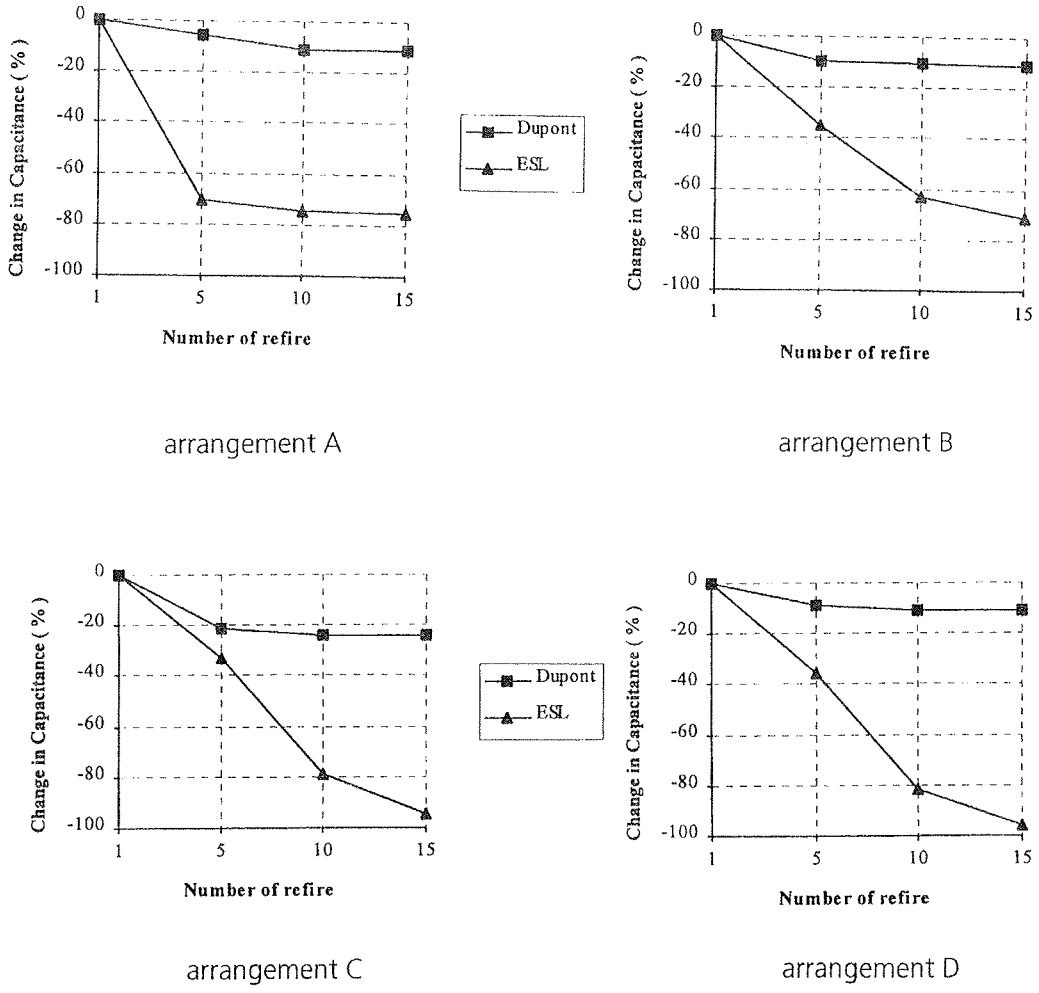


Fig. 5: Change in capacitance in dependence of refiring cycles.

the dielectric layers (Figure 6) due to extra firings which results in a further shift of the Curie temperature.

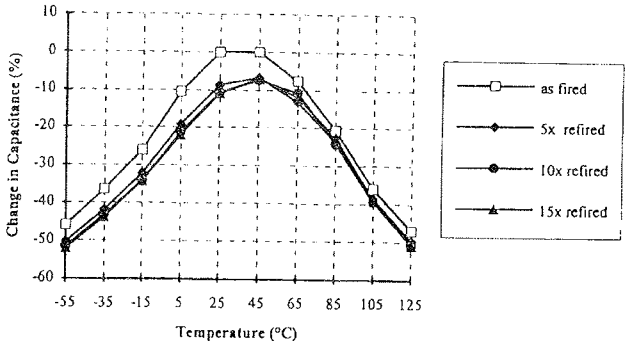


Fig. 6. Shift of temperature characteristic due to extra firing.

2.2. BURIED CAPACITORS

In a next step of the study the viability of realizing buried capacitors will be demonstrated by application of the Du-Pont-system and the ESL-paste- system. To get familiar with the size dependent aspects of capacitance shift, capacitor arrays built up on two substrates by a bottom plate of 22mm x 36mm and square parallel top plates capacitor structures of 2mm x 2mm, 3mm x 3mm, 4 x 4 mm, 5 mm x 5 mm, 6 mm x 6 mm, 8 mm x 8 mm, 10mm x 10mm and 12 mm x 12 mm have been produced. Two types of samples have been prepared: Samples of type A have been placed on the substrate followed by firing a buffer layer (only for the Du-Pont-system) and a multilayer dielectric on top (Figure 7). The capacitor arrays of type B were placed on the multilayer dielectric or on the buffer layer, respectively (Figure 8). No additional layer on the top of the capacitors has been applied. The multilayer as well as the high K-dielectric were printed in two layers using a 200 mesh screen. The thickness of the high-K dielectric is 48 μm for the Du-Pont-system and 55 μm for the ESL-system. To simulate the processing conditions of multilayer circuits, the samples were exposed up to ten additional firing cycles. Figure 9 and Figure 10 depict changes in capacitance versus temperature with varying number of firings for samples of type A with and without buffer layer. Samples built up with a buffer layer show a pronounced shift of Curie-temperature with additional firings. Besides that, lower capacitance values will be realized. They exhibit also a low stability to refire process. For samples of type B the peak of capacitance at Curie-temperature is flattened drastically with an increasing number of firing cycles (Figure 11). The typical temperature dependence characteristic for ferroelectrics is lost as an additional buffer layer is applied. The capacitance values as well as the refire stability of these samples are low.

The ESL-high K dielectric shows a characteristic relaxor behavior (Figure 12). Capacitors of type A, built up with this paste yield high capacitance values with an excellent refiring stability (Figure 13). In the contrary the refiring stability of the capacitors of type B is only poor (Figure 14).

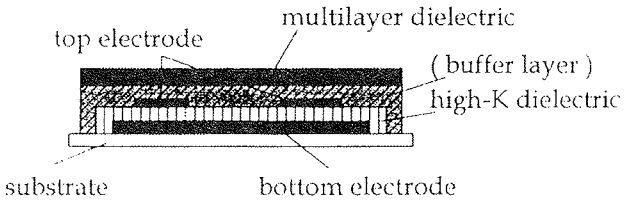


Fig. 7: Sample type A

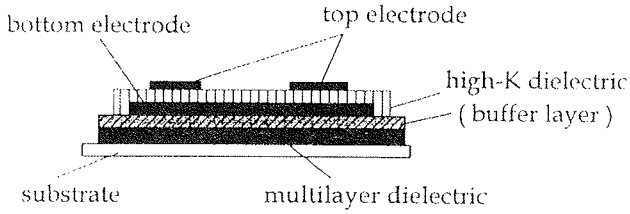


Fig. 8: Sample type B

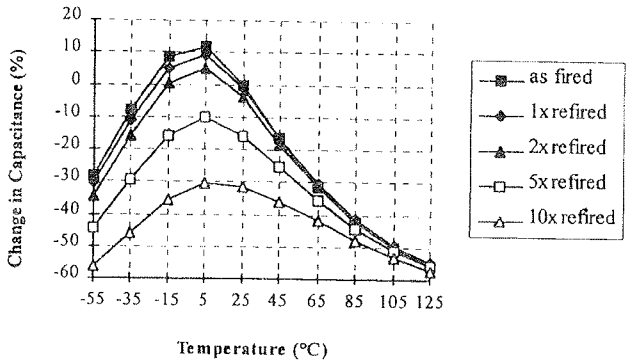


Fig. 9: Capacitance change due to additional firings: sample type A without buffer

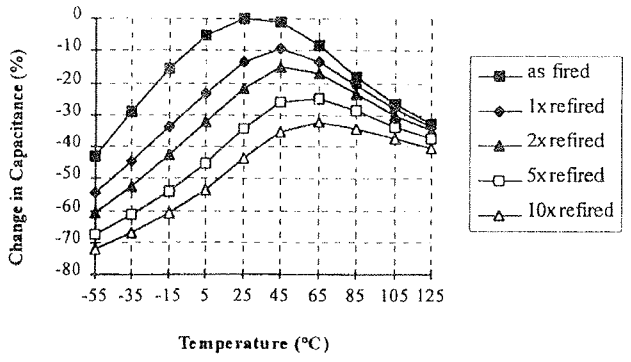


Fig. 10: Capacitance change due to additional firings: sample type A with buffer

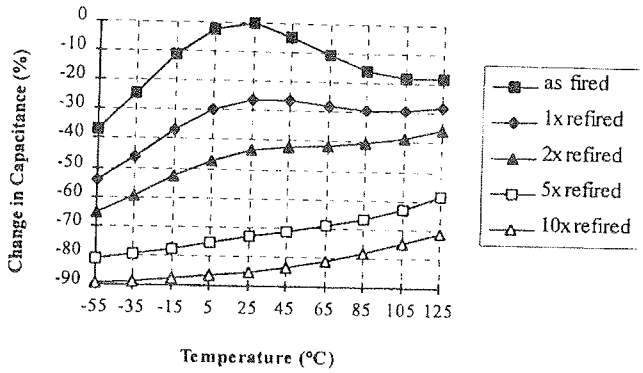


Fig. 11. Capacitance change due to additional firings: sample type B

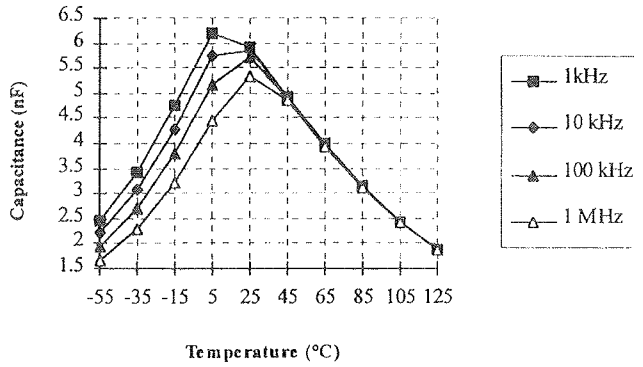


Fig. 12: Temperature dependence of capacitance (relaxor behavior)

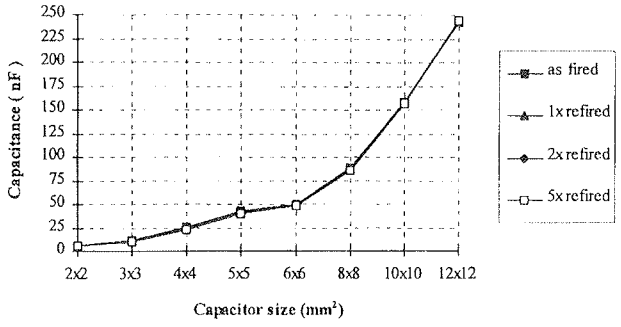


Fig. 13: Capacitance change due to additional firings for samples type A

The capacitance shift of capacitors of type A, independent of the employed paste system, becomes greater as the capacitor size is reduced (Figure 15). This must be related to a peripheral diffusion because the silver electrodes form a nearly impenetrable barrier for diffusion. Therefore the diffusion becomes more effective as the area to circumference ratio of the electrodes becomes smaller. In contrary the capacitance shift of capacitors of type B is increasing with capacitor size for devices of small dimensions or nearly constant for capacitors of larger geometrical proportions (Figure16).

There is evidently a strong interaction from the multilayer dielectric through the bottom electrode. This effect is increased by applying the buffer layer for the Du-Pont system.

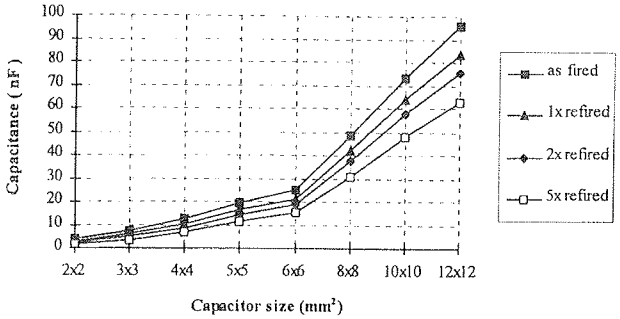


Fig. 14: Capacitance change due to additional firings for samples type B

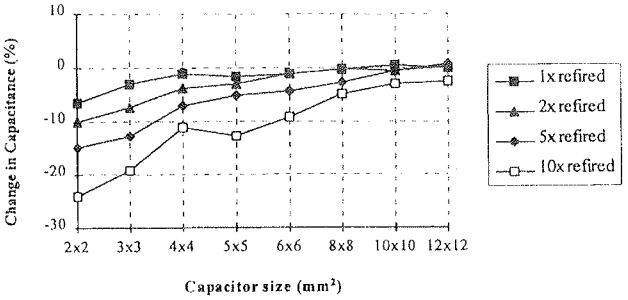


Fig. 15: Capacitance shift due to additional firings: type A (ESL)

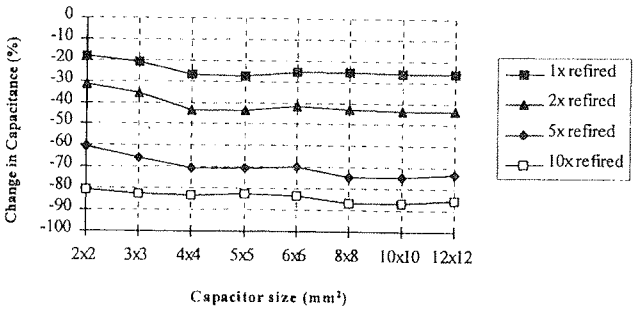


Fig. 16: Capacitance shift due to additional firings: type B (DuPont)

3. Summary

The fabrication of thick film capacitors integrated in multilayer structures is very critical due to the sensitivity of high-K dielectrics to multiple firings and to diffusions. Based on our study it is possible to realize buried capacitors in tight tolerances. The buried capacitors have to be placed immediately on the substrate. This

arrangement minimizes the influence of repeated firing cycles on the stability of performance of integrated capacitors. The integration of capacitors in multilayer structures is a viable method to increase the packaging density of thick film hybrids.

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