DRIVER CIRCUIT FOR AN AUTOMOTIVE SMART POWER SYSTEM CHIP

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Key words: microelectronics, automotive electronics, smar power technology, semiconductor chips, system chips, reliable operation, electronic circuits, driver circuits, warning lamps

Abstract: A driver circuit is presented as part of a system chip fabricated in a smart power technology. In automotive applications like anti brake control systems or airbag control units any malfunctions, detected by internal diagnostic circuits, are reported to a warning lamp. The requirements for this lamp driver and the circuit realization are presented in detail. Special efforts are done to keep the driver circuit operational also under worst case supply voltage conditions.

Krmilna elektronika za inteligentno močnostno sistemsko integrirano vezje avtoelektronike

Ključne besede: mikroelektronika, elektronika avtomobilska, tehnologija močnostna inteligentna, čip-i polprevodniški, čip-i sistemski, delovanje zanesljivo, vezja elektronska, vezja gonilna, lučke opozorilne

Povzetek: V prispevku predstavim krmilno elektroniko kot del sistemskega integriranega vezja izdelanega v inteligentni močnostni tehnologiji. Pri uporabi v avtoelektroniki, npr. za nadzor delovanja ABS ali za nadzor delovanja sistema zračne blazine, mora biti vsaka napaka, ki jo odkrije notranje diagnostično vezje, signalizirana z opozorilno lučko. V tem prispevku natančno opišem zahteve, kakor tudi izvedbo elektronike za krmilnik lučke kot dela večjega sistemskega integriranega vezja. Posebno pozornost sem posvetil obnašanju krmilnega vezja pod najhujšimi pogoji delovanja napajalne napetosti.

1. INTRODUCTION

Today's suppliers of automotive electronic units are going to prefer a system-on-a-chip approach to achieve the ever increasing reliability requirements. Smart Power technologies make it possible to combine parts of the logic, the power drivers and the analog diagnostic functions on one chip. Special efforts are necessary to obtain the right diagnostic functions also under external failure conditions. A bad condition - from the point of view of the circuit designer - is the condition of broken supply wires. How to consider this restriction in designing a driver circuit for a warning lamp is described in detail.

2. SMART POWER TECHNOLOGY

The system chip is realized in a power BiCMOS Technology. The cross section of some devices is shown in fig. 1.

Based on a p^-substrat and a n^-doped epitaxial layer it offers a combination of a high voltage DMOS device and low voltage bipolar (npn and pnp) and CMOS devices. The current path in the power device is vertical but the drain connection is brought to the surface via a buried layer and sinkers, also called an updrain configuration. The low voltage p-channel and n-channel transistors allow the integration of medium complexity CMOS logic

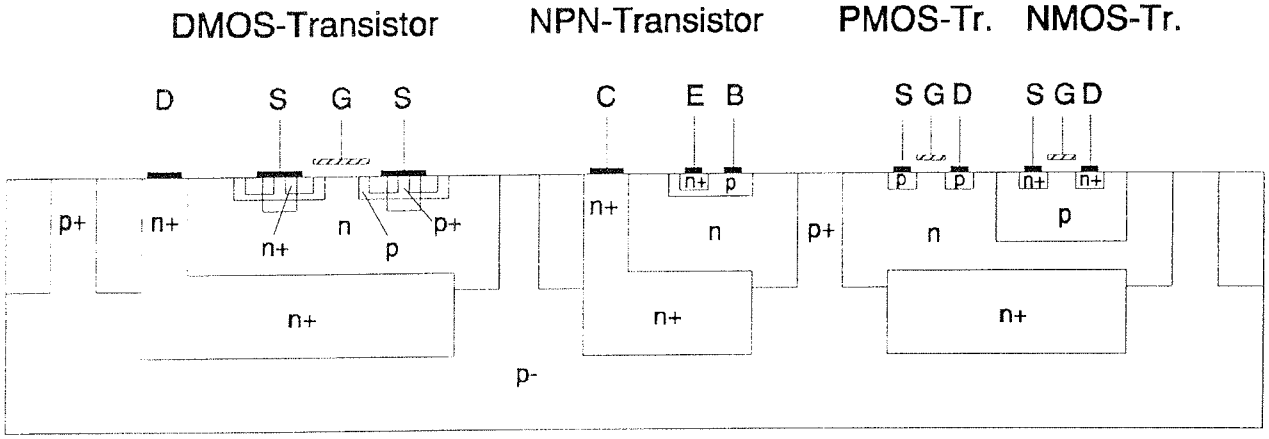

Fig. 1: Cross section of the Smart Power Technology

parts into the power switches. The bipolar transistors are provided for the analog circuits due to their better characteristics like noise, offset and drift behavior.

The use of this technology enables the system integration of the airbag power chip. The DMOS is used as power device to switch currents in the range of few amps, the low voltage CMOS components enable the realization of logic parts. The bipolar components are important for designing the analog functions where maximum precision is required.

3. BLOCK DIAGRAM OF AN AUTOMOTIVE SYSTEM CHIP

The typical configuration of an automotive system chip is shown in fig. 2. The smart power technology allows it to integrate all functions except the microprocessor on one chip. It includes power outputs to drive the application specific loads and analog diagnostic circuits which are responsible for testing the internal circuits and the external components. All diagnostic information are summed up and lead to an output which drives a lamp. This warning lamp is suited in the dashboard of the car. It is switched on for a short time when you start the car and then - if everything is okay - it will be switched off. In case of any error of the system this warning lamp will be switched on again. Because the driver circuit of this warning lamp has to do its job very reliably, it was chosen to be presented in more detail.

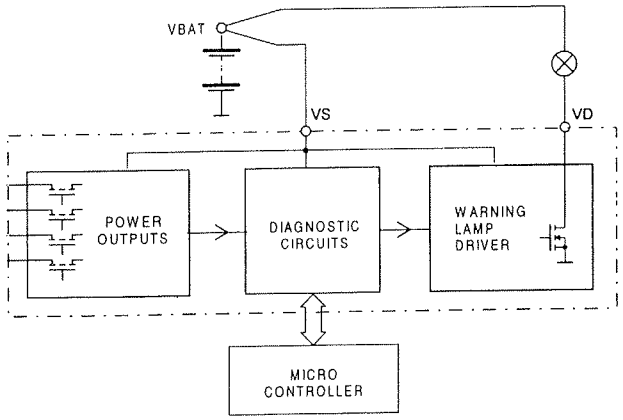

Fig. 2: Block diagram of a smart power system chip

loosing the battery connection (VS in fig.2) to the module should result in an activated lamp. The driver circuit itself has also to be short circuit protected. Therefore current limiting and overtemperature protection are required.

5. CIRCUIT REALIZATION

A block diagram of the lamp driver circuit is shown in Fig. 3. Under normal supply voltage conditions the load RL is fed by the voltage VBAT, whereas the logic and the gate driver circuits are supplied with VS. Now we assume the following error condition: The voltage VS is missing but the voltage VBAT exists. In that case the lamp should be switched on. This would report the error condition of the missing VS because all errors are reported by switching on the lamp - normally by the logic circuit. But the logic circuit is now missing its supply voltage! To achieve the desired function, the gate voltage has to be captured from VBAT via the load. It would be no problem when the DMOS is switched off. But the switched on DMOS does not provide a sufficient voltage VD at its drain to supply the circuits. The target is to develop a gate driver circuit which can manage this condition. This is done by two essential steps: First a charge pump is used to multiply the low voltage VD to an adequate level. And second a regulation circuit controls the saturation voltage VD in that way, that it will not drop below a minimum value which is necessary as operation voltage for the charge pump. Additionally the design of the overload protection circuit has to accept a low voltage VD as supply voltage.

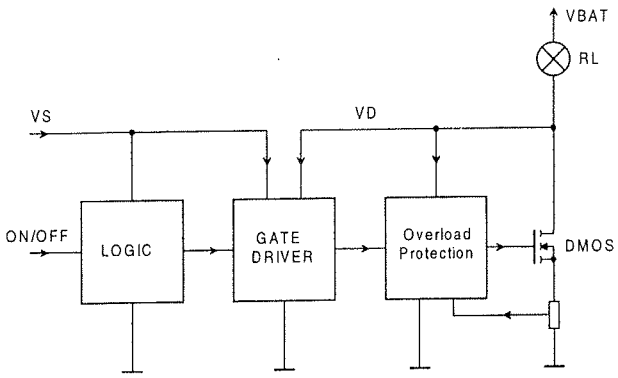

Fig. 3: Block diagram of the lamp driver circuit

4. REQUIREMENTS FOR THE LAMP DRIVER CIRCUIT

The purpose of the warning lamp is to report any malfunction of the electronic system to the car driver. The summary of the status from all internal diagnostic circuits is used as logic input for the lamp driver. In case of an error the lamp has to be switched on. Under normal supply voltage conditions this task is not a challenge to the circuit designer but it is the no-supply-voltage condition which results in a new circuit design:

A more detailed circuit diagram is shown in fig. 4. The gate voltage of the DMOS is supplied either via VS or via VCP, the output voltage of the charge pump. The input voltage of the charge pump is supplied from VD, the drain voltage of the power DMOS. A bias circuit, formed of the devices Q1 to Q4 generates a stabilized current IB which is mirrored to supply the charge pump and the regulation circuit. To keep the bias circuit operating, the voltage VD should not drop below the value of two VBE-voltages. The regulation part controls it in that way: The DMOS gate is charged by the current I8

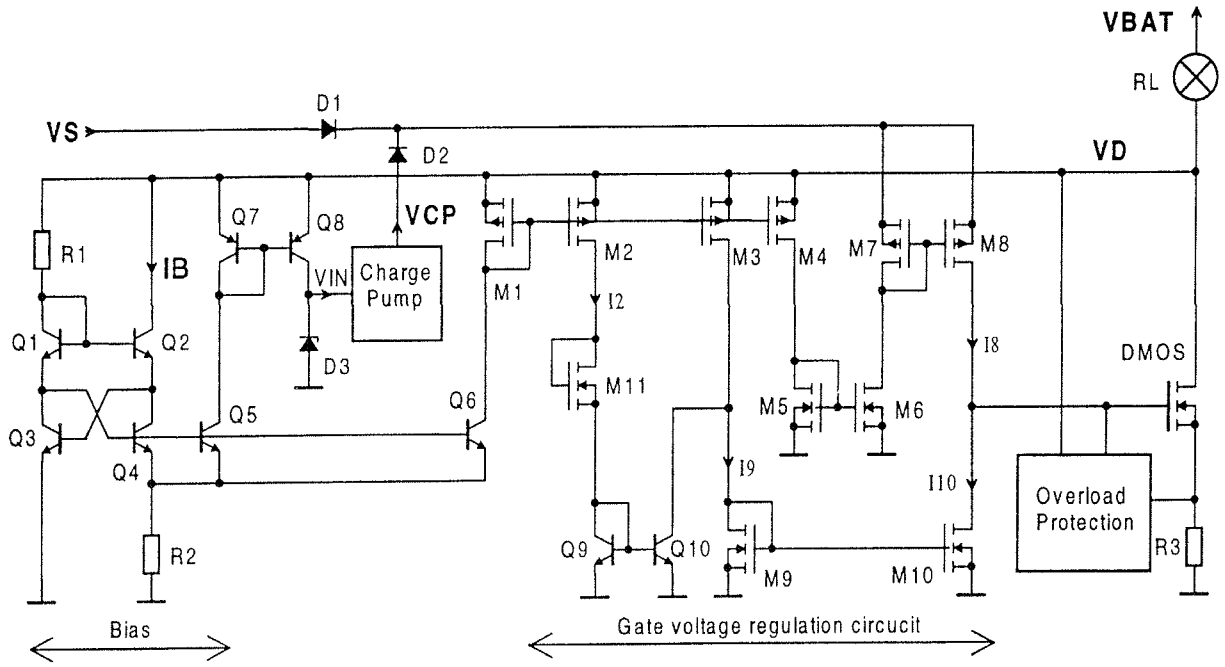

Fig. 4: Circuit diagram of the lamp driver circuit

and discharged by the current I10. The discharging current is cut off by means of Q10, so the DMOS will remain switched on. If the drain voltage VD decreases a point will be reached where the current I2 becomes zero. Then the current I9 and -correspondingly - I10 will increase. This leads to a state, where I8 is equal to I10 as a stable operating point. The relative huge gate capacitance of the DMOS acts as a sufficient loop compensation of this regulation circuit. The final voltage of VD is defined by the voltage drops of M11 and Q9. In practice it is about 2 V which is high enough to feed the bias circuit and the charge pump. On the other hand it is low enough to be accepted as a drain to source voltage drop of the DMOS.

The charge pump circuit is shown in fig. 5. To achieve the required gate voltage a multiple stage design was chosen. The five inverter stages are directly connected in a feedback loop as a ring oscillator, therefore no additional oscillator is necessary.

The overload protection circuit is shown in fig. 6. It provides current limiting and temperature protection of the DMOS. The bias generator is the same as shown in fig.4. The current I2 is defined by $I2 = \Delta VBE / R2$.
ΔVBE is given by comparing Q1 + Q4 with Q2 + Q3:
$\Delta VBE = Vt \cdot [\ln(AreaQ1) + \ln(AreaQ4) - \ln(AreaQ2) - \ln(AreaQ3)]$
$Vt = kt/q$ depends on the absolute temperature, so the bias circuit actually is a so called PTAT source, that means the current is **p**roportional **t**o the **a**bsolute **t**emperature. Adding the current mirror Q7, Q11 and the devices R4, Q14 completes the circuit to a temperature shutoff block. The voltage drop across R4 is increasing with temperature. Compared with the decreasing VBE-characteristic of the bipolar device Q14 it results in a well defined temperature switch off point.

Current limiting is the second task of the shown circuit. The current threshold is defined by the Δ VBE of Q15 and Q16, compared with the voltage drop on R3. The shunt resistor R3 is part of the metal interconnect layer,

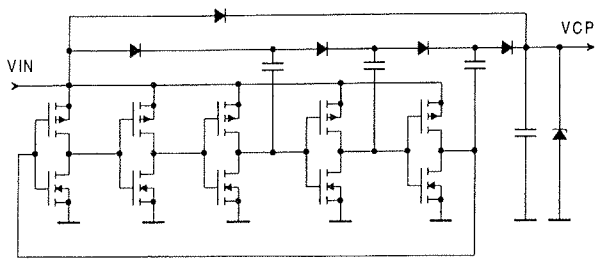

Fig. 5: Charge pump circuit

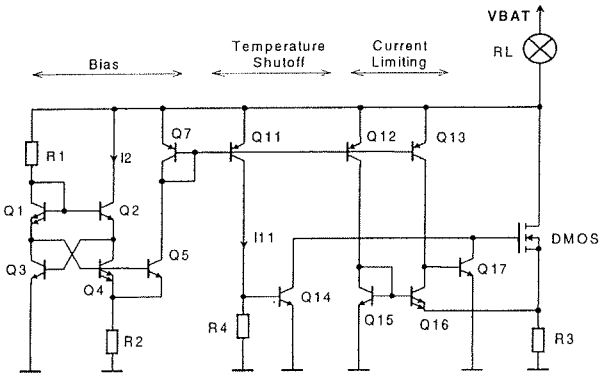

Fig. 6: Overload protection circuit

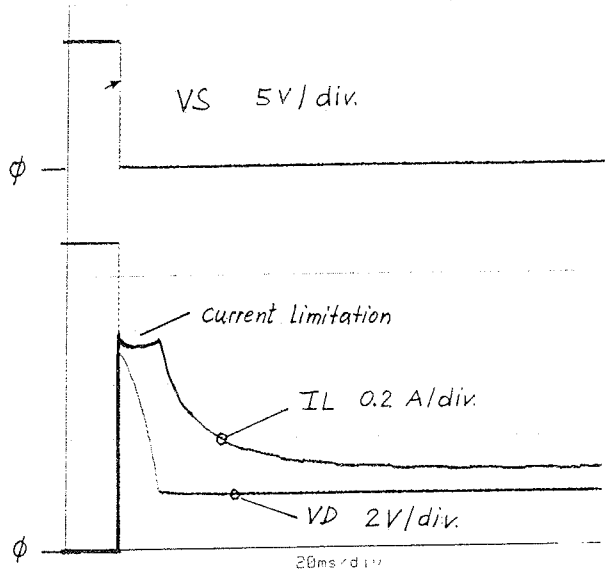

Fig. 7: Measuring result: VS drop from 12V to 0V results in switching on the lamp

this leads to a first order temperature compensation of the current threshold.

6. MEASUREMENT RESULTS

Measurement results are shown in fig. 7. When the supply voltage VS is interrupted, the lamp is turned on. For the first 20 ms the high inrush current of the lamp is limited, then the output voltage VD is stabilized to a value of 2 V.

CONCLUSION

A new lamp driver circuit was realized in a smart power system chip for automotive application. The requirements of reliable operation could be fulfilled also in a situation, where the chip itself has no supply voltage and only the lamp is supplied. This was done by using a charge pump to feed the gate of the power DMOS by its own drain voltage in the on-state. Additionally overload protection circuits were designed which work under very low supply voltage conditions.

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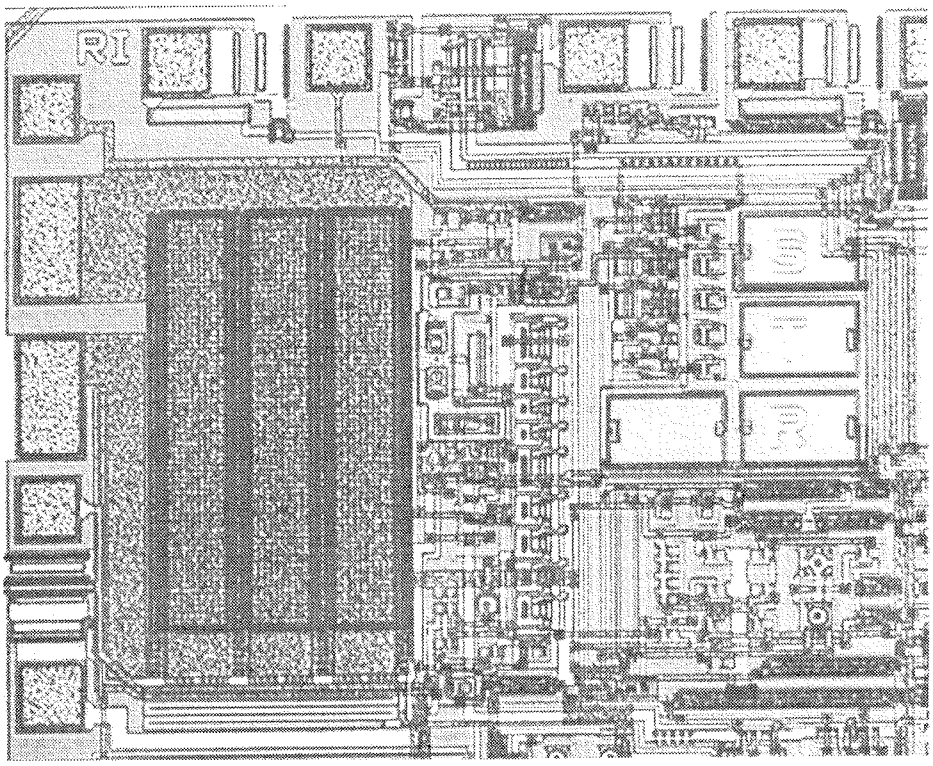

Fig. 8: Part of the chip showing driver circuit, area approx. 1.0x1.1 mm^2