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TECHNOLOGICAL CHALLENGES FOR SILICON TECHNOLOGIES

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Key words: microelectronics, semiconductors, silicon technologies, technological challenges, CMOS technologies, optimization of technologies, future trends, BICMOS technologies, fabrication processes, FA, Furnace Annealing, RTA, Rapid Thermal Annealing, 0.5 micrometer technologies, 0.07 micrometer technologies, Si-Ge technologies, HBT, Heterojunction Bipolar Transistors, low power technologies, CCD-CMOS technologies, NVM, Non volatile memories, Flash EEPROM memories, LV, low voltages, SOI technologies, Silicon-On-Insulator technologies, DUV lithography, Deep UltraViolet lithography, EUV lithography, Extreme UltraViolet lithography, SOG, Spin-On-Glass, TLM technology, Three Layers of Metal, 5LM, 5 layers of Metal, CMP technology, Chemical-Mechanical Polishing technology

Abstract: An overview is given of the present status and future requirements in association with the increasing functionality added to the core CMOS-based technologies, such as e.g. mixed signal, bipolar, low voltage, non volatile memories, low power and smart technologies. The stringent impact on the optimisation of different technological modules is illustrated. Future trends related to process modules such as optical lithography, isolation schemes, interconnects and metallization schemes are outlined. To some extent restrictions imposed by device physics and reliability aspects have to be taken into account.

Tehnološki izzivi za tehnologije na siliciju

Ključne besede: mikroelektronika, polprevodniki, Si tehnologije silicijeve, problemi tehnološki, CMOS tehnologije, optimiranje tehnologij, trendi prihodnji, BICMOS tehnologije, procesi proizvodni, FA žganje v peči, RTA žganje hitro termično, tehnologije 0,5 mikrometer, tehnologije 0,07 mikrometer, Si-Ge tehnologije, HBT transistorji bipolarni heterospojni, tehnologije moči majhnih, CCD-CMOS tehnologije, NVM pomnilniki neizbrisljivi, Flash EEPROM, LV napetosti nizke, SOI tehnologije silicij-na-izolantu, DUV itografija ultravijolična globoka, EUV litografija ultravijolična ekstremna, SOG steklo tekoče naneseno centrifugalno, TLM tehnologija treh plasti kovinskih, 5LM tehnologija 5 plasti kovinskih, CMP tehnologija poliranja kemijsko-mehanskega

Povzetek: V prispevku je podano trenutno stanje in nove zahteve za tehnologije na siliciju, predvsem s stališča povečane funkcionalnosti, oz. zahtev v smislu obdelave mešanih signalov, nizke delovne napetosti, nizke moči in realizacije pametnih funkcij. Prikazano je tudi, kako te zahteve nujno prizadenejo in vplivajo na optimizacijo različnih tehnoloških modulov. Predstavljene so bodoče zahteve glede posameznih procesnih modulov, kot so optična litografija, načini izolacije ter povezovalne in metalizacijske tehnike. Do neke mere moramo upoštevat tudii notranje omejitve, ki nam jih postavljata zanesljivost in fizika polprevodnikov.

1. INTRODUCTION

The "VLSI revolution" has made the microelectronics industry to become one of the largest industries with respect to turn-over and employment opportunities, and has surely a strong impact on many aspects of our social life. The microelectronics revolution is clearly visible in areas such as defence, telecommunication, computers, software services, robotics, medical electronics, consumer applications, instrumentation, industrial electronics, automotive applications... The high expectations in multimedia linked to the electronic highway surely rely on the availability of integrated circuits with high packing density levels and improved speed performances. Handheld, ultralow power electronics will have a strong impact on the the future way people work, play and life together.

Device scaling continues, with a 0.12 μm technology expected in 2004. Every 3 years a new device generation brings 25% more processing steps, 38% larger chips size, a 35% increase in cost of ultra clean materials and a 20% increase in test cost /1/. The technology driver towards higher transistor densities and improved performances is nowadays surely CMOS for memory applications such as SRAMs and DRAMs, while microprocessor requirements push the interconnect technology and routing schemes to high packing density and complex multi level metal processing. The overall trends of the core digital technology for memory applications and mpu's is well known and is schematically illustrated in Fig. 1. In general, the scaling trends are following Moore's law, i.e. the average lifetime for a technology generation is about three years and for every new generation the memory density increases by four. By the end of the century, 0.25 and 0.18 μm technologies will be the standard for volume production of 1 G memories, notwithstanding the extremely high costs to introduce a new technology generation. These deep submicron technologies are requiring advanced processing modules such as e.g. deep UV optical lithography, improved isolation schemes, appropriate metallisation and interconnect schemes for allowing 4 to 5 metal layers, and optimised device engineering concepts to improve the device reliability /2/. The roadmap for some DRAM parameters in shown in Table I.

Table I: Roadmap for some DRAM parameters.

	1 Mb	4 Mb	16 Mb	64 Mb	256 Mb	1 Gb	4 Gb
Year	1987	1990	1993	1996	1998	2001	2004
L (μm)	1.0	0.7	0.5	0.35	0.25	0.18	0.13
Levels	11	14	18	21	21	23	23
Gate (nm)	20	15	12	10	7	5-4	5-4
Steps	200	300	400	500	550	600	600
Junct. (μm)	0.25	0.2	0.15	0.1	0.07	0.05	0.03
access (ns)	50-80	70	50-80	50	40	?	?
wafer (mm)	125	150	150	200	200/300	300	300

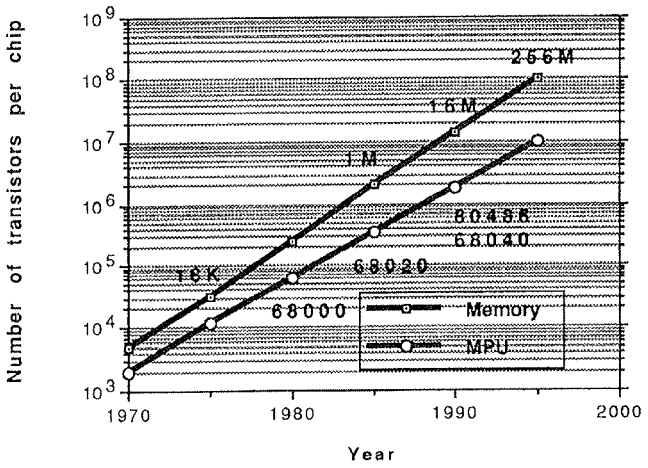

Fig. 1: The change in number of transistors per chip for DRAM and MPU's.

The microelectronics market is not only a digital one, so that beside the trends towards 0.25 and 0.18 μm minimum feature sizes, much attention is also given to an increase of the functionality of a technology. This implies that while a digital technology is taken into production, efforts are devoted towards the development of additional functions such as e.g. analogue building blocs, CCD-CMOS, low voltage, low power, higher frequencies and low noise performance. The added functionality to the core digital process necessitates the availability of dedicated processing modules. This paper reviews first some general trends related to an increased functionality, before discussing future technological challenges in order to keep up with the overall scaling trend. The latter will be illustrated by briefly reviewing the optical lithography, the device isolation, and the interconenct and metallization processing modules.

2. FUNCTIONALITY OF Si TECHNOLOGIES

This section reviews some key aspects related to increasing the functionality of core digital technologies. Attention will be given to BICMOS technologies, the potential of a Si-Ge technology, low power applications, CCD-CMOS, non volatile memories and SOI-CMOS.

2.1 BICMOS

The increased demand for functionality has given a push for the development of analog-digital (mixed mode) and BICMOS technologies. In the past analog-digital technologies came around one year later in production than the pure digital process, while at the moment often a company which has an important market share in mixed mode products tries to have the analog-digital process as fast as possible, meaning at the same time as the digital technology. A modular technology concept facilitates the implementation of additional processing modules.

However, the last few years more and more emphasis has been put on developing technologies with more and different functionality compared to the standard digital and analog-digital technologies. The extension of a CMOS technology with bipolar transistors in order to get an increased speed at an acceptable increase of cost,

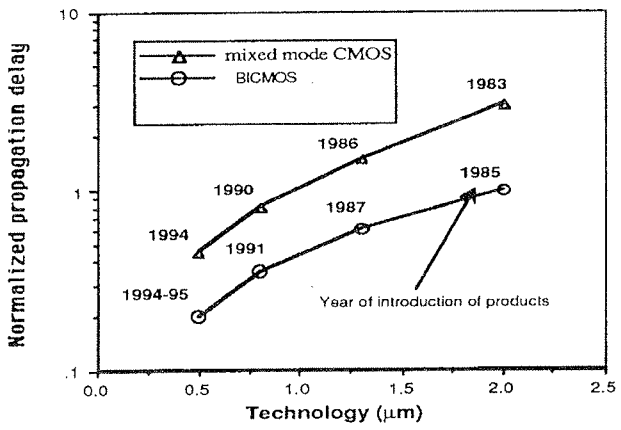

Fig. 2: The normalised propagation delay versus the minimum feature size for mixed mode CMOS and BICMOS technologies respectively /3/.

becomes more and more popular. As shown in Fig. 2 the introduction of a BICMOS technology was 1 to 2 years behind the availability of analog-digital processes with the same minimum feature size. At the moment the difference in time for introducing these technologies is almost negligible. However, when introducing additional functionality there is always an increase in cost. Furthermore the implementation of bipolar transistors in CMOS results in less performant bipolar devices than when they are fabricated in a pure bipolar technology. Different trade off' s for CMOS and BICMOS technologies are summarised in Table II.

Table II: Trade off's between key features in different technologies. The + means the best score and the - means the lowest score.

	Bipolar	CMOS	BICMOS
Speed	+	-	+
Power consumption	-	+	+/-
Packing density	-	+	+/-
Analog features	+	-	+
Driving capability	+	-	+
Complexity	+	+	-
Cost	+	+	-

For high frequency analogue applications the transistor 1/f noise is an important parameter. It has been demonstrated (see e.g. /4/) that for a polysilicon emitter technology, the interfacial oxide thickness and the amount of oxide break-up not only has an impact on the DC parameters, but also strongly influence the low frequency noise performance. To obtain a general picture on the noise behaviour, i.e. to develop fundamental noise models, one has to take into account both technological (pre-cleaning, polysilicon deposition technique, furnace or RTA anneal) and operating (low or high current regime) conditions. The device fabrication process has to be optimised in such a way that the improved noise performance has no degrading impact on the current gain. Recently, a clear relationship between both parameters has been observed as illustrated in Fig. 3. Process splits with both furnace anneal (FA) and rapid thermal anneal (RTA), and with different interfacial oxide layers, have been used to evaluate devices processed in a 0.5 μm technology /5/.

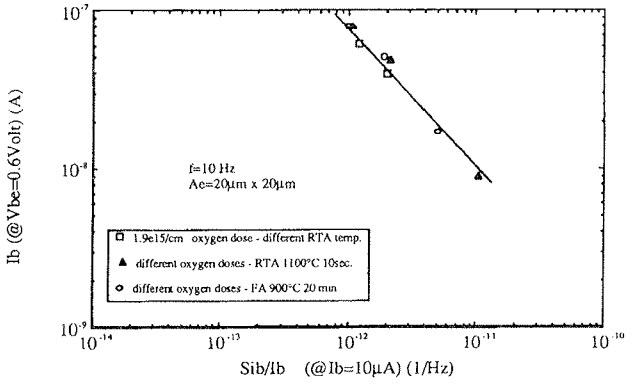

Fig. 3: Experimental relationship between the normalised base current noise spectral density (at I_B = 10 µA and f = 10 Hz) and the base current I_B (at V_{BE} = 0.6 V) /4/.

2.2 SiGe Technologies

Another technological approach to achieve high speed performance circuits is to use a SiGe technology. Although the first reports on these Hetero-junction Bipolar Transistors (HBT) became available in 1986, SiGe devices are not found in production yet. The material aspects of growing the required compound layers with a minimum of lattice strain (too high strain will lead to the generation of interface dislocations) is nowadays well under control. The lattice mismatch, which depends on the Ge concentration and the layer thickness, can be engineered by adding small amounts of carbon. According to Vengard's law a Ge to C ratio of 9:1 would allow a perfect match with the silicon lattice. The pioneering SiGe material and device work has surely been done at IBM and very promising results have been achieved by Daimler-Benz, Analog Devices and NEC. A cross-sectional illustration of an advanced self-aligned SiGe technology is given in Fig. 4. Each hetero-junction transistor is isolated by 1 μm wide trenches etched 4 to 5 μm deep in the silicon and refilled with polysilicon and oxide. Heavily n^+ and p^+ polysilicon layers form the contacts to the emitter and base regions. The contacts are filled with tungsten and a standard Al/Cu metallisation scheme is used.

The driving application for SiGe devices is RF wireless communication, although there is a strong competition in the field from both Si and GaAs devices. At the 1995 IEDM meeting several devices with a f_T around 30 GHz have been reported. The real breakthrough of the Si-Ge

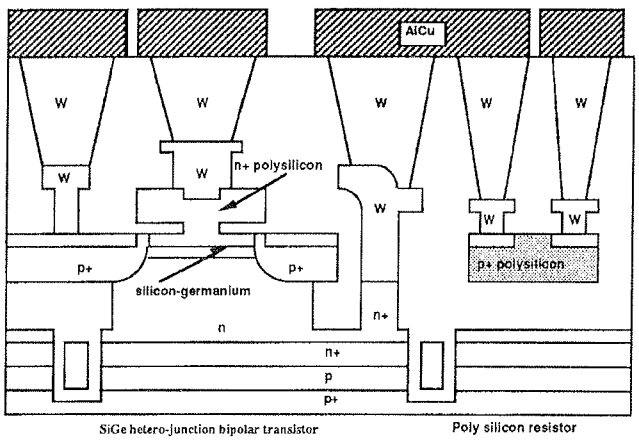

Fig. 4: Schematic illustration of an advanced SiGe circuit, after Cressler /6/.

technology will strongly depend on cost and manufacturing related issues instead of on performance, as the overall goal is to meet the performance specifications at minimum cost in a reproducible way. The closer the fabrication technology can be matched with standard silicon technology, the cheaper the final product will be. Also for some optoelectronic applications SiGe based technologies have a strong potential. A recent review on Si-Ge based materials and devices can be found in /7/. It should finally be mentioned that SiGe HBTs are very promising for cryogenic applications /8/ and have recently been demonstrated to be radiation hard up to 1 Mrad total dose levels /9/.

2.3 Low Power

The increased use of battery-operated products such as portable computers, cordless telephones, pocket calculators, pagers ... has strongly triggered the interest in low power technologies /10/. The power consumption can be restricted by lowering the supply voltage and limiting the load capacitance. However, a figure of merit of the circuit performance is given by the power-delay product. In order for CMOS circuits to compensate for the reduction of the speed performance by lowering the supply voltage, one has to lower the threshold voltage. A typical trade-off between delay time and supply voltage is illustrated in Fig. 5 for different technologies. However, a lower threshold voltage is also making the circuit more vulnerable to threshold voltage fluctuations caused by variations in the fabrication process and short-channel effects. It is therefore necessary either to change some technology steps resulting in higher speeds for the same dimensions, as is the strategy for low power/low voltage CMOS technologies, or to introduce new types of design gates as is more used in low power/ low voltage BICMOS processes. In CMOS the effective channel length, the series resistances, the gate oxide thickness and all the parasitics are reduced as much as possible when reducing the supply voltage from 3.3 V to 1 V. However, it is much more difficult to obtain the same speed for a 1 V CMOS technology then it is for a standard 3.3 V CMOS technology. The threshold voltage is set by the specification on subthreshold current and the required noise margins. Lower supply voltage means reduced drive current, but the loss can be limited by using small threshold voltages and thin

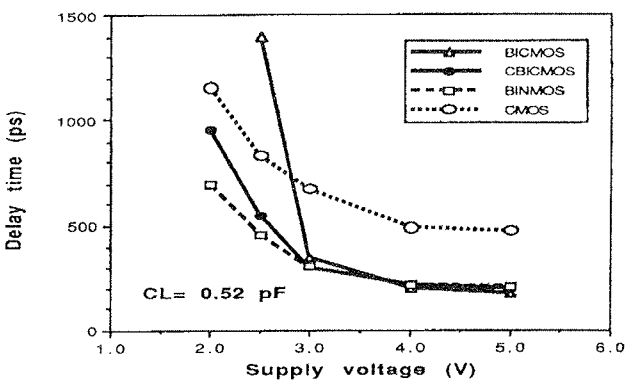

Fig. 5: Delay time versus supply voltage for different CMOS and BICMOS technologies /11/.

gate oxide dielectrics. The loss in speed as a result of reduction in current can be pushed to a minimum by reducing the parasitics like source/drain capacitance, overlap capacitance and routing capacitance and the related resistances. Furthermore a change in design concept is necessary to optimize a low voltage circuit next to technology changes.

The larger increase with decreasing voltage of the delay of standard BICMOS gates has lead to the development of new BICMOS cells like the CBICMOS cell and the BiNMOS cell. These new cells can be used for lower supply voltages. Especially the BINMOS gate is at 1.5 V supply voltage still faster than a loaded standard CMOS inverter gate, while its current drivability is significantly better than that of a CMOS gate. The influence of the supply voltage on the delay time is also illustrated in Fig. 5 for the CMOS and different BICMOS configurations for inverters with an additional capacitive load of 0.52 pF.

2.4 CCD-CMOS

The functionality of digital CMOS processes can be extended by including dedicated processing modules for achieving a CCD-CMOS technology. The CCD technology is superior for imaging applications, while the CMOS part allows the on-chip integration of pre- and/or post-processing functions. In cases where the image quality is less important, e.g. for automated inspection and control applications, the CMOS building blocs also can be used for imaging. In this case either a diode or a transistor cell is used as a pixel. Nowadays there is great interest in CMOS imagers as they can be fabricated at a lower cost compared to the standard CCD devices. Active vision for robotics applications requiring features such as selectable frame rate and integration time, random access of the region of interest, and real-time programmability of the sensor resolution can be achieved by a CMOS technology /12/.

2.5 Non Volatile Memories

An important market segment is taken by circuits based on non-volatile memory (NVM) cells. Although there exists a large variety of cell concepts for realising a floating gate memory structure /13/, the fasted growing market share is taken by the Flash Electrical Erasable PROM (Flash-EEPROM) type devices. Compared to a standard digital CMOS process, this requires the implementation of a second polysilicon layer and the use of very thin oxides. To overcome the major drawback of NVMs which are relying on conventional channel hot electron injection for programming and therefore requiring an external high voltage, a new cell concept called HIMOS, consisting of a split-gate structure and a coupling capacitor has been proposed /14/. In a 1.2 μm and 0.7 μm technologies, 5 V only programming can be achieved in a few microseconds and also the 3.3 V operation has been demonstrated. For further down scaled technologies like 0.5 μm and 0.35 μm the HIMOS cell gives even faster writing speeds. Only minor process modifications are needed for the implementation of the HIMOS cell in a standard digital CMOS technology.

The additional processing steps are the growth of a tunnel oxide, an additional EEPROM drain junction implant and a second polysilicon layer. Based on the diffusion enhanced oxidation rate, the interpoly oxide is grown simultaneously with the gate oxide. For reliability reasons the tunnel oxide has to be of very good quality, limiting the thickness scaling of the tunnel oxide to keep retention within specification. Nitride oxides for tunnel oxide give improved results related to degradion. Much attention is also given to the use of oxynitride (ONO) type of interpoly dielectrics.

Another class of NVM is based on the use of a ferroelectric technology. As ferroelectric layer PZT ($PbZr_xTi_{1-x}O_3$), deposited by either laser ablation or a sol-gel technique, is often used. Although these layers can easily be implemented in a CMOS process flow, there still remain some questions concerning the compatibility and possible contamination risk when processed in a Si fabrication line.

2.6 SOI Technologies

Increased functionality can also be obtained by using a Silicon-on-Insulator technology. Compared to bulk CMOS, a higher speed performance is obtained for the same gate length. Dependent on the application fields, SOI technologies are beneficial for deep submicron /15/, low temperature /16/, low power /17/, radiation-hard, and high temperature operation respectively. The material aspects have originally hampered the breakthrough of SOI technologies for commercial applications, but these have been strongly improved since the availability of SIMOX and wafers bonding (BESOI). In the recent years, a revival of the interest in SOI technologies has been observed. During the last decade several processing modules have been optimised for processing on SOI wafers /18/. Especially for analogue applications, the low frequency noise performance has to be minimised. Recently, an in-depth study of the origin of the different noise sources and their relation to the technological parameters has been published /19/. Furthermore, the lower subthreshold swing for fully depleted SOI devices compared to standard CMOS makes SOI a good candidate for low voltage applications.

2.7 Future Trends

There are also other means to increase the functionality of the circuits by using e.g. smart power, neural network based concepts or the combination of standard CMOS or bipolar processing with micro machining and/or sensor technology. The latter results into integrated microsystems on chip /20-21/. In the coming years these technologies will surely take an important share of the microelectronics market. However, within the restrictions of the present paper they are not addressed.

3. TECHNOLOGICAL CHALLENGES

By the end of the century the core CMOS technology in volume production will have 0.25 μm feature sizes, with 6 nm gate oxides and 0.07 μm junction depths. However some of the more advanced companies will already run 0.18 μm CMOS in production. The process will need more than 20 masking levels and it is expected that more than 5 metal levels will be needed. Therefore it is of crucial importance to develop on time the required advanced processing modules. In order to illustrate the difficulties that this may impose, a few process modules, such as optical lithography, device isolation, and interconnects and metallization schemes will be briefly discussed.

3.1 Optical Lithography

The optical lithography roadmap for submicron technologies is schematically illustrated in Fig. 6. While g-line lithography (436 nm wavelength) was commonly used for a 1 μm technology, i-line lithography (365 nm) was first introduced for 0.7 μm technologies. Nowadays, i-line lithography is the standard for all 0.5 μm processes. Most likely i-line will allow to go down to 0.35 μm and even to 0.30 μm feature sizes in production. Deep UV (DUV) lithography at 248 nm (KrF laser) was first introduced to perform research at the 0.35 μm level and will become the mainstream technology for 0.25 μm technologies /22-23/. It is even expected that 248 nm will be capable to handle 0.18 μm geometries. By further reducing the wavelength to 193 nm (ArF laser), there is a good perspective that optical lithography can be used for volume production of 1 Gb devices. This has also been confirmed by simulations based on Depict 3.0, pointing out that by using a 0.6 numerical aperture (NA) 193 nm DUV exposure tool combined with annular illumination and the use of attenuated phase shifting masks, an acceptable process window can be obtained for 0.12 μm geometries /23/. The main difficulty for optical lithography is to obtain the required resolution with a sufficient depth of focus. Also the presence of underlying topography leads for standard lithography to large problems when scaling down the geometries to values smaller than 0.5 μm. Beyond 193 nm the roadmap is less clear and several possible alternatives are being mentioned, i.e. proximity x-ray, extreme UV at 13 nm (EUV), the exploration of new wavelengths like 126 nm and 157 nm, and ion projection /24/.

On the stepper side it is possible to optimise the numerical aperture of the lens and to reduce the wavelength of the excimer laser. On the processing side, one can work with improved resist schemes or one can use more advanced processing sequences, like the use of top

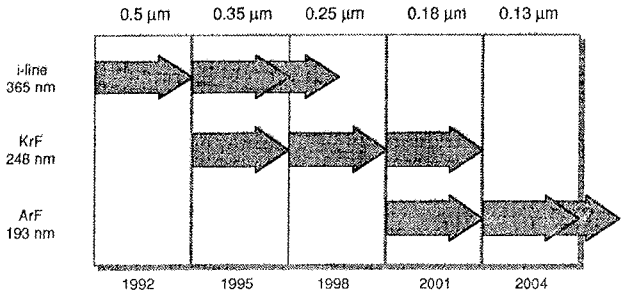

Fig. 6: Roadmap for optical lithography.

and bottom anti-reflective coatings. For the moment, extensive research is on-going related to various resolution enhancement techniques such as respectively multilayer resist schemes, surface imaging techniques (e.g. DESIRE process), off-axis illumination, and the use of phase shifting masks. A recent review on these topics has been published by Van den hove and Ronse /23/. The strong potential for optical lithography is illustrated by the SEM pictures shown in Fig. 7.

Beside the technically feasible solutions, a key factor remains the capital investment and the processing costs. With predicted price tags above $5 million for a DUV stepper and taking into account the associated processing cost, raw calculations point out that about 50% of the wafer fabrication cost is due to patterning. Therefore, in industry preference will be given to an evolutionary approach instead of switching over to a more revolutionary strategy. Mix and match approaches with DUV steppers for the critical layers and i-line for non critical ones will allow 0.18 μm technologies in production. Much attention is also given to the step-and-repeat DUV scanners. Although x-ray lithography /25/ has already been used for 0.5 Mb test memories in a 0.35 μm technology /26/, its breakthrough will only occur when the limits of optical lithography are reached (sub -0.15 μm feature sizes?) due to the high capital investment.

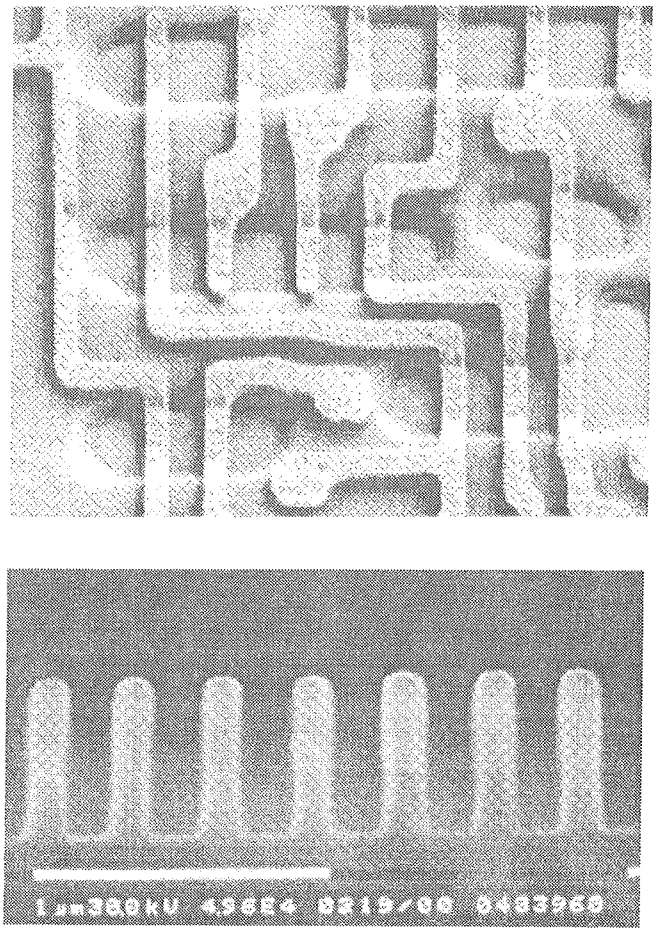

Fig. 7: SEM pictures illustrating the strong potential of optical lithography for deep submicron technologies. (a) 0.25 μm shift register and (b) 0.15 μm line and spacings

Initial results on mixed x-ray and optical lithography have recently been reported for 0.15 μm effective gate length devices /27/.

3.2 Device Isolation

From a technological viewpoint, the down scaling of device geometries is strongly associated with the capability of using an appropriate isolation scheme. For MOS technologies, local oxidation of silicon (LOCOS) has been used as the workhorse isolation technology over the past 25 years /28/. Different alternative approaches have in 1992 been reviewed by Wolf /29/. In general, the optimisation of a LOCOS technique is done by optimising the pad oxide and nitride thickness, the overall thermal budget and/or implementing additional layers in order to reduce the associated stress levels. To optimise an isolation scheme, important features such as the bird's beak length, the overall topography, the generation of bulk defects, gate oxide thinning phenomena, field oxide thinning or thickening, and the electrical device performance (leakage current, gate oxide integrity, overlap capacitance ....) have to be taken into account. In the early 90's it was expected that trench isolation would be needed for submicron technologies. However, the processing difficulties associated with this technique and the progress made in optimising the standard LOCOS technique have strongly hampered its breakthrough. For 0.5 μm technologies, advanced LOCOS techniques are commonly used. Good results are obtained with the polysilicon buffered LOCOS (PBL), while a further improvement by replacing the polysilicon layer in a PBL approach by an amorphous silicon layer as a strong potential to become production worthy for a 0.35 μm technology /30/.

For 0.25 μm technologies a promising approach is the Polysilicon Encapsulated LOCOS (PELOX), first introduced in 1993 by Roth et al. /31/ but further fine-tuned more recently /32/. The scaled-down PELOX is using, similar to LOCOS, a SiO_2-Si_3N_4 stack. However, after patterning the stack and the resist strip, a HF solution is used to undercut the nitride layer and to create a 50 nm deep cavity into the pad oxide. Subsequently the wafers are reoxidised and a 20 nm thick amorphous silicon layer is deposited. During field oxidation the diffusion process is retarded in the filled cavity region, thereby limiting the lateral encroachment and the associated bird's beak formation.

The potential of this PELOX technique is illustrated in Fig. 8, showing a cross section SEM image for 0.2, 0.25 and 0.3 μm wide isolated active area regions respectively. Even for the 0.2 μm wide active regions, the oxide growth under the nitride layer is limited and no pronounced bird's beak is formed /33/. A good control of the recess depth into the silicon, resulting from the dry etching of the active regions, is required for reducing the bird's beak length /34/.

The electrical device performance also depends on the defect formation in the silicon substrate, which is closely related with the associated stress levels in the substrate near the bird's beak. Therefore, stress modelling is becoming essential for the development and optimisa-

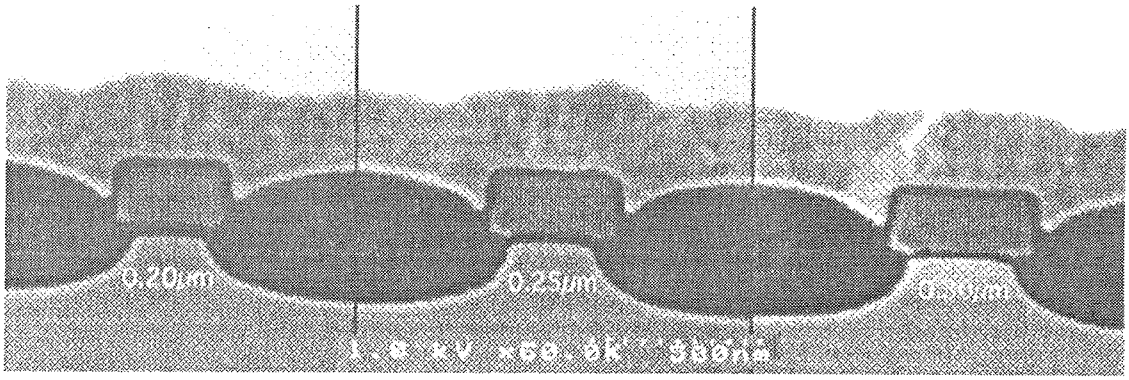

Fig. 8: Cross sectional SEM picture showing 0.2, 0.25 and 0.3 μm wide active regions fabricated with polysilicon encapsulated LOCOS /32/.

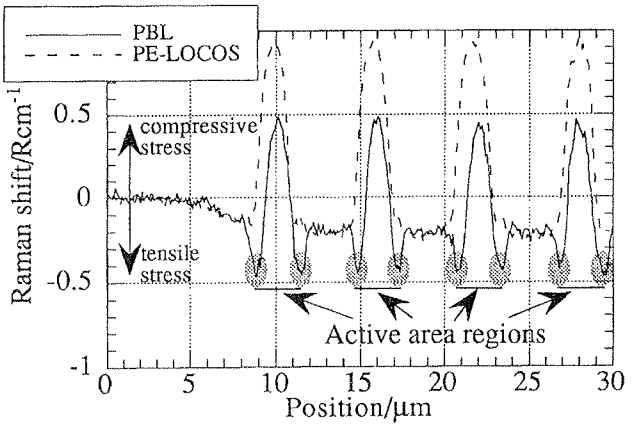

Fig. 9: Illustration of Micro-Raman Spectroscopy to study the difference in stress distribution between PBL and PELOX isolation /32/. A positive Raman shift corresponds with a compressive stress, while a negative shift indicates a tensile stress

tion of an isolation technique. Good theoretical models /35/ are available and experimentally validated by using Micro-Raman Spectroscopy (μ-Raman) in combination with Transmission Electron Microscopy /36/. Detailed information on the local stress distribution can be obtained by combining Convergent Beam electron Diffraction with Electron Diffraction Contrast Imaging /37/. Effective stress measurements combined with 2-D simulations have shown to be a powerful tool for determining in the limits of LOCOS-based isolation techniques /37/. Figure 9 illustrates the use of μ-Raman to study the differences in stress distribution for the PBL and PELOX /32/. In the latter case the tensile stress (negative shift) is reduced, while the compressive stress in the active regions is increased. Too high tensile stress levels will result in the generation of dislocations in the silicon substrate, thereby strongly affecting the leakage current. For an in-depth study, one also has to take into account the quality of the silicon substrate. The impact of the interstitial oxygen content of the substrate on the electrical performance of the LOCOS isolation has recently been demonstrated /38/. Most likely, the increased leakage current for a higher oxygen content of the starting material may be associated with the role of the silicon interstitials on the silicon yield stress /39/. Three dimensional stress analysis can also efficiently be used for studying the defect formation of trench isolation structures /40-41/.

For 0.18 μm CMOS shallow trench combined with Chemical Mechanical Polishing for planarization will become the standard isolation scheme also for ASIC applications.

CMOS-SOI processes are frequently making use of a mesa isolation technique. Also in this case, down scaling the devices may cause some problems. Therefore, attention is given to a refill process combined with planarization. Recently, good results have been reported on using a Chemical Mechanical Polishing (CMP) step for the planarization of 0.35/0.25 μm technology /42/.

3.3 Interconnects and Metallization Schemes

To lower the resistivity of the interconnects in order to increase the speed performance of the circuits, the resistivity of the interconnection should be kept as low as possible. Therefore it has become common practice for VLSI and ULSI technologies to use a salicide technology. For deep submicron feature sizes, the most studied silicides are either $TiSi_2$ or $CoSi_2$. $TiSi_2$ is widely used in manufacturing processes because of its low resistivity and its good thermal stability. The process challenges for yield improvement are related to the silicidation of narrow runners, the elimination of bridging phenomena, and the integration of silicides in combination with shallow junctions respectively /43/. Important parameters to control the yield of silicided narrow polysilicon lines are the doping type and concentration, and the thermal budget of the back-end processing. Retarded silicidation reactions have been observed for As doped layers, and are more pronounced for thinner silicide layers. In the case of narrow active regions, the silicidation reaction can be enhanced by using an As amorphization implant, however with the increased risk for increased junction leakage.

For feature sizes below 0.35 μm, there is a strong interest in the use of $CoSi_2$ in view of the larger process window. For $TiSi_2$ the silicidation is related to the trans-

formation of the high resistivity C49 phase (60-90 $\mu\Omega$cm) into the low resistivity C54 phase (12-15 $\mu\Omega$cm). The transition temperature increases with decreasing film thickness, while at the same time the film disintegration temperature decreases. In addition, the doping type and concentration dependent silicide growth is strongly affecting the use of shallow junctions in a salicide process. In the case of $CoSi_2$, the transformation temperature from the CoSi into the $CoSi_2$ phase is proportional to the film thickness, and is therefore less influenced by down scaling effects. The thermal stability of $CoSi_2$ is also better than that of $TiSi_2$. The larger process window for $CoSi_2$ makes $CoSi_2$ a serious candidate to replace $TiSi_2$ in future scaled down technologies.

For Co silicidation the pre-cleaning step is, however, more critical than for Ti due to the gettering action of the Ti. To overcome this difficulty, investigations have been done to study bilayer systems where either an interfacial Ti layer (Ti/Co scheme) or a Ti capping layer (Co/Ti scheme) is used. Although both bilayers are resulting in a low and uniform sheet resistance for small linewidth, aspects such as the impact on the thermal stability, stress generation at the edges possibly resulting into void formation, the required cleaning steps, and the possible epitaxial regrowth phenomenon have an influence on the reproducibility and overall performance of the system and should therefore be taken into consideration.

The different metallisation schemes that are used have also to be optimised from a reliability viewpoint in order to avoid stress-induced voids and to reduce electromigration problems. The most commonly used metallisation schemes are based on a Al-Si-Cu or Al-Cu alloy. However, interest in other alloys is strongly growing. The research in novel Al-alloys is driven by electro- and stress migration requirements, which become dominant for smaller dimensions. For future technologies much attention is given to Cu-based interconnect layers, while also some more exotic alternatives are investigated. An important problem associated with metallisation is the step coverage, especially when a high aspect ratio is used. Therefore, advanced multilayer metal systems are based on contact and via filling. This can be achieved by using either W-CVD or hot Al-CVD. The selection of either W or Al for contact fill depends strongly on the quality of the barrier layer, both as chemical barrier and adhesion layer and as electrical barrier. Therefor the bottom and sidewall coverage of the barrier layer is of extreme importance, making scaling more and more difficult because of the increased aspect ratio's. Al planarisation is very attractive since its bulk resistivity is only 25 % of that of W-CVD. Present research is aiming at lowering the depostion temperature. Recently, a contact plug technology based on selective nickel silicidation has been proposed /44/. Each of the different plug filling technologies has its own advantages and drawbacks. Another important aspect, which is not addressed here, is the requirement for using barrier layers underneath the metal lines.

Spin-on glass (SOG) and etch-back techniques are commonly used for local topographical smoothing or partial wafer planarisation. However, the introduction of more than 3 metal layers with scaled down dimensions and stacked vias require the implementation of global planarization process steps as illustrated in Fig. 10. The figure shows the difference in approach for a 0.5 μm technology with three metal layers (TLM) and for a 0.35-0.25 μm technology with five metal layers (5LM) respectively. The former is using a SOG planarization, while the latter is based on chemical-mechanical polishing (CMP). One possible process is based on the etch back of Accuflo material, while a better alternative, which is also valid for further scaled down processes, is to use chemical-mechanical polishing (CMP). Although for a long time hampered by equipment, processing and defect control issues, CMP is nowadays a standard for global planarization. The main advantage is related to the global planarity, which compensates for shallow depth of focus. In additional the metal step coverage problems and the associated reliability hazards are also avoided. Some general information of the different aspects of CMP technology are given in /45,46/.

To increase the speed of the circuits, much attention is given to the study of low dielectric materials in order to replace SiO_2 as the interlayer dielectric.The capaci-

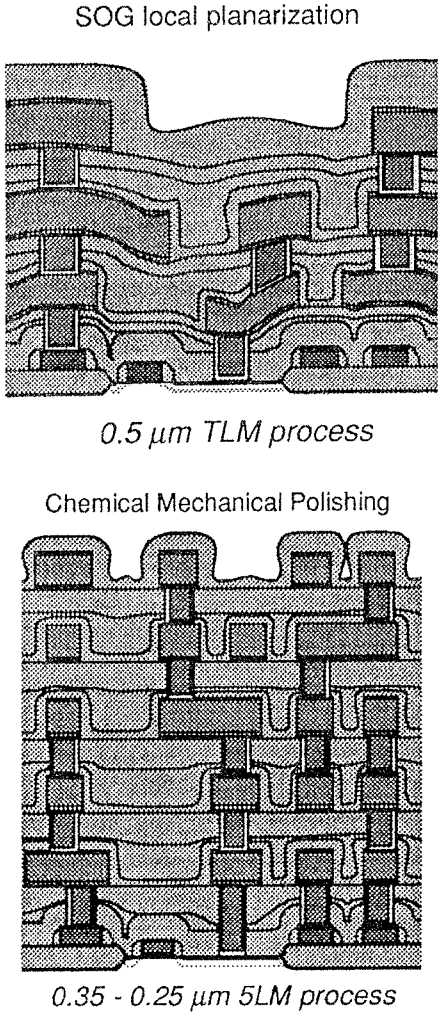

Fig. 10: Illustration of the difference in approach for a 0.5 μm three metal layer (TLM) technology and a 0.35-0.25 μm technology with five metal layers (5LM).

tance is directly proportional to the dielectric constant of the material so that a high K value strongly increases the RC delays. For small geometries, the total capacitance will be dominated by the line-to-line capacitance. This implies that the desired speed (related to the dielectric constant) will depend on the minimum feature size. The target roadmap for low dielectric material is shown in Table III /47/. For different future technologies, to be used for the manufacturing of microprocesses, the table indicated the maximum number of interconnect layers, the possible dielectric material, the desired dielectric constant, and the possible year of introduction.

Table III: Target dielectric constant (K) for future technologies /47/.

Technology µm	Interconnect Layers	Dielectric Material	K	Year
0.35	4-5	SiO_2	3.9	1995
		SiO_2(F)	3-3.7	
0.25	5	polymer	<3	1998
0.18	5-6	polymer	<2.5	2001
0.13	6	polymer	<2	2004
0.10	6-7	polymer	1-2	2007
		aerogels/air		
0.07	7-8	polymer	1-2	2010
		aerogels/air		

The status of the different dielectric materials given in Table III has recently been reviewed by Murarka /48/. The most important conclusions are briefly summarised. The doped oxide films contain 2 to 14 atomic percent fluorine in order to lower the dielectric constant. As for too high fluorine concentrations the films become unstable, the optimum concentration lays around 10%, resulting in a K value of about 3-3.2. However, not only the concentration itself but also the way the fluorine atoms are incorporated in the film has an impact on the dielectric constant. A large variety of polymers have been studied and are still under investigation. The polymerisation process results in anisotropic properties. Cross linking between polymer chains improves the rigidity and may also reduce the anisotropy. Both spin coating and vapour phase deposition techniques are used, with from an environmental viewpoint a preference for the latter due to the fact that they are solvent free. Polyimide siloxane and polysiloxane are intensively studied. Air has the lowest dielectric constant of 1, but imposes some practical problems due the interaction with metal schemes. Therefore aerogels, xerogels or foams in which air is trapped as bubbles in a solidified gel seem to be very promising. To develop a low dielectric material, a variety of materials properties have to be taken into account, such as rigidity, chemical stability, etching behaviour, interaction with metal layers, moisture take up, thickness uniformity, intrinsic stress levels, gap filling and planarization properties .... /49/. The characterisation of these low dielectric materials is a hot topic for the moment and not withstanding the strong industrial need in the near future, the development of new materials has just begun.

4. CONCLUSION

The future trend in silicon technology is on one hand a strong drive towards higher packing densities and increased electrical performances, pushing towards smaller device geometries, and on the other hand an increase of the functionality of core digital technologies by adding different functional options. Both approaches are associated with particular technological challenges. However, to achieve performance specifications at a minimum cost, the overall process complexity and the industrial manufacturability have to be kept under control.

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