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INTEGRATED HALL SENSOR ARRAY ELECTRONICS

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Abstract: The paper describes the approaches for various integrated smart magnetic sensors design in CMOS processes. It presents both sensor biasing electronics and sensor signal processing to obtain the best performance. Magnetic sensor systems are optimized in the following areas:

- The use of multiple sensors - sensor array. This helps to minimize random phenomena like the offset voltage and the noise and allows to compensate for phenomena dependent on sensor orientation and position (piezzo effect) or allows to sense spatial magnetic field distribution.
- Hall sensor biasing - to minimize temperature coefficient and voltage coefficient.
- Two-phase Hall sensor spinning - to minimize the offset voltage.
- Hall sensor signal amplification for signal to noise optimization.

Design examples for each of the listed topic are discussed.

Elektronika za polje integriranih Hallovih senzorjev

Ključne besede: Hall senzorji integrirani, Hall elementi integrirani, polja senzorska, elektronika polj senzorskih, mikroelektronika, vezja napajalna, rotiranje električno, vezja elektronska, optimiranje vezij, avtokalibracija, CMOS procesi, SP procesiranje signalov, signal-šum razmerje, senzorji magnetni inteligentni, snovanje vezij, koeficienti temperaturni, koeficienti napetostni, ojačevalniki signalov

Povzetek: Prispevek obravnava metodologijo za načrtovanje raznih integriranih "pametnih" magnetnih senzorjev v procesih CMOS. Predstavi elektroniko za napajanje senzorjev in elektroniko za procesiranje senzorskega signala s ciljem doseči čim boljše lastnosti sistema. Magnetni senzorski sistemi so optimizirani glede na naslednja področja:
Uporaba več senzorjev - senzorska polja. To pomaga minimizirati naključne pojave kot so napetost ničenja in šuma in pomaga reševati probleme, ki so povezani z orientacijo senzorja in njegovo pozicijo (piezzo effect) ali pa omogoča zaznavo krajevne porazdelitve magnetnega polja.

- Napajanje Hallovega senzorja za minimizacijo temperaturnega in napetostnega koeficienta.
- Dvofazno električno rotiranje Hallovega senzorja za minimizacijo napetosti ničenja.
- Ojačevalniki za ojačenje senzorskega signala glede na optimizacijo razmerja signal/šum.

Podani so zgledi načrtovanja za navedena področja.

1. INTRODUCTION

Integrated Hall sensor opens a way to reduce cost in various applications such as:

- contactless current measurement
- contactless multiturn switch
- power and energy measurements
- position and angle measurements

CMOS process offers effective solutions to compensate or eliminate various problems associated with non-ideal sensors. It turns out that integrated Hall element offers the best possibility for magnetic sensor systems. The main advantages of Hall elements are: possibility to spin the element and therefore to minimize the offset voltage; large linear range of operation; predictable temperature coefficient of the sensitivity, a possibility to design element with minimal dimensions offered by the process.

The main disadvantage of the Hall element is its relatively low sensitivity, so it requires high gain and low noise preamplifiers.

2. HALL ARRAY APPROACH

The idea to use more than one Hall element was selected mostly to minimize the random phenomena which are offset voltage and Hall element noise. The offset voltage and the noise are improved by factor $\sqrt{N}$ where N is the number of sensors. This implies that it is helpful to use the highest number of sensors possible, so it is not unusual to use several tens of sensors if the design calls for the best possible offset voltage or signal to noise ratio is required.

Fig.1 shows a typical Hall element in 0.8 μm CMOS process. Small dimensions of the element (23 μm x 23 μm) present no obstacle to multiply it; the array consisting one hundred elements would occupy less than 0.1mm^2 of silicon area.

The benefit of this approach is not only the noise and the offset minimization by square root of number of sensors, it allows the designer to orientate each element for 90 degrees compared to the nearby sensors. This further reduces the offset voltage introduced by piezzo effect and the offset caused by low gradient of Hall plate material properties.

Furthermore a string of sensors can detect spatial gradient of the applied magnetic field and so help to detect position of the ASIC relative to the magnetic field.

Finally this approach allows the designer to build on the chip the reference magnetic field, which can be used either for testing, autocalibration or even for long term ratiometric measurement of the magnetic field. Such

arrangement is very useful when the magnetic sensor system has to fulfill a strict requirements like the requirements for Watt-hour metering.

Fig. 2 shows the integrated coil which generates magnetic field of 100 μT per 1mA coil current. The coil efficiency increases with decreasing overall dimensions; this is additional reason to use minimal Hall element dimensions.

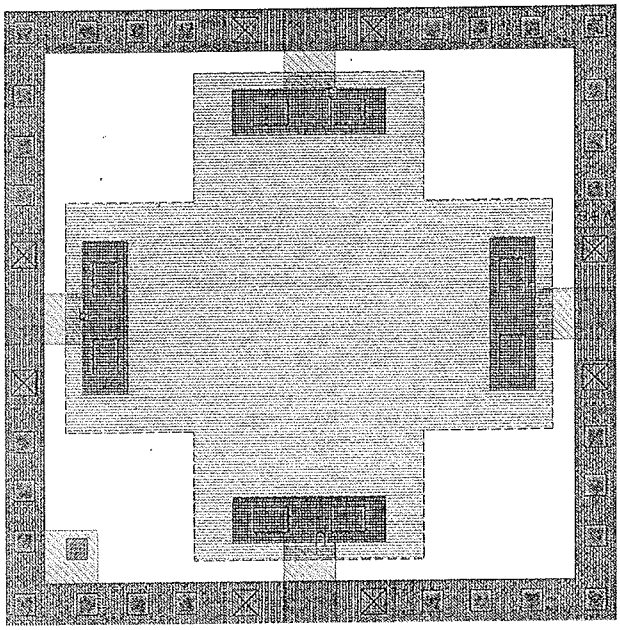

Fig. 1: Layout of minimal Hall element in 0.8 µm CMOS technology. Overall dimensons are 23 µm x 23 µm.

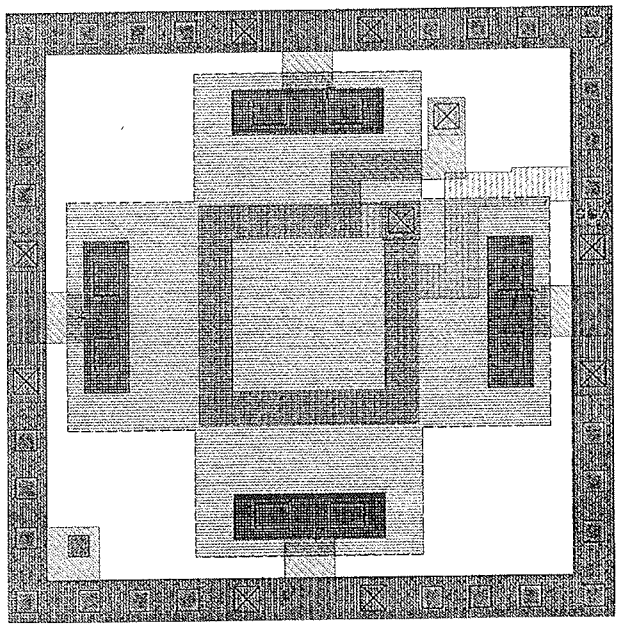

Fig. 2: Integrated coil using one turn of metal 2

3. HALL ELEMENT BIASING

The purpose of Hall element bias electronics is to provide bias current which compensates the temperature effect of the Hall element sensitivity and compensates the effect of the sensitivity change due to substrate to Hall element potential.

The schematic shown in fig.3 solves both problems.

The Hall bias current is linearly proportional to the reference voltage Vref with required temperature coefficient and inversely proportional to the resistor RE. For the total temperature coefficient also temperature coefficient of resistor RE, usually poly-silicon resistor, should be observed.

The substrate potential can be kept constant by the use amplifier 2 and resistor divider R1, R2 which sets the selected percentage of Hall element bias voltage to the required substrate bias voltage.

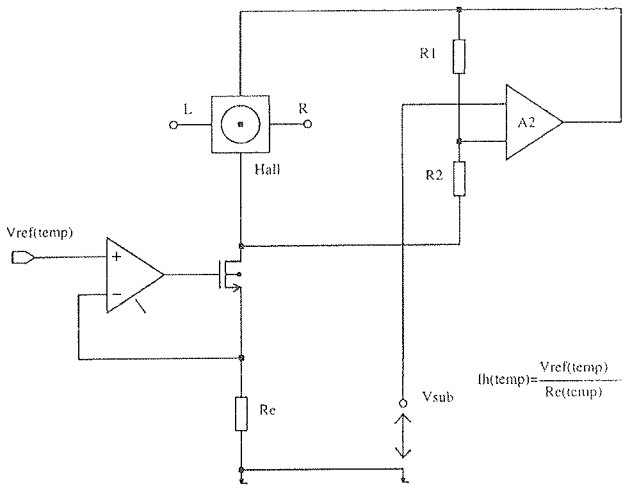

Fig. 3: Bias circuit for Hall element

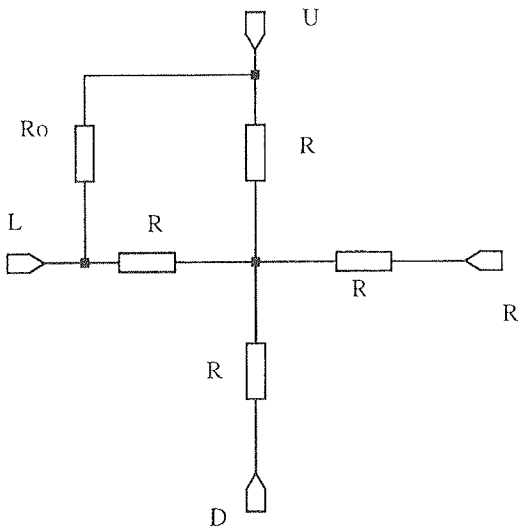

Fig. 4: Equivalent circuit of Hall element offset voltage (first order approximation)

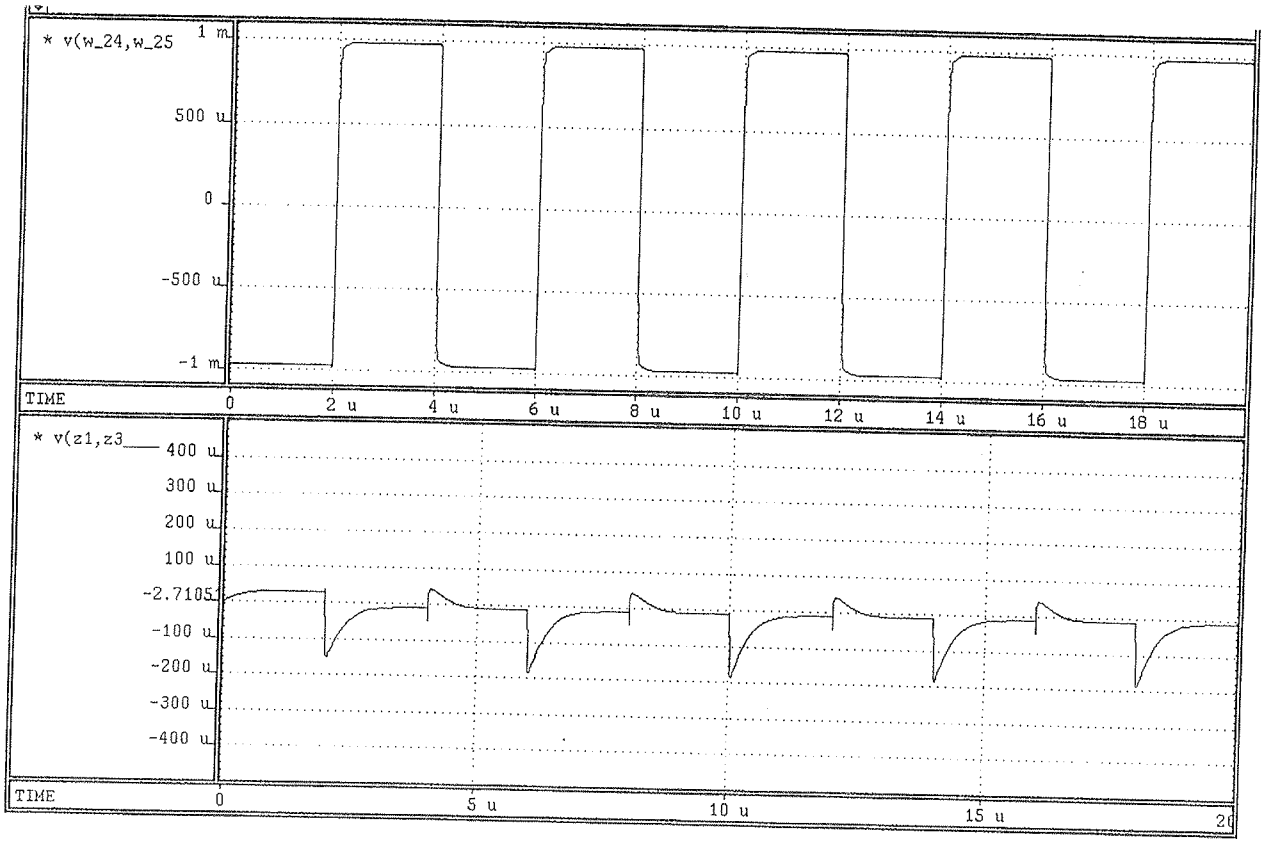

Fig. 5: *Upper trace: simulation results for 1 mV of Hall element offset voltage*
Lower trace: Two phase spinning results for offset voltage cancellation.
Maximal contribution to offset voltage is poor clock feed through cancellation.

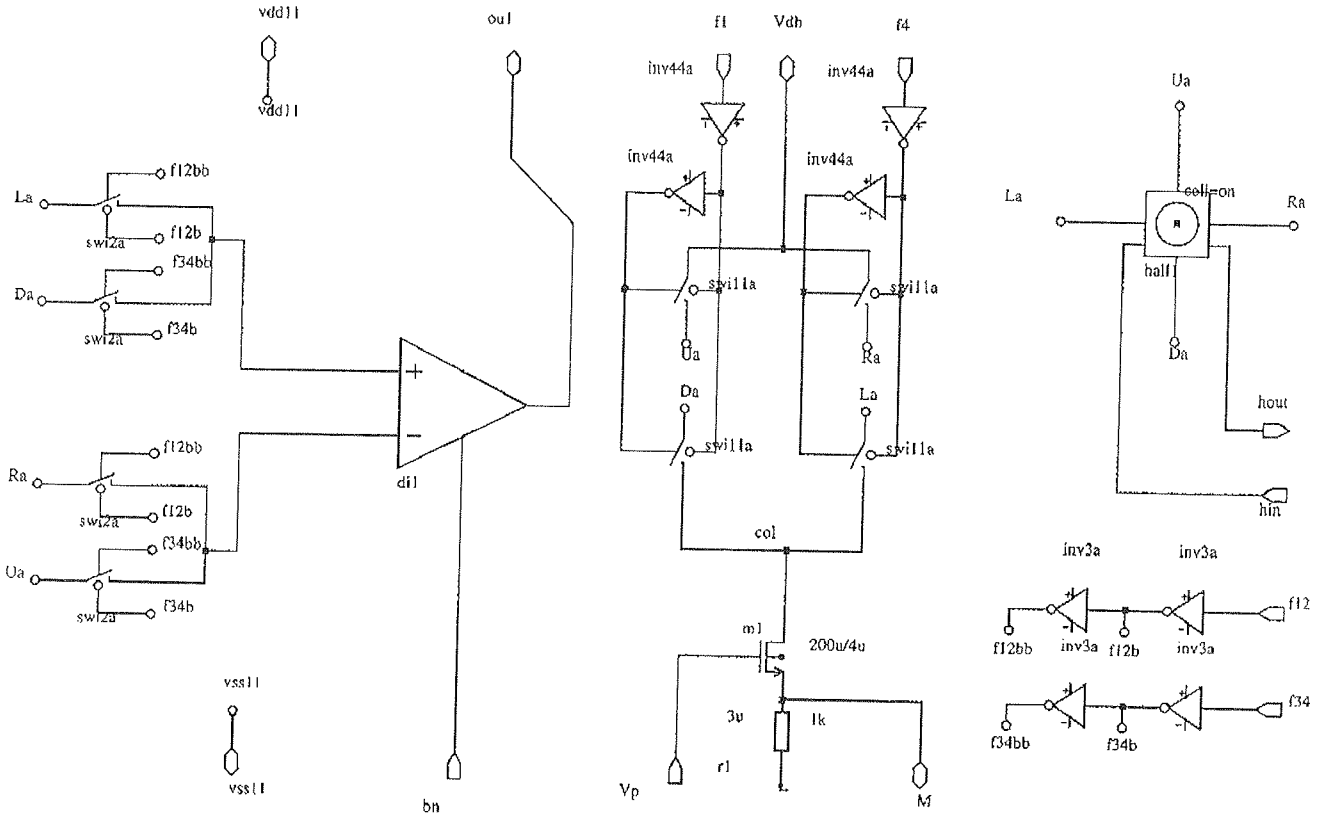

Fig. 6: *Two phase Hall element spinning circuit*

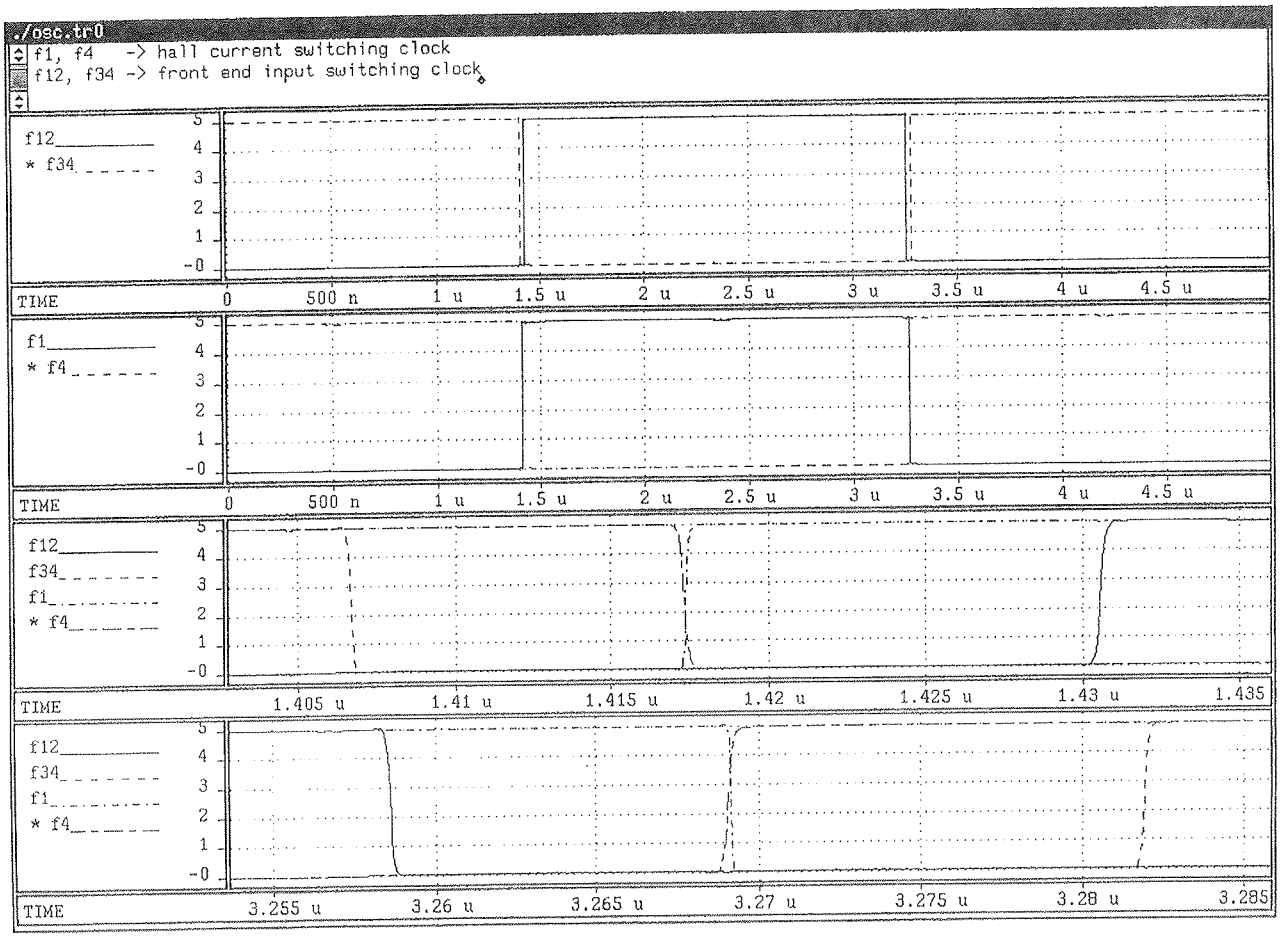

Fig. 7: Simulation results for non-overlapping clocking for clock feed through minimization

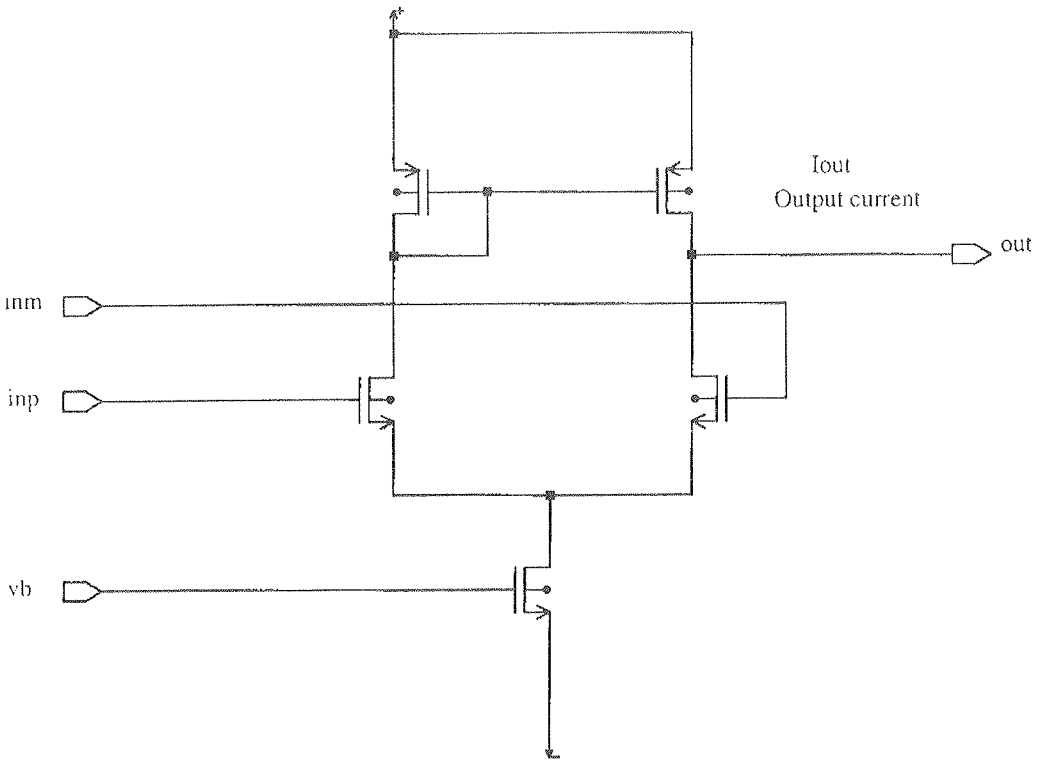

Fig. 8: Differential amplifier - Hall element voltage to current converter

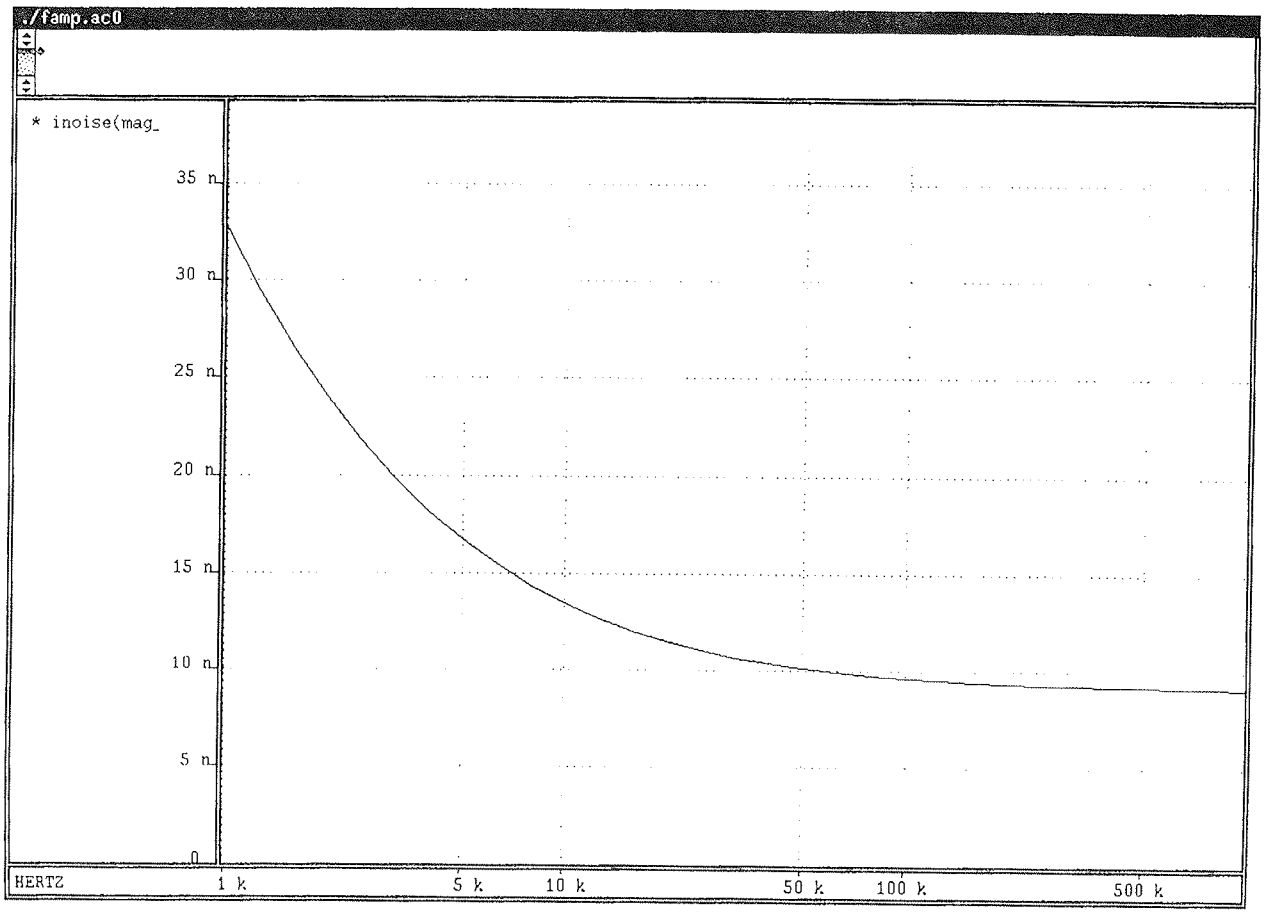

Fig. 9: Simulation results for Hall element voltage to current converter input noise density

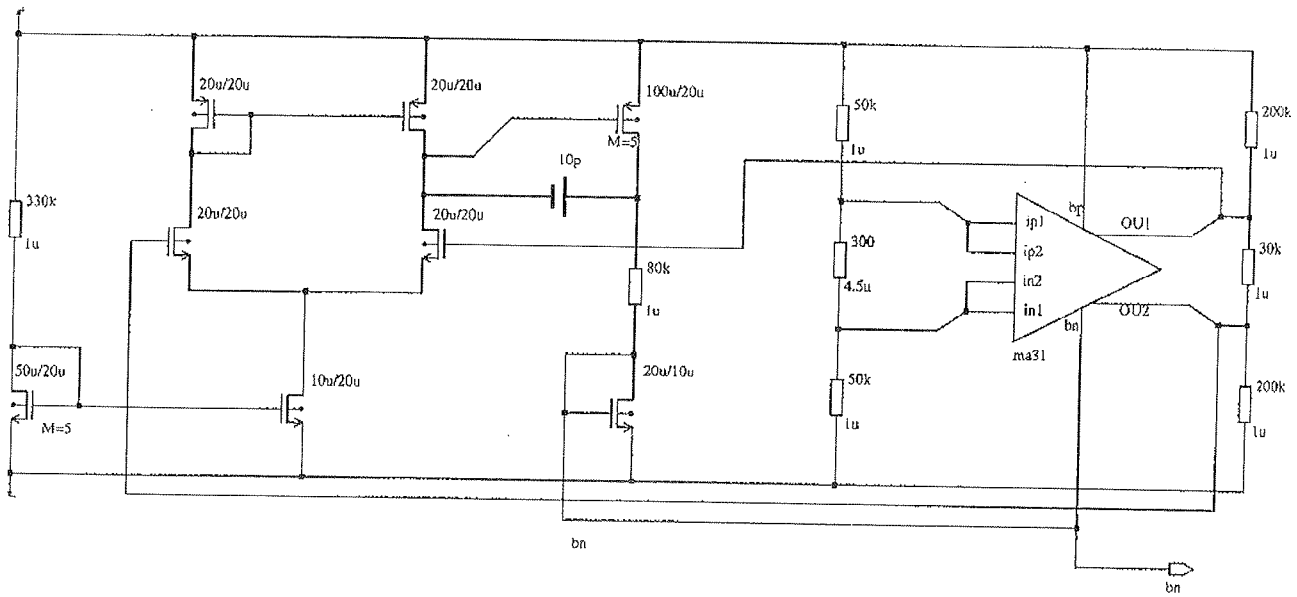

Fig. 10: Close loop amplifier to generate bias current for Hall element voltage to current converter

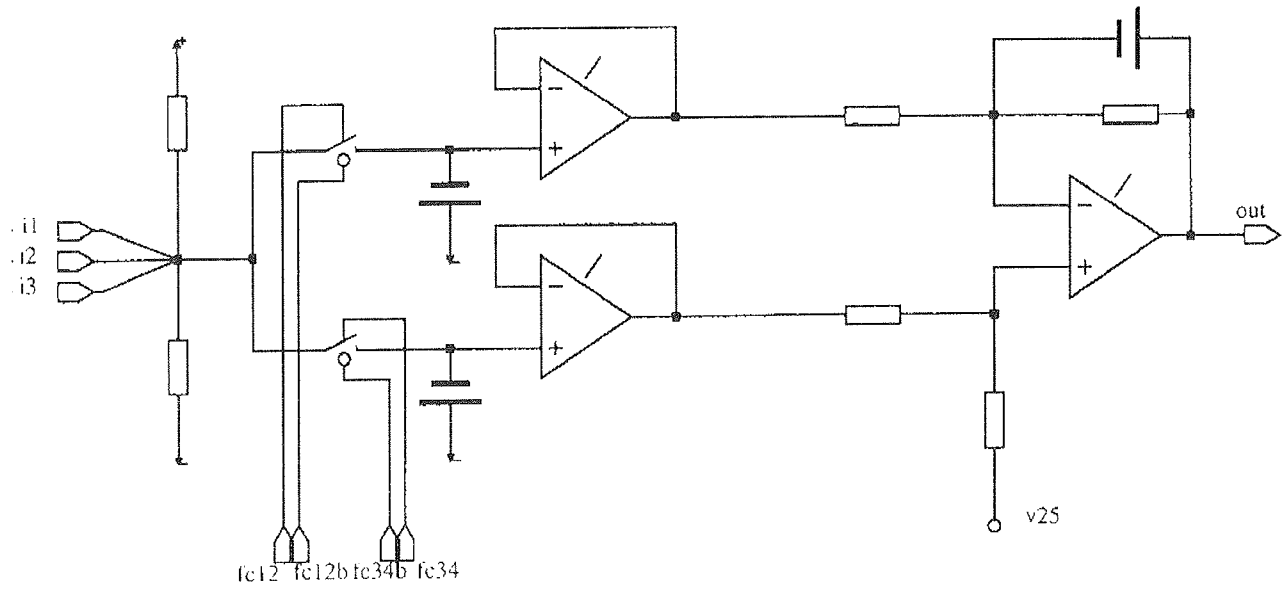

Fig. 11: Hall signal current summation and differential to single ended conversion schematic

4. HALL SENSOR SPINNING

It is well known that electrical rotation for 90 degrees reduces the first order effect of Hall element asymmetry caused by various reasons. The model of such asymmetry is shown in fig. 4, where Ro represents the asymmetry. This model was used in SPICE simulator to prove its efficiency. Fig. 5 shows the results of SPICE simulation, proving that the offset cancellation by two-phase spinning is completely efficient.

Fig. 6 shows the actual spinning circuit.

The selection of spinning frequency helps to minimize the 1/f amplifier noise and determines the frequency response of the systems according to sampling theorem.

Very important feature of spinning is non-overlapping spinning clock for input signals as shown in fig. 7.

5. HALL SIGNAL AMPLIFIERS

The following features are important for Hall signal amplifiers:

- Differential voltage to current conversion to facilitate Hall array signal summation.
- Low noise. Ideally the amplifier noise should be less than Hall element noise. This is achievable only in the high frequencies where 1/f noise becomes insignificant.
- Small size. This allows the use of many Hall elements in the array.
- Controlled gain.

Fig.8 shows the schematic diagram of the Hall signal amplifier. The simple voltage to current converter is achieved by the use of amplifier MOS transistor operating in saturation region. This schematic gives the best possible noise behavior. As shown in fig.9 the noise can drop below in the spinning clock frequency region between 300kHz and 1MHz. This noise level is just below the Hall element noise.

The control of gain is achieved by amplifier bias current which is derived from a closed loop amplifier to assure the supply voltage variation, temperature independence and, process parameter variations.

The amplifier bias schematic is shown in fig.10.

In fig.11 current summation and current to voltage conversion is shown. The spinning clock is at the same time used to eliminate the amplifier stage offset voltage.

6. CONCLUSIONS

Several projects were successfully designed using the described approach. The typical figures achieved are:

Noise density:	<50 nT/√Hz
Offset voltage:	< 100 μT
Temperature coefficient of sensitivity:	<100 ppm/°C
Temperature range:	-40°C - +150°C

These results are better than reported in papers using either single Hall element or other types of integrated magnetic sensors. This proves that the described design approach is very promising.

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