ALCATEL MICROELECTRONICS 0.5 μm Mixed CMOS Technology

Hans Gugg-Schwaiger
Alcatel Microelectronics, München, Germany

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Abstract: The features of the submicron silicon 0.5 μm mixed CMOS technology are described. Process options, process parameters & design rules, cross-section and DOC-references are shown. Achieved Quality levels and design for Quality are discussed briefly. The ADS Asic Design System is described. Finally the CMOS roadmap and 0.35μm mixed CMOS technology are briefly described.

Mešana CMOS tehnologija firme Alcatel Microelectronics z minimalno razsežnostjo 0.5μm

Ključne besede: polprevodniki, mikroelektronika, CMOS tehnologije mešane 0,5 μm, CMOS tehnologije mešane 0,35 μm, ADS ASIC sistem snovanja za vezja integrirana za aplikacije specifične, snovanje za kakovost

Povzetek: V prispevku opisujem osnovne značilnosti mešane CMOS tehnologije z minimalno razsežnostjo 0.5μm. Prikažem procesne možnosti, procesne parametre, načrtovalska pravila, preseke in ustrezno dokumentacijo. Na kratko se dotaknem koncepta vgrajene zanesljivosti in pokažem dosežen nivo kvalitete. Opišem tudi ADS – sistem za načrtovanje ASIC vezij. Na koncu podam možne poti razvoja v bodočnosti in na kratko obravnavam novo mešano CMOS tehnologijo z minimalno razsežnostjo 0.35 μm.

1 INTRODUCTION

Combining the power of a 32bit RISC processor, with its on-board program, VHDL-described hardware and the analog front-end to communicate with analog signals to the external world is the every-day-work for the design community at Alcatel Microelectronics. This type of architectural construction is possible on a single chip thanks to the digital density and the analog capabilities offered by the described half-micron CMOS process.

Applications that have taken advantage of this integration capability are numerous. From integrated toll payment module for cars to low power integrated hearing aids and advanced chip-sets for GSM using the unique zero IF technique.

Speaking about the Application Specific Standard Products (ASSP), the same technology is used to develop the Asymmetrical Digital Subscriber Line (ADSL) chip set, the integrated Power Line Carrier (PLC) modem and the Integrated Services Digital Network (ISDN) product series. Alcatel Microelectronics has made the mixed mode communication chips his niche-flagship.

This breakthrough is the result of a strong revolution within the company. The technological development carried out in the last 5 years has allowed Alcatel Microelectronics to be able to switch its main production to the sub half-micron mixed mode CMOS technology. The company succeeded to bring its digital design methodologies and technology capabilities to the level of expertise recognised for the analog design.

The developed methodologies have been put into the Alcatel Microelectronics EDA system "ADS" (Asic Design System). In parallel the clear strategy for the re-use of value added blocks has been put in place as well as a continued improvement of the product quality.

2 0.5 μm Mixed CMOS Technology

Alcatel Microelectronics started 5 years ago with his first sub-micron mixed mode 0.7 μ CMOS technology. This technology was based on the 1.2 μm generation. Two years after, the new generation 0.5u CMOS was presented to the market. This new generation is characterised by an impressive list of features.

2.1 Digital 0.5 μm CMOS base technology

The efficiency for digital circuitry is obtained by providing self aligned Poly-gate CMOS transistor with size (L and W) down to 0.5 μm. The routing density is made very good by the use of triple metal layers and by the use of stackable vias and contacts. This last feature allows to contact the drain of a CMOS transistor to the highest metal by consuming only the size of one contact. The triple metal allows also to route over the cell, this virtually avoids the need for channel routing. Routing density better than 80% is possible. (see fig. 1, 2, 3)

C05 General Characteristics

Voltage Supply	2.0 V to 3.6 V, 5 V compliant I/O's
Base wafer	6" epi wafers
Dynamic characteristics	
typical gate delay	102 ps
power consumption	0.9μW/Gate/MHz at 3V
ring oscillator delay	104 to 111 ps/Stage
Protection	
latch up resistance	> ±200mA
ESD protection	> ±2000V

Fig.1: C05 General Characteristics

Base process features

	self aligned twin tub N & P Poly Gates
	stackable contacts and vias
	digital & analog NMOS & PMOS transistors
	3V operation / 5V compliant I/O's

Fig.2: C05 Base process features

C05 basic design rules

number of masks: C05D	15
metal interconnect / Poly layers	3M / 1P
Layout rules	
transistor min. width & length	0.5 μm
analog transistors	0.8 μm
Poly line pitch	1.3 μm
Metal 1 pitch	1.6 μm
Metal 2 pitch	1.9 μm
Metal 3 pitch	2.5 μm

Fig.3: C05 basic design rules

2.2 Analog modules of the 0.5 μm CMOS technology

The analog module consists of precision capacitance and resistance. The analog capacitance is build with 2 Poly layers placed on the field oxide. This construction provides a precision capacitance that features a 1.1nF/mm^2 and a voltage non-linearity better than 30ppm/V. The resistance is a high ohmic (HIPO) type. Its sheet resistance is higher than the 1kOhm.

The analog characteristics of the CMOS transistors shows well controlled threshold voltage under the 0.69V in worst case conditions. The thermal noise is limited to 1e-29 V/sqrt(Hz). In addition to the CMOS, capacitance and resistance characteristics, the documentation provided by Alcatel Microelectronics contains characteristics of the junction capacitance, interconnect capacitance, matching data for CMOS transistors, resistances and capacitances. (see fig. 4, 5, 6)

Analog options C05A

number of masks: C05A	18
metal interconnect / Poly layers	3M / 2P
second Poly layer, capacitor	Poly1-Poly2 linear capacitor, 1.1nF/mm2, tol ±10%, Vcl <20ppm/V, Vcq <-10ppm/V, Matching <0.1% (3 sigma) @W/L = 20/20
high-ohmic Poly resistor	1kΩ/sq tol ±10%, voltage linearity: Vcl < 200 ppm/V, temperature coefficient: Tcl < -1500 ppm/°C, matching <0.35% (3 sigma) @W/L = 10/100
bipolar transistor	vertical PNP

Fig.4: C05 Analog options

2.3 Design for reliability

In order to get ultimate quality in production without screening, Iddq and Vscreen testing are implemented in all the designs.

Definitions:

Iddq: Test of Idd leakage current @Vdd_nom & all bias off
Vscreen: Some real testpattern, e.g. ScanPath @ 1.4xVdd_max

These two methods improve the quality and reliability of the IC´s drastically. In order to be able to do the above tests, the IC has to be designed already covering Iddq, which needs some skills especially in analog (e.g. switching off a reference voltage resistor divider, but don´t degrade the matching).

C05 electrical characteristics (worst case)

	NMOS	PMOS	unit
Oxide Tickness	10	10	nm
Threshold Voltage	0.69	-0.66	V
Beta lin	2480	600	$\mu A/V^2$
Noise (Kf)	3E-28	1E-29	V/sqrt(Hz)
Leakage current	1	1	$pA/\mu m^2$
f_T	15	15	GHz
Bipolar transistor		**vertical PNP**, collector to substrate, typical	
Vbe:		0.680	V
Tcl_Vbe		-1.97	mV/K
Hfe		8	
Vearly		170	V
Area		6.76	μm^2

Fig.5: C05 electrical characteristics

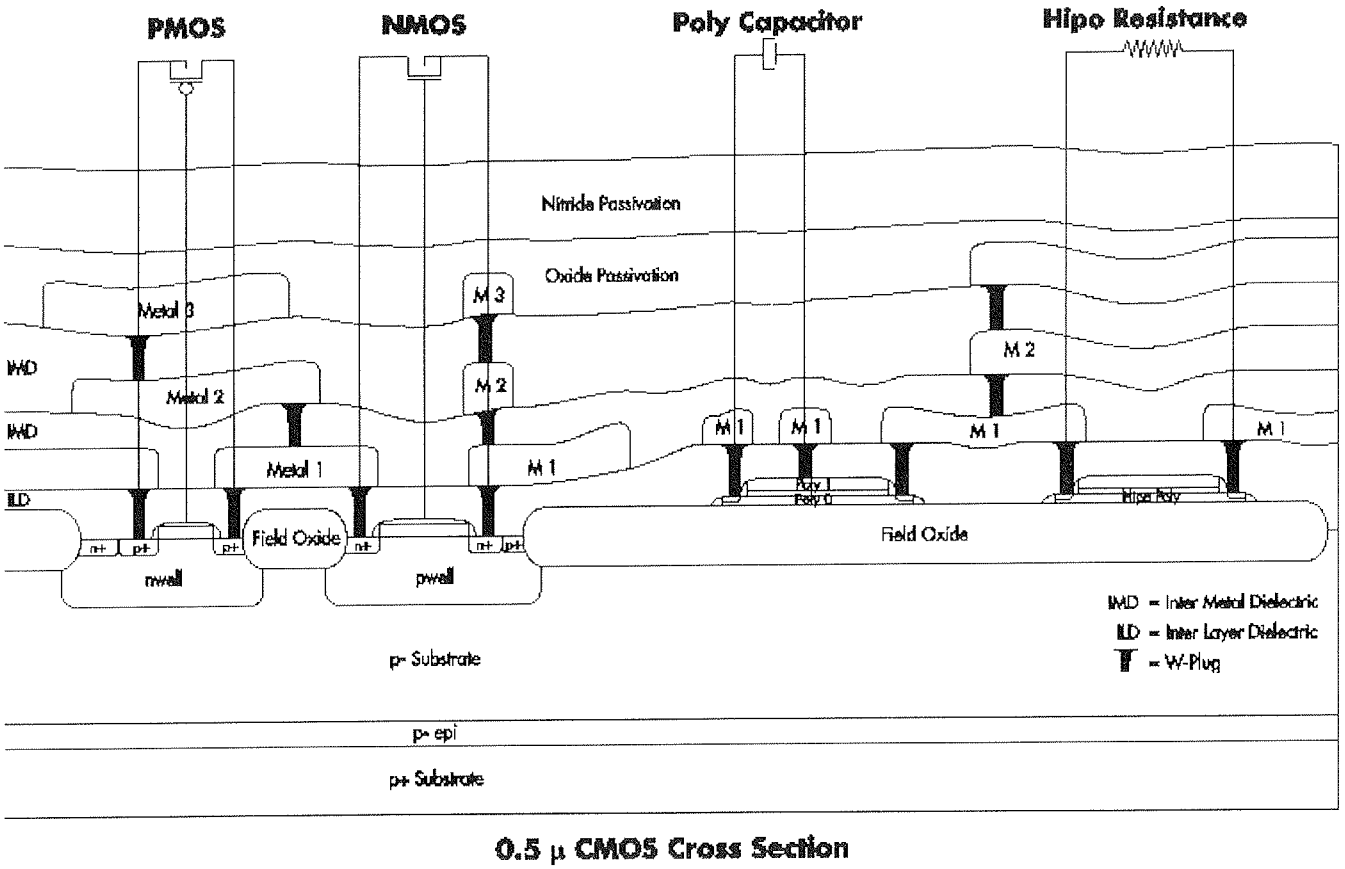

Fig. 6 C05A Cross Section

Two other techniques are the well known ATPG and the use of JTAG, Boundary Scan.

Finally reliability data are provided in the documents to determine the expected live time of circuits stressed under extreme conditions. This allows the designer to anticipate design tuning to maximise the life-time.

2.4 C05 Libraries & Document reference

C05 Libraries

core digital library (Doc)	MTC 35000
high profile IO (Doc)	MTC 35100
low profile IO (Doc)	MTC 35200
5V safe IO (Doc)	MTC 35300
medium profile IO (Doc)	MTC 35400
ROM RAM compilers (Doc)	MTC 35500
functional blocks (CD ROM)	MTC 8332: 32bit RISK, MTC 8308: 8bit μRISC, etc.
functional blocks Analog library	MTC 35800

C05 Documentation

the available material	.. and where ..
the C05 data sheet MTC 35000	CD ROM
SPICE Models for C05M BSIM3V3	DS 13314 CONTROLLED DOCUMENT
C05M-D Design Rule Manual	DS 13315 CONTROLLED DOCUMENT
C05M-A Design Rule Manual	DS 13316 CONTROLLED DOCUMENT
C05 Scribe Lane Insert Description	DS 10994 CONTROLLED DOCUMENT
Assembly Layout Rules	DS 13600 CONTROLLED DOCUMENT
the ADS reference manual	DOCUMENT
the ADS data sheet	CD ROM
the software development tools	CD ROM
and more on the web http://www.alcatel.com/telecom/micro	

Fig. 7 C05 Libraries & Document reference

3 ADS Asic Design System

3.1 ADS description

ADS is the result of thoroughly re-engineering the design methodologies that have supported the growth of the Alcatel Semiconductor Company on the market place. This effort is now released in a new quality-driven and consistent front-end and back-end environment.

ADS is an open design system, based on the best commercial tools and standard interfaces between them (EDIF, Verilog, VHDL, SDF, PDEF, GDSII). The entry of the ADS system is RTL-level both in Verilog HDL and VHDL language. ADS offers, through the complete design flow, a consistent concept of timing constraints and delay, delay calculation, and library timing information. Based on this, ADS provides a tight coupling between engines for logic synthesis and place & route. This enables the ADS system to converge quickly to a design that meet the initial timing constraints.

Within ADS front end, both Verilog & VHDL and co-simulation tools can be used. For the backend operation, Avant! floor-planning and place & route tools are supported. ADS provides an accurate characterisation of the libraries done at worst case with guaranteed accurate de-rating within a restricted range of voltage and temperature.

ADS is a mixed mode design system. The realisation of analog blocks is done by using the most advanced design methodology for the analog components. ADS supports behavioural (HDLA) description of analog circuits. This allows to implement high level description of circuits that are used for the specification distribution during the co-design phase. In-depth design and verification of the analog circuits are done at the transistor level with SPICE simulation. Finally, top-level simulation is possible by running mixed mode simulation. Last but not least ADS is used to control the backend integration.

In addition, ADS allows the mapping of the most common FPGA prototypes. The documentation is provided through an easy to use on-line documentation tool. ADS quality is ensured by a dedicated QA-flow whenever a new tool release is supported by the environment.

3.2 The value added re-usable blocks

ADS includes several compilers for ROM and RAM blocks, as well as a long list of high added-value Application Specific Standard Blocks (ASFB) in the telecom and data-processing area.

ADS brings into the design flow a family of embedded 8bit, 16bit and 32bit RISC μ-cores, capable to deliver up to 30 MIPS, and microprocessors peripherals: UART, DMA, IRQ, PIC, RTC, ..., and telecommunication blocks: ISDN interface, HDLC controller, RS encoder, QAM demodulator, ... (see also our Internet web site: http://www.alcatel.com/telecom/micro).

The ASFB strategy supports also value added analog blocks like broadband and/or high dynamic A/D and D/A converter, PLL, pass-band filters.

4 THE QUALITY

Alcatel Microelectronics is a quality-minded company.

A state of the art Average Quality Level (AQL) of 3ppm is the result by today of a long and continuous improvement of the quality system put in place to track the defects. Methods like Iddq (test of Idd leakage current @Vdd_nom & all bias off) and Vstress/Vscreen (some real test-pattern, e.g. ScanPath, @ 1.4xVdd_max) are standard test methodologies put in place to reduce the AQL-level to the target number of 0.5ppm in the year 2000.

This commitment to the quality has been re-enforced by the decision to fulfil the QS9000 by year 1999.

5 CMOS ROADMAP

The commitment of Alcatel Microelectronics to the state of the art mixed mode technologies is dedicated to mixed CMOS.

The 0.5 μm mixed CMOS technology and the I²T technology (0.7 μm mixed high voltage CMOS) are in production since begin 1996.

The 0.35 μm digital CMOS technology is in production since end 1997.

The analog 0.35 CMOS technology is in prototype phase since mid 1998 and will be released for production begin 1999.

The next generation will be 0.25 μm digital CMOS, start of the prototype phase is spring 1999, production release is forecasted begin 2000.

6 0.35 μm Mixed CMOS Technology preview

Based on the same technology route as the 0.5 μm CMOS, the mixed mode CMOS 0.35 μm will be available fall 98. This technology provides an increased digital density: About a factor of 4. It is based on a five-layer metal obtained by Chemical Mechanical Planarisation (CMP). This technology makes use of amorphous silicon gates.

Analog options C035A, target parameters

second Poly layer, capacitor	Poly0-Poly1 linear capacitor, 1.1nF/mm2, tol ±10%, Vcl <20ppm/V, Vcq <10ppm/V, matching <0.1% (3 sigma) @W/L = 20/20
high-ohmic Poly resistor	1kΩ/sq, tol ±10%, voltage linearity: < 300 ppm/V temperature coefficient: < 2000 ppm/°C matching <0.5% (3 sigma) @W/L = 5/50
bipolar transistor	vertical PNP

Fig.8: C035 Analog options

7 CONCLUSION

Alcatel Microelectronics, leader of the mixed mode ASIC market, is bringing the technologies for the mixed-mode system-on-a-chip. This strategy is the result of an important investment in the technologies and design methodologies fitted for sub-micron design. This important step in the mixed mode design shows the move from large analog / small digital (Ad) to the large digital / small analog (Da) chip manufacture technique. This strategy is supported by a continuous improvement of the product quality.

Finally, the commitment of Alcatel Microelectronics to the state of the art mixed mode technologies is now continued in the set-up of the first 0.35 μm mixed mode technology.

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Hans Gugg-Schwaiger
Alcatel Microelectronics
Arabellastrasse 4, D-81925 München, Germany
e-mail: hans.gugg-schwaiger@mie.alcatel.be

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