CHARACTERISATION AND MEASUREMENTS OF SILICON DETECTORS

Valter Bonvicini

INFN-Sezione di Trieste, Italy

TUTORIAL INVITED PAPER
MIDEM'98 CONFERENCE – Minisymposium on Semiconductor Radiation Detectors
23.09.98 – 25.09.98, Rogaška Slatina, Slovenia

Keywords: silicon radiation detectors, electrical parameters, parameter measurements, parameter influence on performance, energy resolution, position resolution, bias circuits, ENC, Equivalent Noise Charge, FOXFET, Field OXide Field Effect Transistors, GCD, Gate-Controlled Diodes

Abstract: An overview of the principal techniques and methods used to characterise silicon radiation detectors is given. These techniques allow to measure the most important electrical parameters of the detectors (leakage current, junction and inter-electrode capacitance, depletion voltage, etc.). The influence of these quantities on the detector's performance and on the achievable energy and position resolutions is discussed. Their knowledge is also of fundamental importance for the construction and understanding of the detector functional models. Experimental measurements illustrating the characterisation in the laboratory of some of the most used types of silicon detectors are given.

Karakterizacija in meritve silicijevih detektorjev

Ključne besede: detektorji sevanja silicijevi, parametri električni, merjenje parametrov, vplivi parametrov na zmogljivost, ločljivost energijska, ločljivost položajna, vezja napajalna, ENC naboj šumni ekvivalentni, FOXFET transistorji z učinkom polja poljsko-oksidni, GCD diode z vrati krmiljenimi

Izvleček: Prispevek podaja pregled glavnih tehnik in metod za karakterizacijo silicijevih detektorjev sevanja. S pomočjo teh metod lahko izmerimo najbolj pomembne električne parametre detektorjev (zaporni tok, kapaciteta spoja in med elektrodami, napetost osiromašenja itn.). Obravnava tudi vpliv teh parametrov na delovanje detektorja in na dosegljivo energijsko in pozicijsko ločljivost. Poznavanje teh parametrov je v osnovi pomembno za načrtovanje in razumevanje funkcijskih modelov detektorja. Podani so tudi eksperimentalni rezultati, kot primer karakterizacije nekaterih najbolj uporabljenih silicijevih detektorjev v laboratorijskem okolju.

1. INTRODUCTION

Semiconductor detectors are nowadays one of the most powerful tools for radiation detection and measurement in many experimental physics research fields. High Energy Physics, Nuclear Physics, Cosmic and Gamma-ray Astrophysics, Medical Imaging, X-ray spectroscopy, have all taken great advantage from the impressive development of the semiconductor detector technology during the last 20 years. Although germanium is still widely used, for its high efficiency, in gamma and X-ray spectroscopy, and although research and development in other semiconductor materials (such as GaAs, for instance) are giving encouraging results, silicon remains undoubtedly the most used and reliable semiconductor material for detector fabrication. The possibility to realise high-resistivity, high-purity substrates with very high mobility and lifetime of the charge carriers and the existence of an advanced, reliable and continuously upgraded technology (the planar process of the microelectronics) have determined its success. Actually, the application of the planar process to the production of silicon detectors (first introduced by J. Kemmer in 1972 /1/) was a landmark in the development of these devices. Since then, starting from the simple single-sided microstrip detectors, increasingly sophisticated detectors for position and energy measurements have been produced and employed: microstrip detectors with integrated coupling capacitors and DC-biasing structures /2/, double-sided microstrip detectors with both p-implant /3, 4/ and field-plate sepa-

ration /5, 6/ of the n^+ strips, silicon pixel detectors /7, 8, 9/, Charge Coupled Devices (CCDs, /10/), Silicon Drift Detectors (SDDs, /11, 12, 13/), fully-depleted p-n CCDs /14, 15/. Whatever the type of the device, an accurate laboratory measurement of its electrical parameters is of fundamental importance for a correct detector operation in the experiment and for obtaining the desired performance. Basically, the laboratory characterisation has to allow for:

1) ensure that, for a given device, all the functional parameters are within the previously fixed acceptance limits;

2) study and understanding the electrical model of the detector;

3) control the technology and possibly give a feedback for improving some processing steps.

In the next Section, the influence of the detector's parameters on the overall signal-to-noise ratio and, hence, on the achievable resolution of the system (detector + readout electronics) will be reviewed. In Section 3, the basic techniques for detector characterisation will be illustrated with examples of measurements performed on different detector types. Section 4 briefly illustrates the importance of the measurements performed on *ad hoc* designed "test structures" for the determination of extremely important quantities (such as the charge carrier generation lifetime, for instance). Finally, conclusions are drawn in Section 5.

2. DETECTOR, BIAS NETWORKS AND EQUIVALENT NOISE CHARGE

Figure 1 sketches the layout of a generic charge measuring system. The detector is modelled as a capacitive current source, delivering in a very short time a charge Q on the parallel of the total detector capacitance C_D and the preamplifier input capacitance C_i. It should be noticed that the real preamplifiers usually differ from the simple voltage-sensitive configuration of Figure 1, but the general concepts introduced hereafter are practically independent on the preamplifier's configuration.

The noise sources of the system can be represented by a series voltage generator with a spectral power density $a(\omega)$ and by a parallel current generator with a spectral power density given by $b_1(\omega) + b_2(\omega)$ /16/.
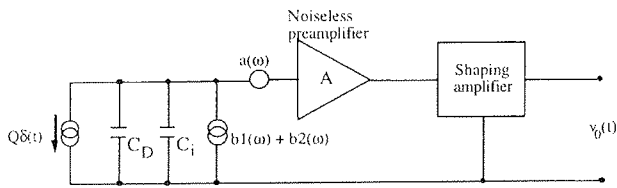

Fig. 1. *General representation of an analogue front-end for charge measurement, with the noise sources represented by the equivalent generators $a(\omega)$ and $b1(\omega) + b2(\omega)$.*

The term $a(\omega)$ is characteristic of the preamplifier and in general we have:

$$a(\omega) = a_1(\text{white}) + \frac{a_2}{|\omega|} \qquad (1)$$

where the term a_1 is due, depending on the type of input active device employed, whether to the shot noise in the collector current for a BJT or to the thermal noise in the channel for an FET (both junction and MOS). In Eq. 1, the "$1/\omega$" part of the series spectral power density is negligible for BJTs, small for JFETs and rather important for MOSFETs and GaAs MESFETs /16, 17/.

The parallel noise is split into two terms: b_1, which is again a contribution of the preamplifier (shot noise in the base current or in the gate current for a BJT or a JFET, respectively; it is virtually negligible for a MOS-FET) and b_2, which is contributed by the detector and by the bias networks. Focusing now our attention on b_2, we have in general to distinguish two cases:

a) the detector is DC-coupled to the preamplifier (Figure 2a);

b) the detector is AC-coupled to the preamplifier (Figure 2b).

For the sake of simplicity, in both cases of Figure 2 the preamplifier uses as input active device a JFET and again the preamplifier is sketched as a voltage-sensitive one. Independently on the type of coupling, the detector contributes to the term b_2 in the power spectral

density of the parallel noise source of Figure 1 with a term

$$\Sigma_{det} = qI_L \qquad (2)$$

describing the shot noise associated to the detector's leakage current. Moreover, in the AC-coupling of Figure 2b there are two sources of thermal noise: one associated with the JFET bias resistor R_G and the other associated with the detector bias resistor R_P. The resulting spectral power density is given by

$$\Sigma_T = 2kT\left(\frac{1}{R_G} + \frac{1}{R_P}\right) \qquad (3)$$

Therefore, from Eqs. (2) and (3) we have that, in the case of AC-coupling, the parallel noise generator b_2 of Figure 1 has the following expression:

$$b_2 = qI_L + 2kT\left(\frac{1}{R_G} + \frac{1}{R_P}\right) \qquad (4)$$

Clearly, for the configuration of Figure 2a (DC-coupling), the expression is

$$b_2 = qI_L + \frac{2kT}{R_G} \qquad (5)$$

So far we have seen that two parameters of the detector (namely, its leakage current and, when present, its bias resistor) represent two noise sources that enter into the formulae describing the parallel noise. But another detector parameter, though being not a physical noise
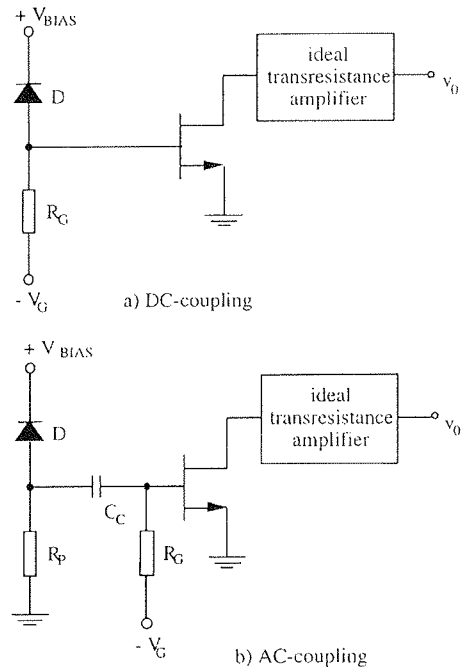

Fig. 2. *Schematic illustration of the two types of coupling between detector and preamplifier. The detector is modelled as a diode D reverse-biased by the applied voltage V_{BIAS}.*
a): DC-coupling; b): AC-coupling.

source, is of key importance in determining the noise level of the read-out electronics. This is the detector load capacitance C_D, i. e. the total capacitance presented by the detector at the preamplifier's input. It can be shown /16/ that the general expression for the Equivalent Noise Charge (ENC, that is the amount of charge at the input for which the signal-to-noise ratio at the output reduces to unity) for a system like that of Figure 1 can be written as:

$$ENC = \left[h_1 \frac{a_w}{\tau_M} (C_D + C_i)^2 + h_2 a_{1/f} (C_D + C_i)^2 + \right.$$

$$\left. + h_3 (b_1 + b_2) \tau_M \right]^{1/2} \qquad (6)$$

where h_1, h_2 and h_3 are numerical constants whose values depend on the particular type of shaping and τ_M is the shaping time. In Eq. (6) the explicit form of a_w, $a_{1/f}$, b_1 and b_2 depends, as we have seen, on the type of active input device in the preamplifier and on the type detector-preamplifier coupling. Therefore, the detector parameters play an essential role both in the series white noise (through the detector capacitance C_D) and in the parallel noise (through the spectral power density b_2).

The relative amount of signal charge and noise determines the energy and position resolution (and even the detectability of the signals) in all devices mentioned in Section 1. In the case of detectors with segmented electrodes (such as silicon microstrips) it is well known that analogue readout of the signals collected by the strips permits the use of interpolation methods that greatly enhance the position resolution /18/. For example, let us consider a microstrip detector having an amplifier pitch p_a; if the centre-of-gravity method is used as interpolation algorithm, than the achievable position resolution σ is given by /19, 20/:

$$\sigma \approx \frac{a_{cf} \cdot ENC \cdot p_a}{Q_s} \qquad (7)$$

where ENC is the equivalent noise charge for one amplifier, Qs is the signal charge produced by the ionising particle and a_{cf} is a constant called "centroid finding constant", which determines the error in centroid finding and whose value depends on the correlation of the noise from adjacent preamplifiers and on the number of preamplifiers used in centroid finding. For example, for uncorrelated noise and using the outputs of 3 adjacent preamplifiers, $a_{cf} \approx 2$.

3. MEASUREMENT OF DETECTOR PARAMETERS

3.1 General considerations

As it is well known, analysis and characterisation of semiconductor "bare" (i. e. not encapsulated) devices should be performed in adequate environments ("clean rooms") with dedicated equipment and adopting precise precautions for handling. Silicon radiation detectors do not constitute an exception to this rule. The basic instrumentation for silicon detector tests consists of a

"probe station", i.e. a micrometric table with a microscope mounted on top of it. The DUT (device under test) is mounted on a special support (the "chuck") and held in place by vacuum. Special coaxial probes terminating with tungsten (or tungsten carbide) needles are used to contact the micrometric structures on the device. The needles can be moved accurately under the microscope by micrometric screws. Probe stations can be either manual or automatic and in the last case the movements are executed by computer-programmed stepping motors. Often, when dealing with highly segmented detectors (e. g. microstrips), special printed circuit boards, called "probe cards", are used. These boards can house a large number of needles with the same pitch as the structures to be contacted on the DUT, thus speeding up and simplifying the measurements.

The probe station is usually enclosed in a grounded metallic box that has the twofold function of keeping the DUT in a dark ambient and acting as a Faraday's cage. Coaxial cables are used to connect the probes (hence, the DUT) to the measuring instruments. A very basic equipment should consist of a voltage source-measuring unit (with a very high input impedance, in order not to affect the voltage measurements), a current source-measuring unit, a high-frequency C-V analyser and a quasi-static C-V meter. Often, some of these functions are performed by units integrated into a single instrument. Clearly, besides the above mentioned "minimal" instrumentation, other instruments usually equip a silicon detector laboratory. Unless otherwise specified, all the examples of measurements described in the next Subsections were performed in the Laboratory for Silicon Detectors of the Trieste INFN Section.

3.2 Leakage current measurements

Basically, all measurements of leakage current consist in doing an I-V characterisation of the diode(s). The number of contacts to be implemented on the device clearly depends on its type, biasing scheme and complexity.

For example, Figure 3 shows the results of a measurement performed on a DC-coupled pad detector de-
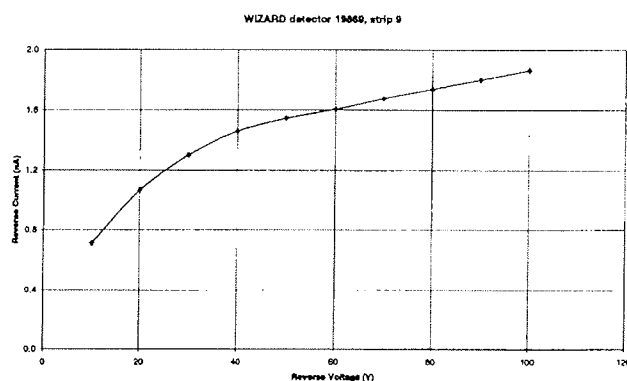

WiZARD detector 19569, strip 9

Fig. 3. Example of the measured leakage current as a function of the reverse voltage for one strip (implantation area of 59 x 3.6 mm^2) of a WiZard detector (manufactured by Canberra Semiconductors N.V., Belgium)

signed and realised for the silicon-tungsten imaging calorimeter of the balloon-borne experiment WiZard for the search of anti-matter in Cosmic Rays /21/. The whole calorimeter is made by 1024 detectors arranged in 8 planes (each plane has two "views", one X and one Y), for a total surface of 3.68 m² of silicon. Each detector has dimensions of 6x6 cm², is 380 μm thick and has 16 pads or large strips with a pitch of 3.6 mm. A metallized p⁺ implantation, the guard ring, surrounds the whole sensitive area and serves to collect the edge currents. For the strip shown, the current is about 1.5 nA/strip at full depletion, that was measured to be 55 V. The fact

that the current does not saturates after the full depletion voltage indicates that, besides the bulk generated current, there is a non negligible contribution from the surface generation. A discussion of the contributions from bulk and surface generation to the leakage current is done in Section 4.

An important item to be controlled when analysing the leakage current is its stability in time. It is in fact well known that the reverse currents in a silicon detector may vary of orders of magnitude depending on the environmental conditions, sometime even many hours after having biased a seemingly perfect detector /22/.

These phenomena can be attributed to the charges trapped on the outer oxide surface. For example, if an uncovered oxide surface is exposed to humidity, typically negative charges are collected on that surface. These charges provoke the formation of an inversion layer under the oxide and this leads to an extension of the depletion region towards the detector's edge (Figure 4 a, b, c). If the depletion region reaches this edge, the current may increase by orders of magnitude due to the generation of electron-hole pairs in the crystal lattice damaged by the cut. On the other hand, in the presence of no or positive charges on the oxide surface (that may happen for instance in a very dry environment or in vacuum), the positive oxide charge at the Si-SiO2 interface is undisturbed in creating an electron accumulation layer in the silicon below the oxide. This may lead to very strong electric fields at the junction edges, and even to a junction breakdown for potentials lower than the full depletion one. Again, the detector's surface may be protected by a highly resistive layer (such as polyimide), which may be charged by the metal electrodes in an unpredictable way because of local variations in the material's resistivity. Therefore, a careful stability measurement of the leakage current is mandatory. Figure 5 shows the result of such a measurement performed on a WiZard detector for 112 hours at the operating bias voltage (that in this case was defined as 10% above full depletion). As it can be seen, the reverse current presents an excellent stability.

Usually, the selection of detectors is made on the basis of the current in the active area, this means that the current collected by the guard ring(s) is of no matter in the acceptance or rejection of a device. Nevertheless, this is not the case for balloon or satellite-borne devices.
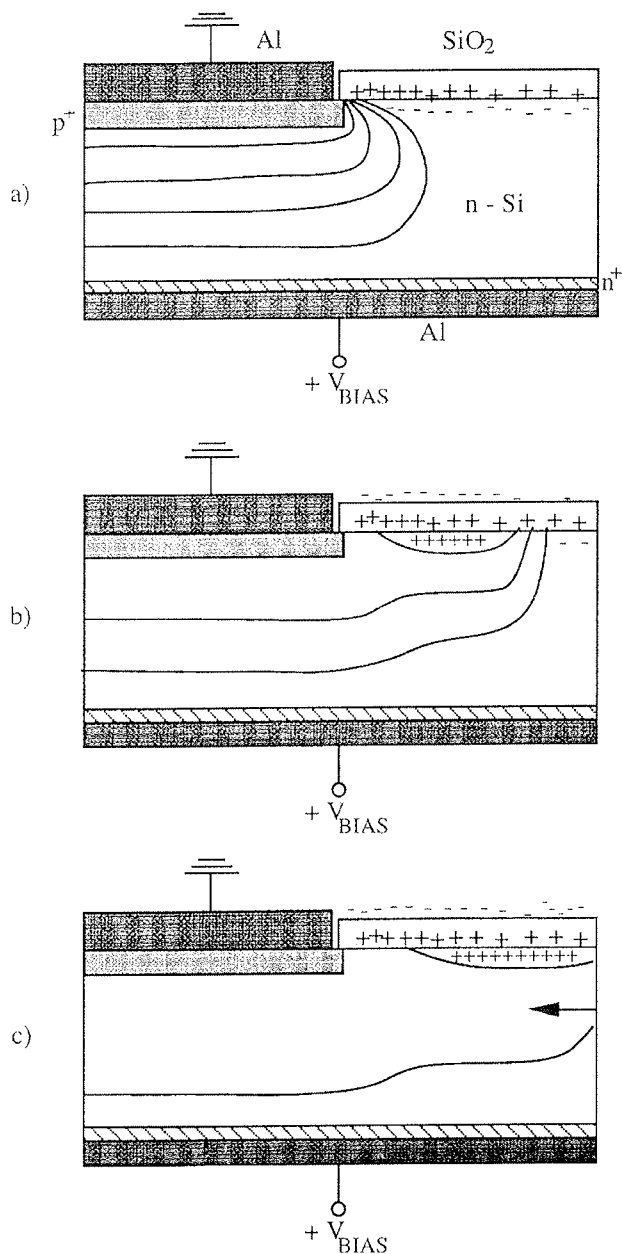

Fig. 4.   Influence of environmental conditions on detector characteristics: a) without negative charge accumulation on outer silicon surface (high field at the junction edge); b) inversion layer due to accumulation of negative charge on the surface; c) extension of the depletion region to the damaged detector edge.
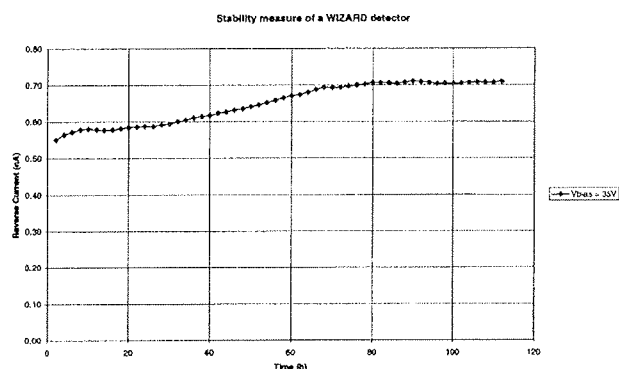

Fig. 5.   Result of a stability measurement (112 h) performed on a WiZard strip detector (manufactured by SINTEF, Oslo, Norway). The current on a single strip is shown.

Since in these experiments a very limited power budget is available, a large or unstable (continuously increasing) current is not acceptable, even if it does not affect the detector's performance.

3.3 Integrated biasing structure measurements: the FOXFET

In case of AC-coupled strip detectors, a DC-biasing structure for the strip leakage currents has to be provided. This can be accomplished either with polysilicon resistors of suitable value, which connect each strip to a common bias line /2/, or by a punch through effect from a guard ring /23/. With this last technique it is possible to avoid the polysilicon steps in the processing, thereby using for capacitively coupled detectors the same technology as for direct coupled ones. Sometimes, a metal gate electrode is placed on the oxide that covers the gap between the strips and the guard ring (Figure 6). In this way, by varying the gate potential, one can control the strip voltage. This gated punch through structure is usually referred to as a FOXFET (Field OXide, Field Effetct Transistor) /23, 24/. Since the gated punch through biasing technique presents more interesting items of discussion from the point of view of the measurements, it will be used as an example in this Subsection. In order to introduce the measurements to be performed on this structure, a brief and qualitative summary of its working principle is given hereafter. The interested reader can find a detailed, quantitative analysis in the literature /24-31/. The measurements shown here were performed on AC-coupled microstrip detectors designed and realised for the SYRMEP experiment (SYnchrotron Radiation for MEdical Physics), a digital radiology program which is in operation at the ELETTRA Synchrotron light source in Trieste, Italy. All details about the detector's design and performance can be found in Ref. /32/.

In the usual biasing scheme, the drain (i.e. the biasing guard ring) is held at ground potential with respect to the positive bias voltage applied to the backplane. As V_{BIAS} increases, the depletion layer of the drain junction
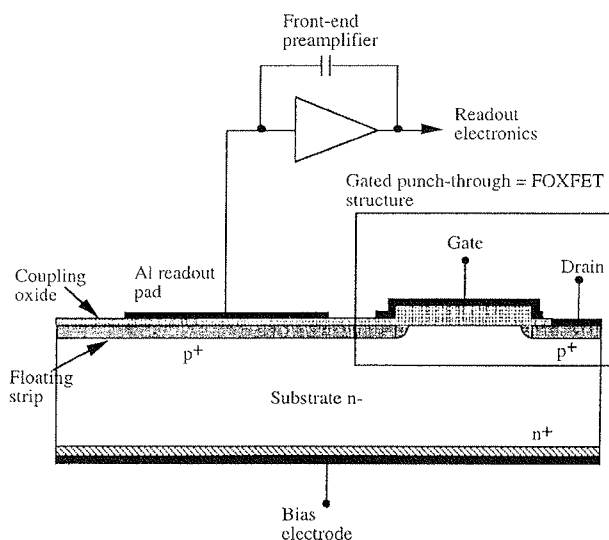
extends both towards the bulk and laterally towards the floating p+ strip. At the surface, a strong accumulation layer of electrons exists, which is due to the positive oxide charge in the field oxide /28/; obviously, this accumulation layer effectively inhibits the spreading of the depletion layer at the surface. Therefore, the two junctions are "isolated" and a potential difference is established between them as V_{BIAS} increases. Hence, since the strip is floating, its potential initially "follows" the bias voltage: Figure 7 shows a typical measured strip voltage as a function of V_{BIAS}, with the gate voltage (V_{GATE}) as parameter.
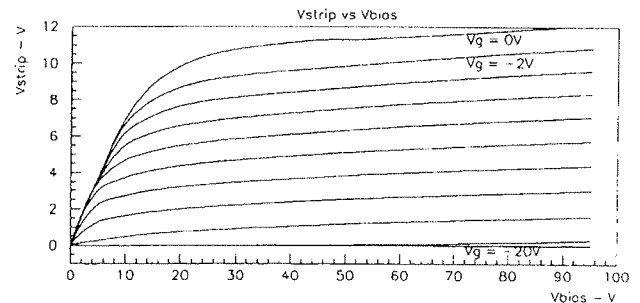

Fig. 7. *Typical result of a strip voltage vs. bias voltage measurement (with the gate voltage as a parameter) performed on a Syrmep microstrip detector (manufactured by Canberra Semiconductors N.V., Belgium)*

The input impedance of the measuring instrument (Hewlett Packard 4142B) was $> 10^{12}$ Ω, and therefore the strip voltage was practically not affected by the measurement. When the punch through between the two junctions (the strip and the drain junctions) is reached, the strip voltage tends to settle and an effective reverse bias exists between the strip and the n bulk. In terms of current, the mechanism can be described in the following way: since the strip junction is reverse biased towards the substrate, it needs to be forward biased in a certain point in order to satisfy Kirchhoff's Current Law (condition of zero net current entering and escaping the strip). As a result, the strip leakage current (holes from the n-type substrate) is injected back into the substrate and flows through the channel into the drain junction as punch through current /31/. It should be noticed that this current flow does not take place at the silicon-oxide interface, but rather in the bulk of the device, a few microns below the surface, due to the presence of the electron accumulation layer /29, 31/.

By applying a negative voltage to the gate electrode, the punch-through voltage gets smaller, since the applied field partly compensates the one due to the positive oxide charge, thereby reducing the electron accumulation layer. At a certain gate voltage (- 20 V in Figure 7), the applied field is strong enough to fully compensate the positive oxide charge; the accumulation layer at the Si-SiO2 interface vanishes and the strip voltage is zero, indicating that the channel is close to the inversion mode and therefore the transistor is turning on. The biasing structure showed excellent results for all the measured detectors; the maximum variation of the strip voltage over 256 strips was 3.1 V, while the

Fig. 6. *Schematic illustration of a detector structure with AC-coupled floating strip junction and FOXFET biasing structure.*

local variations among neighbouring strips were always below 0.4 V. The resulting distortions in the drift field are practically negligible.

A very important parameter in the FOXFET is the so-called dynamic resistance, defined as

$$R_d = \frac{\partial V_{STRIP}}{\partial I_{STRIP}} \qquad (8)$$

where V_{STRIP} is the strip voltage and I_{STRIP} the current flowing from the strip to the drain. As we have seen in Section 2, the value of the bias resistor in AC-coupled detectors enters into the expression of the spectral power density of the parallel noise generator b_2 (see Eq. 4). In order to minimise this contribution, the value of R_d has obviously to be large. In the case of the Syrmep detector-electronics system, values of dynamic resistance below 20 MΩ start to contribute significantly to the total noise /32/ The dynamic resistance value is known to be determined (for a given FOXFET geometry) almost entirely by the leakage current: it is extremely high at low currents and it decreases as the current increases approximately as I^{-1}; the dependence of R_d on the gate voltage is very poor, at least until the transistor threshold voltage is reached /28, 31/. When characterising FOXFET-biased detectors, one is mainly interested in measuring the dynamic resistance in operating conditions, i.e. as determined by the leakage current flowing in the strip at operating bias voltage. This means to force small variations of strip current around the "quiescent" value I_L and record the corresponding changes in strip voltage V_{STRIP}. To do so, we used the measurement set-up schematically illustrated in Figure 8; the current monitor/source that was used can measure currents down to 100 fA.

A typical result is shown in Figure 9; here, $I_s = 0$ means that no current flows from or to the external current source, i.e. the strip current is the quiescent leakage current I_L. For negative values of I_s the instrument acts as a current sink, while for positive values of I_s the instrument adds current to I_L. The dynamic resistance,

obtained as the slope of a linear fit of the measured points, was about 60 MΩ for this strip, which corresponded to a leakage current of $\approx$ 1.5 nA.

3.4 Capacitance measurements

As it was evidenced in Section 2, load capacitance is one of the most significant parameters determining the noise level of the readout electronics. Let us first consider the case of microstrip detectors. In this case, the significant contributions are those from the other strips on the detector surface and also from the backplane. The relative importance of these two contributions depends on the detector characteristics: implant and metal strip pitch and width, capacitive or direct coupling to the readout electronics, type of doping, etc. /33/. As a general statement, one can say that if the strip pitch is much smaller than the detector thickness, the interstrip capacitance C_{is} between two adjacent strips dominates over the junction capacitance C_j of a single strip to the backplane.
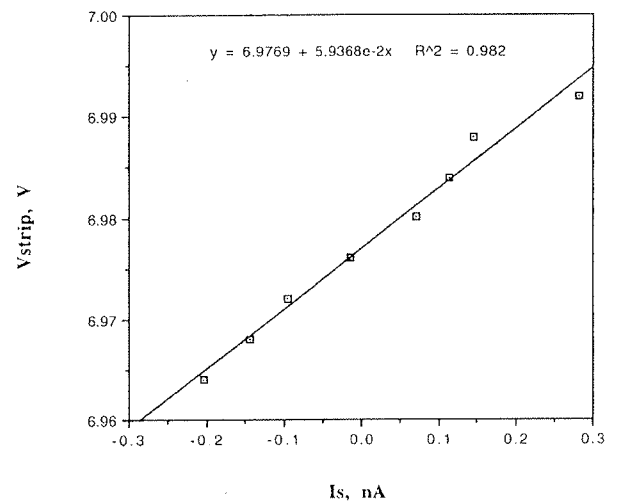

Fig. 9. Result of a dynamic resistance measurement: the value of R_d is obtained from a linear fit of the measured data.
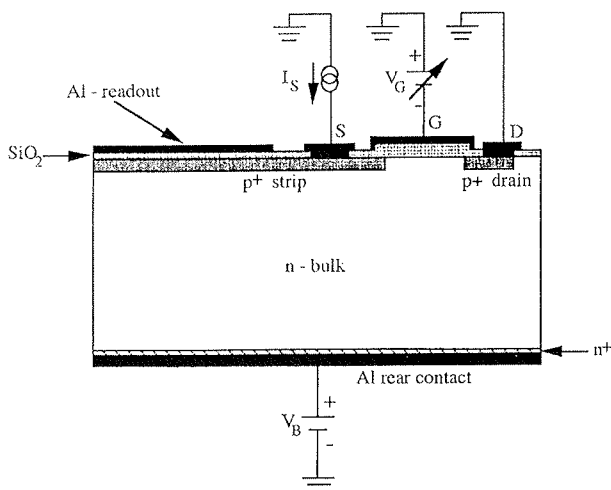
It is important to simulate the detector operation in real experimental conditions, where every strip is held at a well defined potential through an amplifier. To do so, one can use the stitchbonding technique to connect together all the strips except those which have to be measured (Figures 10 and 11). In this way, both junction and interstrip capacitance can be measured correctly. Figure 10 shows a diagram of the experimental set up employed to measure C_j on DC-coupled microstrip detectors /34/. The devices (manufactured by Canberra Semiconductors) had 52 strips each, having a length of 10 mm and a pitch of 200 μm. The implant width was 160 μm and the metal width 140 μm. The wafer thickness was 300 μm. A Keithley 590 CV Analyser was used; the measuring signal had a signal of either 100 kHz or 1 MHz and an amplitude of 15 mV rms. Data were taken at 100 kHz, but no significant differences were observed at 1 MHz. The strip under measurement was biased by keeping the backplane at a positive voltage with respect to the CV Analyser input.

Fig. 8. Schematic illustration of the set up used to perform the I-V and dynamic resistance measurements of the biasing structure.

When measuring low level capacitances, special attention must be paid to reduce parasitic effects. A subtraction of the parasitic capacitances (i.e. cables capacitance and capacitance between the probe contacting the measured strip and all other strips on the detector plane) has to be performed. With the above mentioned set up, this was done using the "open circuit correction" feature of the instrument. This consists in raising the probe tip of the strip under measurement at a fixed height (about 50 μm) and leaving all the rest equal. The
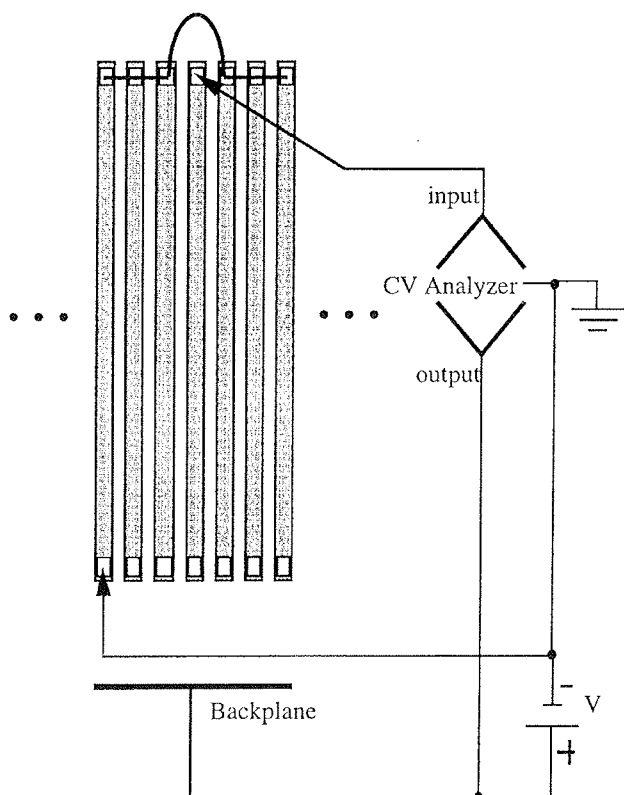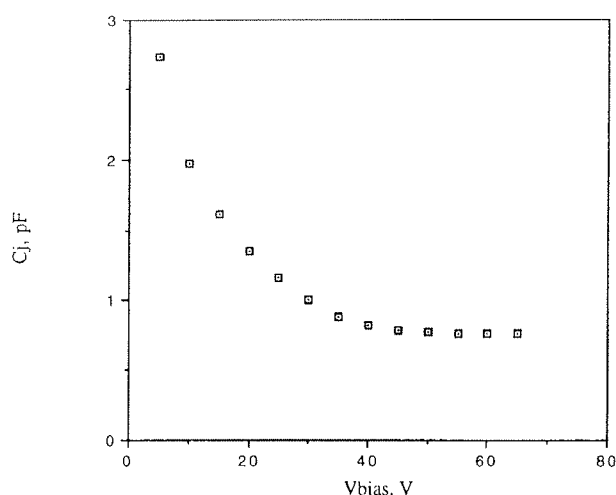
resulting parasitic capacitance measured is automatically taken by the instrument as the reference value ("zero") for the next measurements.

The typical junction capacitance measured is shown in Figure 11. The curve clearly shows the well known dependence on $1/\sqrt{V}$ expected for an abrupt junction (see Section 4). The measured C_j at full depletion was≈ 0.75 pF.

Figure 12 shows the circuit used for interstrip capacitance measurements. The stray capacitance subtraction method is the same. One central strip (the one under test) was left out and 50 strips (25 on both sides of the central one) were stitchbonded together. In that way it was possible to evaluate the contribution of farther strips by disconnecting strips or groups of strips starting from the outer ones. Hence one can measure the interstrip capacitance as a function of the number of adjacent strips. The results obtained experimentally are plotted in Figure 13 versus the number of strips connected. It is apparent from that plot that, for these particular detectors, more than 90% of the total interstrip capacitance is contributed by the two closest neighbours and that the contribution of the strips beyond the fourth neighbours is completely negligible.

The measuring techniques described so far in this Subsection obviously apply also to other types of segmented silicon detectors, like e. g. pixel detectors. The interpixel capacitance measurements are nevertheless more complicated, due to the geometry of the system. Moreover, if one tries to disentangle the different contributions to the measured total interpixel capacitance, there is the difficulty represented by the diagonal pixels, whose contribution is not trivially evaluable. The interested reader can find in Ref. /35/ a discussion of the

Fig. 10. Diagram of the experimental set up used for junction capacitance measurements.

Fig. 11. Result of a junction capacitance measurement on the microstrip structures described in the text.
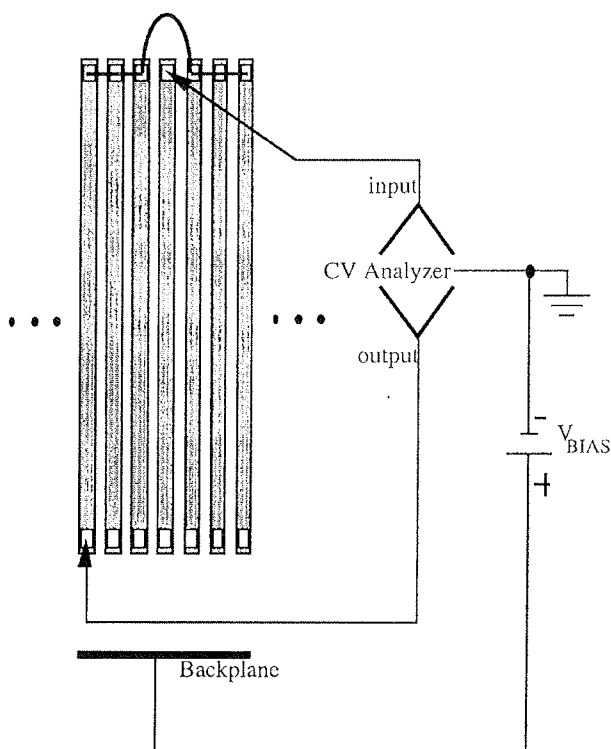

Fig. 12. Diagram of the experimental set up used for interstrip capacitance measurements.

pixel capacitances, together with a modellization of the interpixel capacitance on the geometry and experimental results on test structures.

When dealing with AC-coupled strip detectors, the basic considerations expressed so far still apply. Nevertheless, it should be clear that now that the quantity obtained by stitchbonding the metal readout lines (see Figure 12) and performing the above described measurement is effectively the capacitance of one strip with respect to its neighbours in real experimental conditions (that is what is more important for real applications), but is NOT, strictly speaking, the mere interstrip capacitance. In fact, what is measured in this case is a convolution of the coupling and interstrip capacitances. By constructing an adequate equivalent circuit of the capacitive network of the detector and knowing the value of the coupling capacitance, it is possible to calculate the true value of C_{is}. A measurement of the coupling capacitance C_c is therefore necessary. Anyway, besides the understanding of the capacitive model
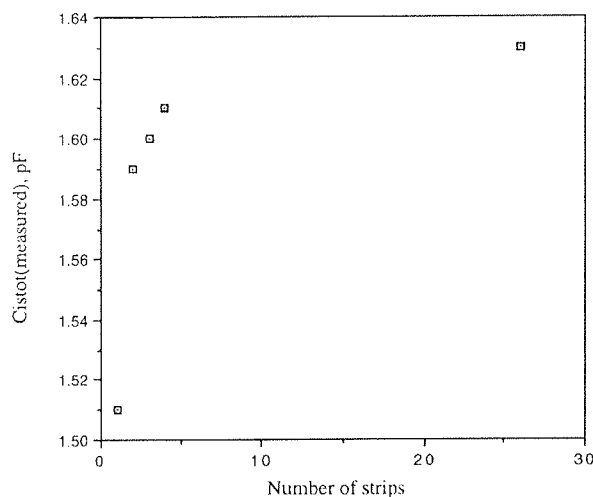

Fig. 13. Result of an interstrip capacitance measurement on the microstrip structures described in the text.
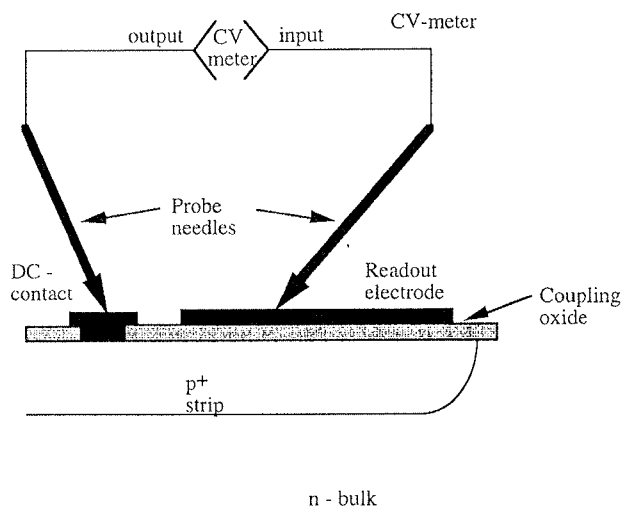

Fig. 14. Schematic of the circuit used to measure the coupling capacitors.

of the detector, this kind of measurement should be performed in order to control that the design value for C_c is met and to control the number of "pinholes", i.e. pierces in the coupling oxide. In AC-coupled detectors with integrated coupling capacitors, the rate of strips with pinhole defects is a key indicator of the quality of the oxide. The circuit to be used for coupling capacitance measurements is sketched in Figure 14. The coupling capacitance should be much larger (about 10 times at least) than between junction or interstrip capacitances, in order to avoid charge losses. For a correct measurement of C_c, a quasi-static CV meter has to be used.

4. MEASUREMENTS ON DEDICATED TEST STRUCTURES

A certain number of devices (called "test-structures") is always realised on the detectors' wafers, usually around the main detector. Their purpose is to allow measurements of important physical quantities that ultimately determine the detector performance. The most important of these parameters are the bulk doping density, the charge carrier generator lifetime, the surface generation velocity and the oxide charge density at the Si-SiO$_2$ interface. The first two can be measured using diodes, the third using gate-controlled diodes and the last using MOS capacitors /36/.

In a p-i-n diode a measurement of the junction capacitance versus the bias voltage shows the well-known dependence given by the following formula /37/:

$$C(V) = \frac{\varepsilon_0 \varepsilon_r S}{t\sqrt{V/V_d}} \qquad (9)$$

where V is applied reverse voltage, V_d the total depletion voltage, t the substrate thickness, S the diode surface, $\varepsilon_0 = 8.85 \cdot 10^{-12}$ F·m^{-1} is the vacuum permittivity and $\varepsilon_r = 11.8$ is the relative dielectric constant of silicon. The depletion voltage is better evaluated by plotting $1/C^2$ versus V (Figure 15, where $1/C^2$ is expressed in $1/pF^2$ and V in volts). The linear dependence up to the depletion voltage clearly indicates that the bulk doping is constant.

Another measurements that is usually performed on p-i-n test diodes is the I-V curve. For a good junction,
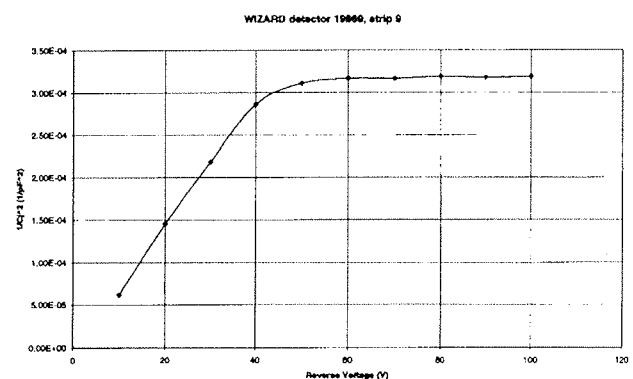

Fig. 15. Reverse bias voltage dependence of $1/C^2$: the full depletion voltage is clearly visible.

the reverse current should reach a plateau at total depletion; this would indicate that the current is practically due totally to bulk generation. If this is the case, the carrier generation lifetime τ can be evaluated according to the formula:

$$\tau = \frac{qn_iSt}{2I_L} \qquad (10)$$

where q is the electron charge, n_i the intrinsic carrier concentration, S the diode surface, t the wafer thickness and I_L the measured asymptotic value of the current.

With a gate-controlled diode (GCD) it is possible to measure the surface generation velocity. In this structure, a metal gate partially overlaps, on top of the oxide, the bulk and implant regions of a diode (see Figure 16). For gate voltages positive with respect to the flat band voltage V_{fb}, the surface of the n region is accumulated and the surface depletion layer is minimum /38/. Therefore, the leakage current is determined by the generation of electrons and holes in the "metallurgical" junction, whose area (in section) is indicated by S_M in Figure 16. By calling I_{GB} this bulk generated current, one has immediately from Eq. 10:

$$I_{GB} = \frac{qn_i}{2\tau}S_M x_{db} \qquad (11)$$

where x_{db} is the bulk depletion layer, that becomes equal to the wafer thickness τ at full depletion, and all other symbols are defined after Eq. 10.
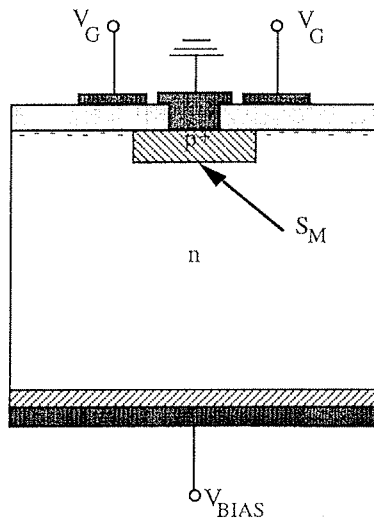

Fig. 16. A schematic cross section of a gate controlled diode structure for $V_G > V_{fb}$. In this case, the diode leakage current is virtually determined only by the generation in the "metallurgical" junction.

If the gate voltage V_G becomes more negative than the flat band voltage, the surface of the n region below the gate electrode is brought to depletion. Therefore, in addition to the current I_{GB}, there are now two other current components. First of all, there is a current due to the generation of carriers in the depletion region induced by the gate. This component, called "field induced junction current", is given by

$$I_F = \frac{qn_i}{2\tau}S_F x_{ds} \qquad (12)$$

where x_{ds}, the thickness of the surface depletion region, is a function of the applied gate voltage, and S_F, the area of the surface depletion region, is determined by the over-lapping of the gate electrode on the n region. The second current component which takes place when the surface is depleted, is due to the activity of the surface generation centres. This component is given by

$$I_S = \frac{qn_is_0S_F}{2} \qquad (13)$$

where s_0 is the surface generation velocity when the surface and the bulk are equi-potential /38/. The value of s_0 is directly proportional to the density of surface generation - recombination centres and is therefore strongly influenced by the process with which the device has been fabricated. Hence, the knowledge of s_0 is of great importance for the control and the improvement of the fabrication technology.

If the gate voltage is further decreased until the surface is brought to inversion, I_F in Eq. 12 increases to a maximum value when x_{ds} increases to its maximum value $x_{d,max}$. On the other hand, once the inversion has taken place, the surface hole density p_s is much larger than n_i and the surface generation velocity decreases strongly from the value s_0 /38/. Typically, $I_F < I_S$ when the surface is depleted; after inversion I_S becomes negligible and the reverse current becomes the sum of I_{GB} and I_F. In Figure 17 is reported the typical behaviour of the current experimentally measured in a GCD /36/. The three regions are clearly visible.
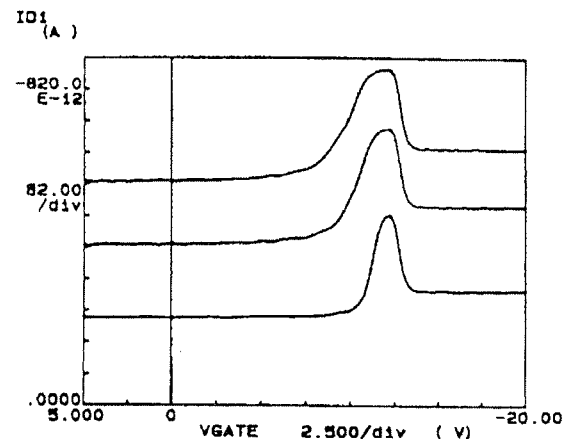

Fig. 17. GCD current versus gate voltage for three values of bias voltage (courtesy of L. Bosisio).

With MOS capacitors, an estimation of the oxide charge density Q_{ox} is possible by measuring the capacitance C as a function of the applied voltage V. The behaviour of the capacitance of an MOS structure as a function of the applied voltage is well known (/37, 38/): at low

voltages, the bulk is not depleted and the electron accumulation layer at the surface under the oxide is not perturbed. Increasing the reverse voltage V, the metal gate starts to be sufficiently negative (with respect to the bulk) to partially compensate the positive oxide charge, thereby reducing the electron accumulation layer. When the flat-band voltage (V_{fb}) is reached, the surface is brought in depletion mode. From the curve, the flat-band voltage V_{fb} can be determined and, assuming that the fixed oxide charges are concentrated at the interface, one can write /39/

$$V_{fb} \approx \frac{Q_{ox}}{C_0} = \frac{qN_F}{C_0} \qquad (14)$$

where N_F is the number of oxide charge at the Si-SiO$_2$ interface, q is the electron charge. C_0 is the geometrical capacitance per unit area, which is given by

$$C_0 = \frac{\varepsilon_0 \varepsilon_{ox}}{t_{ox}} \qquad (15)$$

where $\varepsilon_{ox}(SiO_2)=3.9$ and t_{ox} is the oxide thickness. From Eqs. (14) and (15) one can therefore estimate Q_{ox}.

5. CONCLUSIONS

This paper presented an elementary discussion about the laboratory characterisation of silicon radiation detectors. The relevance of the detector's parameters on the ENC, hence on the achievable energy and position resolution, has been overview. Some of the most important laboratory measurements have been illustrated with examples taken from experimental results. It has been shown that important physical properties of the silicon devices under test, that play a key role in determining the detector's performance, can be derived from standard measurements on simple structures.

REFERENCES

/1/ J. Kemmer, Nucl. Instr. and Meth. 169 (1980) 499.

/2/ M. Caccia et al., Nucl. Instr. and Meth. A260 (1987) 124.

/3/ P. Holl et al., Nucl. Instr. and Meth. A257 (1987) 587.

/4/ G. Batignani et al., Nucl. Instr. and Meth. A326 (1993) 183.

/5/ R. Brenner et al., Nucl. Instr. and Meth. A326 (1993) 198.

/6/ R. Brenner et al., Nucl. Instr. and Meth. A326 (1993) 189.

/7/ S. Gaalema, IEEE Trans. Nucl. Sci. NS 32 (1985) 417.

/8/ H. Heijne et al., Nucl. Instr. and Meth. A273 (1988) 615.

/9/ P. E. Karchin, Nucl. Instr. and Meth. A305 (1991) 497.

/10/ C. Damerell, Nucl. Instr. and Meth. 226 (1984) 26.

/11/ E. Gatti and P. Rehak, Nucl. Instr. and Meth. 225 (1984) 608.

/12/ E. Gatti, P. Rehak and J. T. Walton, Nucl. Instr. and Meth. 226 (1984) 129.

/13/ P. Rehak et al., Nucl. Instr. and Meth. A248 (1986) 367.

/14/ L. Struder et al, Nucl. Instr. and Meth. A253 (1987) 386.

/15/ E. Gatti et al., Nucl. Instr. and Meth. A288 (1990) 168.

/16/ E. Gatti and P.F. Manfredi, Riv. Nuovo Cimento 9, ser. 3, no. 1 (1986).

/17/ W. Buttler et al., Nucl. Instr. and Meth. A288 (1990) 140.

/18/ R. Turchetta, Nucl. Instr. and Meth. A335 (1993) 44.

/19/ V. Radeka and R. Boie, Nucl. Instr. and Meth. 178 (1980) 543.

/20/ V. Radeka, Nucl. Instr. and Meth. 226 (1984) 209.

/21/ M. Bocciolini et al., Nucl. Instr. and Meth. A370 (1996) 403.

/22/ A. Bischoff et al., Nucl. Instr. and Meth. A326 (1993) 27.

/23/ J. Kemmer and G. Lutz, Nucl. Instr. and Meth. A273 (1988) 588.

/24/ C. Bauer et al, IEEE Trans. Nucl. Sci. NS-36(1) (1989) 267.

/25/ P. Holl et al., IEEE Trans. Nucl. Sci. NS-36(1) (1989) 251.

/26/ P. P. Allport et al., Nucl. Instr. and Meth. A310 (1991) 155.

/27/ P. P. Allport et al., Nucl. Instr. and Meth. A348 (1994) 416.

/28/ M. Laakso et al., Nucl. Instr. and Meth. A326 (1993) 214.

/29/ N. Bacchetta et al., IEEE Trans. Nucl. Sci. NS-40(6) (1993) 2001.

/30/ N. Bacchetta et al., IEEE Trans. Nucl. Sci. NS-40(6) (1993) 1602.

/31/ D. Križaj, V. Bonvicini and S. Amon, Nucl. Instr. and Meth. A384 (1997) 482.

/32/ F. Arfelli et al., Nucl. Instr. and Meth. A385 (1997) 311.

/33/ S. Masciocchi et al., Proceedings of the 1992 IEEE NSS, Orlando (USA).

/34/ V. Bonvicini et al, INFN /TC-94/14.

/35/ V. Bonvicini et al., Nucl. Instr. and Meth. A365 (1995) 88.

/36/ G. Batignani et al., Nucl. Instr. and Meth. A360 (1995) 98.

/37/ S. M. Sze, "Physics of Semiconductor Devices", Wiley, 1981.

/38/ R. S. Muller and T. I. Kamins, "Device electronics for Integrated Circuits", Wiley, 1977.

/39/ D. K. Schroder, "Semiconductor Material and Device Characterisation", Wiley, 1990.

Valter Bonvicini
INFN-Sezione di Trieste
via A. Valerio 2, 34127 Trieste, Italy
e-mail: bonvicini@trieste.infn.it