FRONT-END ELECTRONICS FOR ENERGY AND POSITION MEASUREMENTS WITH SEMICONDUCTOR RADIATION DETECTORS

Valerio Re
Dipartimento di Ingegneria, Università di Bergamo, Italy
Lodovico Ratti
Dipartimento di Elettronica, Università di Pavia, Italy

TUTORIAL INVITED PAPER
MIDEM'98 CONFERENCE – Minisymposium on Semiconductor Radiation Detectors
23.09.98 – 25.09.98, Rogaška Slatina, Slovenia

Keywords: solid-state detectors, solid-state radiation detectors, energy measurement, position measurement, FEE, Front-End Electronics, X-ray spectrometry, GAMMA-ray spectrometry, X-ray imaging, GAMMA-ray imaging, particle tracking, HEP, High Energy Physics, state-of-the-art, problem solutions, design of implementations, ultra low noise, signal preamplification

Abstract: Semiconductor radiation detectors are presently used in many areas of physics research, from X and γ- ray spectrometry and imaging to particle tracking in high energy physics experiments. Front-end electronics have to comply with the requirements set by the different detector applications, such as low noise, to get high energy and position resolution, high speed, radiation tolerance and operation at cryogenic temperatures. Highly segmented detectors stimulated the development of readout circuits in monolithic form, and special integration technologies were purposely developed to achieve optimum performances. After reviewing the basic problem of front-end design, the paper presents solutions which have been adopted in specific applications, such as ultra low noise preamplification for X and γ- ray spectrometry, and analog processing of signals delivered by silicon microstrip detectors. The examined circuits range from all-JFET monolithic charge-sensitive preamplifiers, where a non resistive feedback technique can be used for minimum noise performances, to a mixed-signal multichannel CMOS integrated circuit containing the complete readout electronics for a silicon vertex tracker in a collider experiment.

Čitalna elektronika za meritev pozicije in energije pri polprevodniških detektorjih sevanja

Ključne besede: detektorji polprevodniški, detektorji sevanja polprevodniški, merjenje energije, merjenje položaja, FEE elektronika čelna, spektrometrija X-žarkov, spektrometrija GAMA-žarkov, upodabljanje X-žarkov, upodabljanje GAMA-žarkov, sledenje delcev fizikalnih, HEP fizika energij visokih, stanje razvoja, rešitve problemov, snovanje izvedb, šum ultra mali, predojačenje signala

Izvleček: Polprevodniške detektorje sevanja uporabljamo na mnogih področjih raziskovanja v fiziki, od spektrometrije in slikanja z žarki X in γ do sledenja delcev pri eksperimentih v visokoenergijski fiziki. Čitalna elektronika mora ustrezati zahtevam, ki jih postavljajo različne uporabe detektorjev, kot so nizek šum za dosego visoke pozicijske in energijske ločljivosti, visoka hitrost, odpornost proti sevanju in delovanje pri nizkih temperaturah. Močno segmentirani detektorji so vzpodbudili razvoj monolitnih čitalnih vezij, medtem ko je bilo potrebno razviti prav posebne integracijske tehnologije za dosego optimalnega delovanja. Po predstavitvi osnov načrtovanja čitalne elektronike, v prispevku opisujemo rešitve, ki smo jih uporabili v posebnih primerih, kot so ultra nizkošumno predojačevanje za spektrometrijo z žarki X in γ ter analogno obdelavo signalov iz silicijevih mikropasovnih detektorjev. Vezja, ki jih opisujemo, segajo od nabojno občutljivih predojačevalnikov, izvedenih z JFET monolitnimi tranzistorji, kjer s posebno tehniko povratne vezave brez uporov dosežemo minimalen šum, do večkanalnih CMOS analogno-digitalnih integriranih vezij, ki vsebujejo kompletno čitalno elektroniko za silicijeve detektorje sledi v spektromerih na trkalnikih visokih energij.

1. INTRODUCTION

Semiconductor detectors are widely used to obtain information about various properties (such as energy, momentum, time of occurrence, position) of nuclear particles and radiation, that produce ionisation in the detector material. A measure of the information appears as an electric charge, induced on a set of two electrodes, characterised by their capacitance. The detector is connected to front-end electronic circuits, which include an amplifying device (usually a charge-sensitive preamplifier) and a filter, performing a shaping of the signal in the time domain to optimise the measurement of a desired quantity such as signal amplitude as a measure of the energy loss of the particle. The problem of the measurement of the charge delivered by a capacitive source with the best possible accuracy compatible with noise intrinsically present in the amplifying system has been widely discussed in the literature /1, 2, 3, 4, 5/, also taking into account the constraints (power dissipation, event rate) set by the different applications. The main results will be reviewed here, to derive the basic criteria for the design of low-noise front-end electronics.

Figure 1 shows a schematic model of an analog channel processing the signal from a semiconductor detector. The detector itself is modelled as a current source delivering in a very short time a charge Q across its capacitance C_D. The detector signal is integrated by a charge-sensitive preamplifier (with a feedback capacitance C_F and an input capacitance C_i) and then shaped

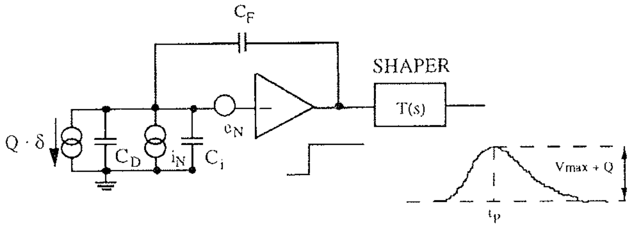

Fig. 1. Analog processing channel for the measurement of the charge Q delivered by a semiconductor detector.

by a filter with transfer function T(s). The filter allows the measurement of a quantity, for example signal peak amplitude, related to the charge released in the detector, minimising the error due to noise and to signal pileup due to a high event rate, which may set constraints on the signal duration and peaking time t_P.

The noise in the amplifier system arises from two uncorrelated sources at the input, a series voltage source e_N and a parallel voltage source i_N, each of which generates a spectral density with a white (independent of frequency f) and a non-white component:

$$\frac{\overline{de_N^2}}{df} = A_W + \frac{A_f}{f} \qquad (1)$$

$$\frac{\overline{di_N^2}}{df} = B_W + B_f \cdot f \qquad (2)$$

The white term in equation (1) is mostly determined by the white noise in the main current of the preamplifier input device, that is drain current for an FET or collector current for a bipolar transistor. g_m is the transconductance, while k is the Boltzmann's constant and T is the absolute temperature. Γ is a coefficient equal to 0.5 in bipolar transistors; it is about 2/3 for JFETs, and may exceed 1 for short-channel MOSFETs.

$$A_W = 4kT\frac{\Gamma}{g_m} \qquad (3)$$

The second term in the series noise is given by the 1/f noise in the drain or collector current. The white term in (2) is determined by the shot noise in the detector leakage current I_{det}, by the shot noise in the input device gate (base) current $I_{G(B)}$ and by the thermal noise in the preamplifier feedback resistor R:

$$B_W = 2qI_{det} + 2qI_{G(B)} + \frac{4kT}{R} \qquad (4)$$

where q is the electronic charge. The second term in (2) arises form dielectric losses in the components connected to the preamplifier input, and mainly depends on the detector - preamplifier assembly. It will be neglected in the following.

2. EFFECT OF NOISE ON CHARGE MEASUREMENTS FROM SEMICONDUCTOR DETECTORS

The effect of noise on the charge measurement is usually characterised by the standard deviation or Equivalent Noise Charge (ENC). This is the charge which injected at the input produces at the output of the linear processor a signal whose amplitude equals the root mean square noise. ENC is given by the quadrature sum of contributions from series and parallel noise terms described in the previous paragraph:

$$ENC = \sqrt{ENC_{A_W}^2 + ENC_{A_{1/f}}^2 + ENC_{B_W}^2} \qquad (5)$$

The contribution to ENC given by white series noise can be expressed in the following way:

$$ENC_{A_W} = \sqrt{\frac{A_1}{\tau}}\sqrt{4kT\frac{\Gamma}{f_T}}\sqrt{C_D}\left(m^{1/2} + m^{-1/2}\right) \qquad (6)$$

Several design criteria for achieving low-noise performances can be extracted from relationship (6). This term is directly proportional to the factor A_1/t, which is determined by the signal-shaping filter. τ is a parameter related to the time scale of the signal, and can be assumed to be the peaking time t_P. A long measurement time has to be used to minimise ENC_{AW}. The preamplifier input device has to feature a high transition frequency f_T, and to be capacitively matched to the detector. Equation (6) has a minimum at m=1, where $m=C_D/C_i$ is the capacitive matching coefficient. A low capacitance detector is also needed if very low noise performances must be achieved. The two latter conditions are also valid for the 1/f series noise contribution to ENC:

$$ENC_{A_{1/f}} = \sqrt{A_2}\sqrt{H_f}\sqrt{C_D}\left(m^{1/2} + m^{-1/2}\right) \qquad (7)$$

where A_2 is a coefficient depending on the filter. No dependence on t_P is present in this term, so its minimisation is essential both at short and long measurement times. The parameter $H_f = A_F C_i$ is a constant for a given technology and device gate length /6/. The need of reducing the effect of 1/f noise may determine the choice of the input device, reminding that typical values are $H_f = 10^{-27}$ J for silicon JFETs, $H_f = 10^{-25}$ J for P-channel MOSFETs and $H_f = 10^{-23}$ J for N-channel MOSFETs.

The parallel noise contribution to ENC is:

$$ENC_{B_W} = \sqrt{A_3\tau}\sqrt{2qI_D + 2qI_{G(B)} + \frac{4kT}{R}} \qquad (8)$$

It is proportional to $\sqrt{A_3\tau}$, which is determined by the filter: therefore it has a larger influence at long peaking times. Its minimisation requires a small detector leakage current I_D, which may limit the maximum active area of the detector, and may also force to operate it at low temperature. As it appears from (8), because of their base current I_B, standard bipolar transistors do not permit high resolution spectroscopy, instead allowed by FETs with a small gate current I_G, which can also be reduced by cooling. A main source limiting the achievable signal-to-noise ratio is the preamplifier feedback resistor. Several non resistive techniques have been developed to discharge the feedback capacitor, allowing to approach the ultimate resolution limits /7, 8, 9, 10, 11/.

The previous discussion shows that the energy resolution of the detection system is given, as far as electronic noise is concerned, by the detector itself, by the preamplifier input device and by the signal processor setting the values of the coefficients A_1, A_2, A_3 and of the signal peaking time t_P. It was shown that several measures can be taken to minimise the noise. If allowed by the counting rate, operation at the optimum t_P (usually several μs), determined by both series and parallel noise, is mandatory. In high rate applications adequate resolution can be achieved by operating with a low capacitance detector-FET system.

The following section describes a charge-sensitive preamplifier, where technology and design parameters are optimised to the achievement of very low noise in view of applications in high resolution spectroscopy. Section 4 presents a multichannel integrated circuit for the readout of silicon microstrip detectors in an accelerator experiment: here the design choices had to cope with severe constraints set by detector geometry and operating environment.

3. MONOLITHIC JFET PREAMPLIFIER FOR HIGH RESOLUTION SPECTROMETRY

The Junction Field-Effect Transistor (JFET) is considered to be the best choice in X and g-ray spectrometry applications for several reasons /12, 13, 14/. Among the FET devices, it has the smallest amount of low frequency noise and its white noise has a reliable dependence on the transconductance. It has intrinsic properties of radiation hardness, and it can operate at cryogenic temperatures, with a considerable reduction of the leakage current and of the series noise.

It is worth pointing out here that very good results were recently obtained also with CMOS devices, especially in applications requiring relatively short peaking times, such as room temperature operated detectors having non negligible leakage currents or low-capacitance detectors /15, 16, 17, 18/.

The excellent characteristics of the JFET suggested the development of the monolithic buried layer process, where N-channel JFETs of outstanding noise performances are integrated on the same substrate. This process provided the basis for the realisation of several preamplifiers /19, 20, 21, 22/. One of them (IPA4) /23/ was conceived for γ-ray spectrometry in association with large germanium detectors. For this purposes the front-end device was designed with $W = 1820\,\mu m$ and $L = 5\,\mu m$, yielding an input capacitance of about 10 pF.

This circuit achieves the best noise performances /24/ when operated with a non resistive, continuous-type charge reset based on the forward-biased JFET principle /7/, as shown by the schematic in figure 2.

The preamplifier consists of an input cascode (J_1, J_2), a bootstrapped active load (J_3, J_4, J_7) and a source follower output stage (J_8), with an integrating feedback capacitance C_F. The detector leakage current and the signal charge from the feedback capacitor are fed to the gate of the input transistor. These currents add to the reverse current of the gate-to-drain junction and force the gate-to-channel junction to be forward-biased. A low frequency feedback loop is employed to stabilise the operating point of the preamplifier in presence of the forward-biased gate-to-source junction. It goes from the central point of the R_1, R_2 divider to the gate of J_2. The current needed to operate the input JFET with a forward-biased gate is provided by the resistor R_{BL}.

The benefit brought about by the non-resistive charge reset becomes apparent from the comparison of curves a) and b) in fig. 3, both obtained with the preamplifier

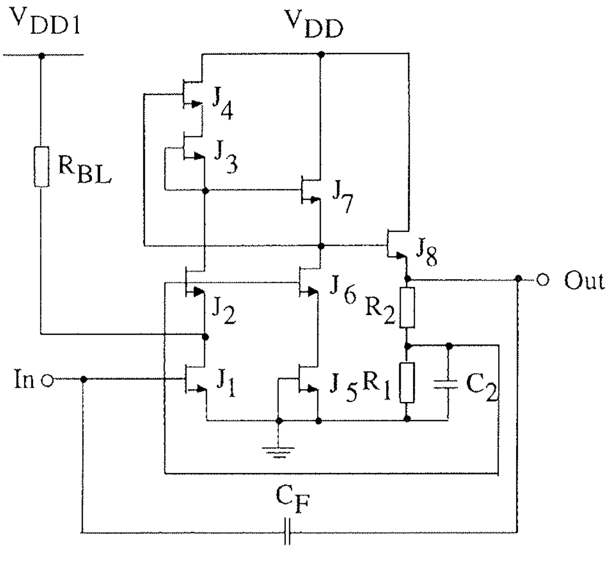

Fig. 2. IPA4 preamplifier with forward biased gate-to-source junction in the front-end device.

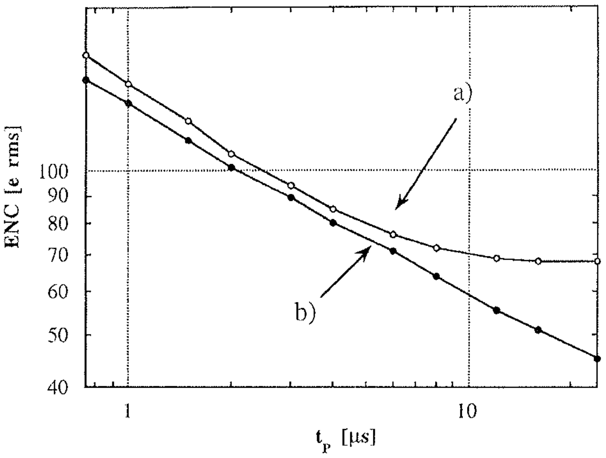

Fig. 3. Equivalent noise charge as a function of the peaking time tp, at zero detector capacitance, for the buried layer IPA4 charge-sensitive preamplifier. (a) Preamplifier with resistive feedback. (b) Preamplifier with non-resistive charge reset.

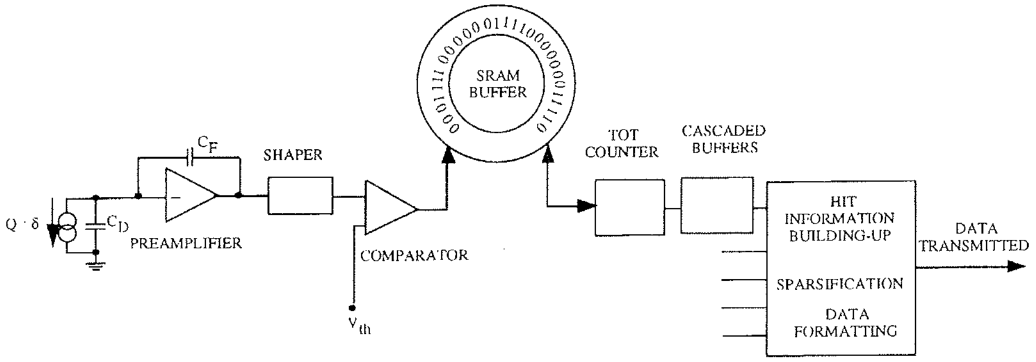

Fig. 4. Block diagram of the front-end chip intended for signal processing in BaBar vertex detector.

followed by a unipolar semigaussian shaper. In order to enhance the relative importance of the ENC contribution coming from parallel sources, among them dielectric noise, from that due to series sources, the measurements were done with no external detector simulating capacitance. Curve a) in fig. 3, relevant to the preamplifier with resistive feedback, shows that ENC tends to level off to about 70 e rms at peaking times t_P beyond 10 μs and even shows a gentle rising trend at 24 μs. The ENC behaviour at long peaking times results from the combined effects of dielectric and thermal noise associated with the feedback resistor. In the case of the preamplifier with non-resistive feedback, where these effects are eliminated, ENC keeps decreasing as t_P is increased and reaches 45 e rms at the longest explored peaking time. This value is certainly very good for a preamplifier which employs at the input a device with a 10 pF input capacitance. These considerations bring favour to the buried-layer process as a very suitable basis for the realisation of monolithic preamplifiers with noise characteristics adequate to high resolution spectrometry.

4. A CMOS MULTICHANNEL READOUT INTEGRATED CIRCUIT FOR A SILICON VERTEX TRACKER

Very high granularity semiconductor position-sensitive detectors such as silicon microstrip or pixel detectors are used in applications ranging from tracking in elementary particle physics experiments to medical imaging. The readout of these detectors has to be carried out by high density multichannel mixed-signal ASICs, combining analog processing functions and high speed digital circuits. Low-power design techniques are used, and the choice of the technology is restricted to CMOS or BiCMOS processes. The latter are usually preferred in very high rate applications, where signal shaping times are of the order of a few tens of ns, because of the high values of the parameters g_m/I_C, g_m/C_i featured by bipolar transistors used as input devices /25, 26, 27, 28, 29/. In lowerrate applications ($t_p \geq 100$ ns) and with low capacitance detectors (C_D $\leq$1 pF) purely CMOS Ics are commonly used /examples are given in references 30, 31, 32, 33/. In many applications radiation hardness is also a very important issue, especially in experiments at high luminosity colliders, where the front-end electronics has to stand high doses of ionising radiation and neutron fluences without performance degradation.

One of the readout ICs most recently developed is a low-noise, mixed-signal CMOS chip containing the complete readout electronics for the Silicon Vertex Tracker based on double-sided microstrip detectors in the BaBar experiment at SLAC. The chip has 128 channels that process in parallel the signals coming from an equal number of strips. The strip signals are amplified, shaped and then digitised using a range compression method, based on the Time-over-Threshold technique /34/. To do this, the signal at the shaper output is presented to a comparator with a preset threshold. The duration of the signal at the comparator output is the Time-over-Threshold (ToT), that is the time during which the shaper output signal exceeds the threshold.

The block diagram of the BaBar SVT front-end chip is shown in figure 4. The charge information carried by the ToT value is stored into trigger latency buffers, one for each channel, to compensate for delay and jitter in the time of arrival of the first-level trigger. Upon receipt of a trigger, the data are retrieved from the latency buffers, and after passing through two cascaded derandomizing buffers they end up in a sparsifying unit, where the final hit information is built up, providing, for each channel which has recorded a signal, the channel number, the hit time stamp and the value of the charge. This information is transmitted by the chip in serial format upon receipt of a readout command. The previous functional description gives an oversimplified view of the actual readout chip, named AToM (A Time-over-threshold Machine). Many more functions are implemented as described in a detailed way in references /35, 36, 37/. Among them, the possibility of selecting the value of the charge sensitivity of the analog channel (LOW = 150 mV/fC, HIGH = 250 mV/fC) and of the signal peaking time t_P (from 100 ns to 400 ns), and of operating on both detector signal polarities (n-side and p-side).

During the operational lifetime of the detector, the chip will be exposed to considerable levels of ionising radiation. A worst-case estimate of the ionising dose in the inner layers of the detector is 2 Mrad (Si). To achieve the required degree of radiation tolerance, the chip was fabricated in a rad-hard technology (Honeywell RICMOS IV bulk CMOS, 0.8 μm minimum gate length).

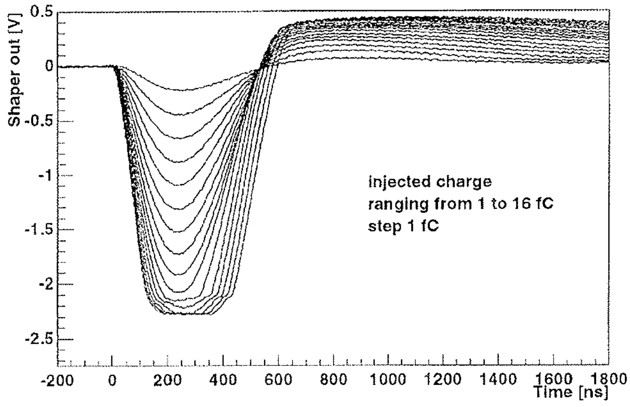

Fig. 5. Waveforms at the shaper output at 200 ns peaking time for the AToM chip.

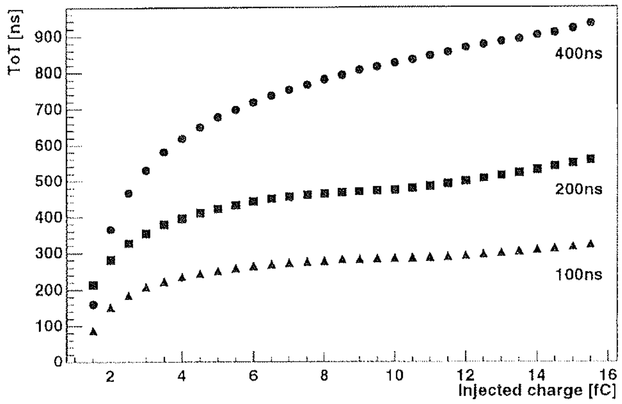

Fig. 6. ToT at the comparator output at three different peaking settings for the AToM chip.

Figure 5 shows the signals at the shaper output at the 200 ns peaking time setting with the input charge as a parameter. Three ToT curves at three different peaking times are shown in figure 6. The range-compression features obtained with the ToT technique are evident. Noise measurements at 200 ns peaking time and 3.5 mW total power dissipation per channel yield an ENC of 700 electrons rms at 12 pF detector capacitance.

5. CONCLUSIONS

This paper presented a review of the design criteria of front-end electronics for semiconductor radiation detectors, especially targeting low-noise specifications. As an example of available front-end circuits, two designs for very different applications were described. As a conclusion, it is worth pointing out that research in this field is stimulated by the severe requirements of future physics experiments and extending medical and industrial applications of semiconductor detectors. To this purpose, attention is focused on the technological developments in the fields of III-V devices, such as MESFETs or HEMTs /38/, of short-channel ("deep submicron") MOSFETs /39/ and of electronics for cryogenic temperature operation /40/.

6. ACKNOWLEDGEMENTS

The front-end circuits presented in this paper were designed and characterised by the Electronic Instrumentation group at the Department of Electronics of the University of Pavia, under the supervision of Pier Francesco Manfredi and Valeria Speziali.

7. REFERENCES

/1/ E. Gatti, P.F. Manfredi, "Processing the signals from solid-state detectors in elementary particle physics", La Rivista del Nuovo Cimento, Vol. 9, 3 (1986), p. 140.

/2/ V. Radeka, "Low-noise techniques in detectors", Ann. Rev. Nucl. Part. Sci. 1988. 38: 217-77.

/3/ P.F. Manfredi, V. Speziali, "Noise limits in detector charge measurements", Techniques and Concepts of High Energy Physics VI. Plenum Press, New York (1991), 381.

/4/ A. Pullia, G. Bertuccio: "Resolution limits of silicon detectors and electronics for soft X-ray spectroscopy at non cryogenic temperatures", Nucl. Instr. and Meth. in Phys. Res. A380 (1996), 1.

/5/ G. Bertuccio, A. Pullia, G. De Geronimo: "Criteria of choice of the front-end transistor for low-noise preamplification of detector signals at sub-microsecond shaping times for X- and γ-ray spectroscopy", Nucl. Instr. and Meth. in Phys. Res. A380 (1996), 301.

/6/ G. Lutz, P.F. Manfredi, V. Re, V. Speziali: "Limitations in the Accuracy of Detector Charge Measurements set by the 1/f Noise in the Front-end Amplifiers". Nucl. Instr. and Meth. in Phys. Res., A277 (1989), 194.

/7/ G. Bertuccio, P. Rehak, D. Xi, "A novel charge sensitive preamplifier without feedback resistor". Nucl. Instrum. and Meth. in Phys. Res. A 326 (1993), 71.

/8/ G. Bertuccio et al.: "Silicon drift detector integrated P-JFET for continuous discharge of collected electrons through the gate junction". Nucl. Instrum. and Meth. in Phys. Res. A377 (1996), 352.

/9/ F.S. Goulding, J. Walton, D.F. Malone, "An opto-electronic feedback preamplifier for high-resolution nuclear spectroscopy", Nucl. Instr. and Meth. in Phys. Res., 71 (1969), 273.

/10/ T. Nashashibi, G. White, "A low-noise FET with integrated charge restoration for radiation detectors", IEEE Trans. Nucl. Sci., Vol. 37, No. 2 (1990), 452.

/11/ D.A. Landis, F.S. Goulding, R.H. Pehl, J.T. Walton, "A low-noise FET with integrated charge restoration for radiation detectors", IEEE Trans. Nucl. Sci., Vol. 18, No. 1 (1971), 115.

/12/ P.F. Manfredi, V. Speziali, "Silicon junction field-effect transistors in low noise circuits: research in progress and perspectives", Techniques and Concepts of High Energy Physics VI. Plenum Press, New York, (1991), 423.

/13/ G. Cesura, V. Re, A. Tomasini: "Radiation Sensitivity of Noise in Monolithic JFET circuits exposed to 60Co γ-rays", Nucl. Phys. B (Proc. Suppl.), 32, 546 (1993).

/14/ G. Cesura, V. Re, "Effects of γ-rays and Neutrons on the Noise Behaviour of Monolithic JFET Circuits", IEEE Trans. Nucl. Sci., Vol. 41, No. 3 (1994), p. 577.

/15/ P. O'Connor, G. Gramegna, P. Rehak, F. Corsi, C. Marzocca, "Ultra low noise CMOS preamplifier-shaper for X-ray spectroscopy", Nucl. Instr. and Meth. in Phys. Res., A409 (1998), 315.

/16/ B. Ludewigt, J. Jaklevic, I. Kipnis, C. Rossington, H. Spieler, "A high rate, low noise, X-ray silicon strip detector system", IEEE Trans. Nucl. Sci., Vol. 41, No. 4 (1994), 1037.

/17/ R. Turchetta et al, "High spatial resolution silicon read-out system for single photon X-ray detection", IEEE Trans. Nucl. Sci., Vol. 41, No. 4 (1994), 1063.

/18/ M.L. Prydderich, P. Seller, "A 16 channel analogue sparse readout I.C. for INTEGRAL (International Gamma-Ray Astrophysics Laboratory)", IEEE Trans. Nucl. Sci., Vol. 42, No. 4 (1994), 776.

/19/ M. Demicheli, P.F. Manfredi, S. Rescia, V. Radeka, V. Speziali, "Design of monolithic preamplifiers employing diffused N-JFETs for ionization chamber Calorimeters", Nucl. Instrum. and Meth. in Phys. Res. A289 (1990), 418.

/20/ V. Radeka, S. Rescia, L.A. Rehn, P.F. Manfredi, V. Speziali, "Monolithic Junction Field-Effect Transistor Charge Preamplifier for Calorimetry at High Luminosity Hadron Colliders", IEEE Trans. Nucl. Sci., NS-40 (1993), 1321.

/21/ V. Radeka, S. Rescia, P.F. Manfredi, V. Speziali, F. Svelto, "JFET Monolithic Preamplifier with Outstanding Noise Behaviour and Radiation Hardness Characteristics", IEEE Trans. Nucl. Sci. NS-40 (1993), 744.

/22/ F. Lanni, P.F. Manfredi, V. Radeka, S. Rescia,V. Re, V. Speziali, "Monolithic silicon JFET front-end for calorimetry". Nucl. Instrum. and Meth. A 360 (1995), 158.

/23/ P.F. Manfredi, V. Re, V. Speziali, "JFET-based monolithic preamplifiers for spectrometry applications", Nucl. Instrum. and Meth. A 380 (1996), 308.

/24/ P.F. Manfredi, V. Re, V. Speziali: "Monolithic JFET preamplifier with non-resistive charge reset", IEEE Trans. Nucl. Sci. Vol. 45, No. 4 (1998), p. 2257-2260.

/25/ I. Kipnis, H. Spieler, T. Collins, "A bipolar analog front-end integrated circuit for the SDC silicon tracker", IEEE Trans. Nucl. Sci., Vol. 41, No. 4 (1994), p. 1095.

/26/ E. Spencer et al, "A fast shaping low power amplifier - comparator integrated circuit for silicon strip detectors", IEEE Trans. Nucl. Sci., Vol. 42, No. 4 (1995), p. 796.

/27/ W. Dabrowski et al: "Low-noise monolithic bipolar front-end for silicon drift detectors", Nucl. Instr. and Meth. A 420 1-2 (1999), 270.

/28/ F. Anghinolfi et al, "SCTA - A rad-hard BiCMOS analogue readout ASIC for the ATLAS semiconductor tracker", IEEE Trans. Nucl. Sci., Vol. 44, No. 3 (1997), 298.

/29/ W. Dabrowski, J. Kaplon, R. Szczygiel, "SCT128B - A prototype chip for binary readout of silicon strip detectors", Nucl. Instrum. and Meth. A 421 1-2 (1999), 303.

/30/ T. Zimmermann et al, "SVX3: a deadtimeless readout chip for silicon strip detectors", ", Nucl. Instrum. and Meth. A 409 (1998), 369.

/31/ F. Anstotz at al, "Performance of a CMOS mixed analogue-digital circuit (APVD) for the silicon tracker of CMS", Proceedings 4th Workshop on Electronics for LHC experiments, Rome, September 21 - 25, 1998. CERN/LHCC/98-36.

/32/ L. Blanquart et al, "Pixel analog cell prototypes for ATLAS in DMILL technology", Nucl. Instrum. and Meth. A 395 (3) (1997), 313.

/33/ M. Campbell et al, "Development of a pixel readout chip compatible with large area coverage", Nucl. Instrum. and Meth. A 342 (1994), 52.

/34/ R. Becker et al, "Signal processing in the front-end electronics of BaBar vertex detector", Nucl. Instr. and Meth. in Phys. Res., A 377 (1996), p. 459-464.

/35/ I. Kipnis et al, "A Time-over-Threshold Machine: the Readout Integrated Circuit for the BaBar Silicon Vertex Tracker", IEEE Trans. Nucl. Sci., Vol. 44, No. 3 (1997), p. 289-297.

/36/ V. Re et al: "The rad-hard readout system for the BaBar silicon vertex tracker", Nucl. Instr. and Meth. in Phys. Res., A 409 (1998), p. 354-359.

/37/ P. F. Manfredi et al: "Functional characteristics and radiation tolerance of AToM, the front-end chip of BaBar Silicon Vertex Tracker", presented at 1998 IEEE Nuclear Science Symposium, Toronto, November 10-12, 1998, to be published on IEEE Trans. Nucl. Sci.

/38/ G. Bertuccio, G. De Geronimo, E. Gatti, A. Longoni, J. Ludwig, K. Runge, W. Webel, S. Lauxtermann, "About the use of HEMT in front-end electronics for radiation detection", Proc. 20th Internat. Symp. GaAs Related Compounds, Freiburg, Germany: IOP Publishing, Sept. 1993, p. 111.

/39/ A. Marchioro, "Deep submicron technologies for HEP", Proceedings 4th Workshop on Electronics for LHC experiments, Rome, September 21 - 25, 1998. CERN/LHCC/98-36.

/40/ Proceedings 3rd European Workshop On Low-Temperature Electronics 3, San Miniato, Tuscany, Italy, June 24-26, 1998. Journal de Physique IV, Vol. 8, Pr 3, June 1998.

Dr. Valerio Re
Dipartimento di Ingegneria, Università di Bergamo
Via Marconi, 5, 24044 Dalmine, Italy

Dr. Lodovico Ratti
Dipartimento di Elettronica, Università di Pavia
Via Ferrata, 1, 27100 Pavia, Italy

Prispelo (Arrived): 18.01.1998 Sprejeto (Accepted): 03.03.1999