CMOS PROCESSES AS BASIS FOR MICROSYSTEM TECHNOLOGY

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Abstract: CMOS ICs have become the dominant technology in the semiconductor industry and will continue to be the fastest growing segment. At IMEC we try, for our R&D work in the microsystems technology (MST) field, to built as much as possible on the know-how and infrastructure available at IMEC for the development of CMOS process steps, modules and fully integrated processes. Monolithic integration is pursued by industry for mass-produced transducers or for microsystems with large array of sensors or actuators. Today´s monolithic devices include visible and IR imagers, miniature displays, biochemical, pressure, flow and acceleration sensors. The application of technologies developed for CMOS are not limited to monolithic integration alone. They can also used to improve the performance of the more classical micromachining technologies. The present paper gives an overview of work in this field at IMEC.

CMOS procesi kot osnova tehnologijam za izdelavo mikrosistemov

Ključne besede: CMOS polprevodniki kovinskooksidni komplementarni, MST tehnologije mikrosistemske, IC vezja integrirana, proizvodnja množična, integracija monolitna, pretvorniki, senzorji, aktivatorji, upodabljalniki, zasloni miniaturni

Izvleček: CMOS je postala dominantna tehnologija v polprevodniški industriji in bo še nadalje predstavljala njen najhitreje rastoči del. V IMECu si prizadevamo naše raziskovalno delo na področju tehnologije mikrosistemov čim bolj osnovati na znanju in infrastrukturi, ki je že na razpolago. oz. nam jo nudijo že razviti procesni moduli in CMOS tehnologije. Monolitno integracijo danes industrija potiska v ospredje predvsem zaradi množične proizvodnje pretvornikov, oz. mikrosistemov z velikim deležem površine senzorjev in aktuatorjev. Današnja monolitna integrirana vezja vsebujejo IR detektorje slike, miniaturne prikazalnike, biokemične senzorje ter senzorje pritiska, pretoka in pospeška. Vendar uporaba tehnologij razvitih za CMOS vezja ni omejena samo na opisano. Lahko jih uporabimo tudi za izboljšanje delovanja bolj klasičnih mikromehanskih tehnologij. Namen tega prispevka je prikazati tovrstna prizadevanja in aktivnosti v IMECu.

1. Introduction

Sensors and actuators transform an input signal to an output signal. In case of a sensor, the input signal is e.g. optical, chemical, the output usually electrical. In most system applications, the transducer is complemented by dedicated electronic circuitry for output signal treatment. The interconnection between both is either done by hybrid mounting (flip-chip, wire bonding) or by monolithically integrating transducers and transistors on the same Si-substrate using a dedicated process flow. This is feasible because many transducers use similar process technology as microelectronics, namely planar thin film processing.

Monolithic integration has substituted the hybrid approach in some but not all cases. The hybrid approach will continue to co-exist because of its specific merits. Hybrid integration allows an independent optimisation of the technology and specifications for the electronic circuitry and the transducer. Further, the longer development cycle of monolithically integrated transducers, due to the lengthy and complicated process sequences (typically 15...20 mask levels), implies a longer time-to-market.

There are two typical situations where monolithic integration is generally preferred. If the transducer is used as a transducer matrix array, containing thousands up to millions of identical pixels, these pixel signals have to be multiplexed in order to reduce the number of output connections to a reasonable level. This massively parallel interconnection can not always be realised by flip-chip techniques, because of the technological limitations (pitch, yield, reliability, ...) that arise for large pixel numbers and densities. The other advantage of monolithic integration is towards mass-production. Silicon transducer markets vary in size from niche-applications where a few 10000´s of devices a year are made, up to mass-applications in the automotive or consumer sector where 10´s per millions/year are produced. For the largest markets, economics often dictate the monolithic solution because the reduced assembly and packaging costs outweighs the increased process cost.

At IMEC we focus on the development of fabrication technologies for microsystems. Since the background and main activity at IMEC is sub micron CMOS process development we try built for the work in MST as much as possible on the available infrastructure and know-how in that area. The CMOS know-how is complemented by expertise in other areas such as thin film multi-chip-module (MCM-D) technology, ferro-electric materials processing for non-volatile memory applica-

tions, III-V materials processing and the processing of organic materials for opto-electronic applications. As shown in figure 1 the MST activities are built upon broad and solid general thin film materials processing foundation. The work in the MST group focuses on the development of process flows avoiding as much as possible non-standard materials and equipment. Non-standard modules are developed taking into account the limitations imposed by the CMOS environment.

The advantages of such an approach are obvious: maximum usage of what has already been developed resulting in a reduction of the technological risk, development time and cost. From the start of the project the involvement of a commercial foundry is pursued, in order to facilitate the transfer of the process from IMEC to an industrial environment. Depending on the process flow part of the processing can be done in a standard CMOS foundry, part in a MST foundry environment. Industrial project partners usually provide the application know-how and device concepts. Typically this results in trilateral relationship with a user initiating the device concept, IMEC developing the process flow and specific non-standard process modules and a foundry for the later mass production.

This relationship is schematically represented in figure 2 indicating the information flow between the partners.

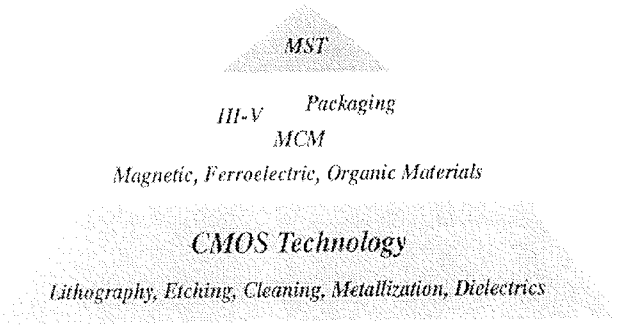

Fig. 1: IMEC MST process development approach

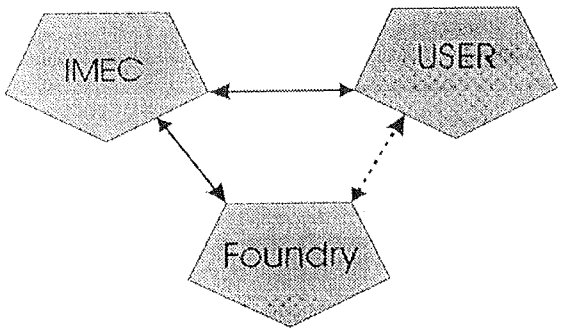

Fig. 2: MST process development partnership

2. Integrated processing

As shown in figure 3 adding transducer specific process steps and modules can be done in 3 different ways: as pre-processing, as a modified-back-end process or as post-metal processing. The first approach is not widespread because it requires that a foundry accepts pre-processed wafers, When the third route, post-metal processing, is followed, all transducer specific process modules are added after completion of the CMOS processing steps. The advantage of this route is that the CMOS part remains intact and therefore the influence of the added transducers on the behavior of the transistors is minimized.

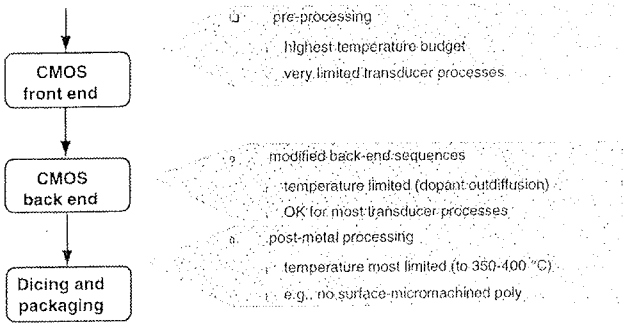

Fig. 3: addition of transducer-specific processes

The base wafers can be purchased from any standard CMOS fabrication facility, resulting in a large choice of available technologies. Also there is nearly no limitation on the kind of metal materials used to fabricate the transducers. However there is one main limitation on the kind of processing steps that can be added after full CMOS completion: the allowable thermal budget. Process temperatures above 400°C are not allowed, limiting e.g. depositions to mainly PECVD. This excludes e.g. poly-Si surface micromachining technology, LPCVD nitride as an ISFET-gate, wafer fusion bonding. In the second option, some or all of the transducer specific process modules are placed in between the CMOS process modules. When this route is followed, the possible impact of the added process steps on the CMOS behavior and on manufacturing issues has to be fully investigated. These main issues are related to additional thermal budget, additional layers which are deposited or grown, regions where additional etches are done and the addition of metal layers not commonly used in semiconductor fabrication which can cause contamination problems.

The impact of additional thermal steps depends on the position of the step in the process flow. Additional thermal budget will result in a change in the concentration profile under the transistor gate due to additional diffusion, especially for temperatures higher or equal to 900°C, leading to V_t-shifts. Having these temperature steps after junction implantation will also result in a further diffusion of the junction profiles, resulting in reduced channel lengths. If these effects occur, compensation is required by changing the implantation conditions, reduction of already existing temperature steps or additional mask biases.

The addition of layers above transistor areas also has its impacts. When a nitride layer is placed on top of a transistor, this layer will block hydrogen diffusion during

the final sintering step in the process. The effects of the added layers on hot carrier degradation can also be very important. In many applications, openings have to be made in the oxide layers on top of the silicon to clear the silicon or another layer (e.g. nitride). In the pre-metal and the intermetal dielectrics, different kinds of oxide layers have to be etched: undoped and doped LPCVD oxides, doped and undoped PECVD oxides, SOG layers, PECVD nitrides. This means that etching has to be controlled in these different layers in terms of profile, etch rate and selectivity. Combination of dry and wet etch is often the best solution because the dry etch gives the required profile control and the wet etch the required selectivity. To be able to control these etches higher densification temperatures of the oxides are required, especially in more advanced sub-micron technologies.

The monolithic integration of transducers further often requires the introduction of materials not standard used in semiconductor fabrication like Pt, Ag, PZT... Before these materials are introduced, careful contamination studies are required and additional working procedures need to be installed.

3. Examples

We can distinguish distinct application groups: those dealing with images, with physical signals, and with biochemical signals. Transducers dealing with images by nature, have to deal with 2-dimensional optical information which is captured, displayed, reproduced etc. This requires 1-dimensional or linear arrays (which are mechanically scanned in the second dimension) or 2-dimensional matrix arrays (which are static). The large majority of the 2D-arrays, and some of the 1D-arrays, are made monolithically to solve the interconnect problem. Physical sensors (primarily pressure sensors and accelerometers) for the automotive market, are produced in both monolithic /1/ and hybrid versions. Integrated biochemical sensor arrays are the most novel application group. Within the limited scope of this paper, we will not give an exhaustive review of all applications, but highlight selected work in the imaging and biochemical field.

3.1 Imaging transducer arrays

Recent improvements in CMOS imagers have allowed CMOS-based imagers to reach an image quality comparable to CCD´s /2/. CMOS imagers are made using fully standard process sequences. Additional process steps can enlarge their functionality. One example is full color imagers, on which a red-, blue- and green-died pattern is applied. The pattern formation can be done using commercially available died resists and standard i-line or g-line exposure systems. Another example is resist-based microlenses, which increase the fill-factor.

For infrared imagers, a recent innovation has been the introduction of Si-based uncooled infrared imagers. Infrared radiation can be captured by photon sensors (e.g. diodes with a small barrier height converting infrared photons to excited electrons) or by phonon sensors. Photon sensors can be made very sensitive but cryogenic operation is required in order to suppress the dark currents. Phonon sensors (converting infrared photons to phonons and thus heat) have demonstrated room temperature performance comparable to cooled detectors /3, 4/. A bolometer consists of a temperature dependent resistor and an IR absorber. The bolometer has a thermal capacity, and it is connected to an infinite heat sink at constant temperature through supports having a thermal conductance G. The absorbed IR radiation increases the temperature of the bolometer. In order to maximize the temperature increase, the bolometer must be thermally insulated (low G). The use of surface micromachining techniques allowed reducing the thermal conductance of the device to values close to the radiation limit. A SEM picture of an IR bolometer is displayed in figure 4. The structure is separated from the substrate by a vacuum gap, which is realized by surface micromachining using a sacrificial oxide. The only remaining thermal path to the substrate is through the supports.

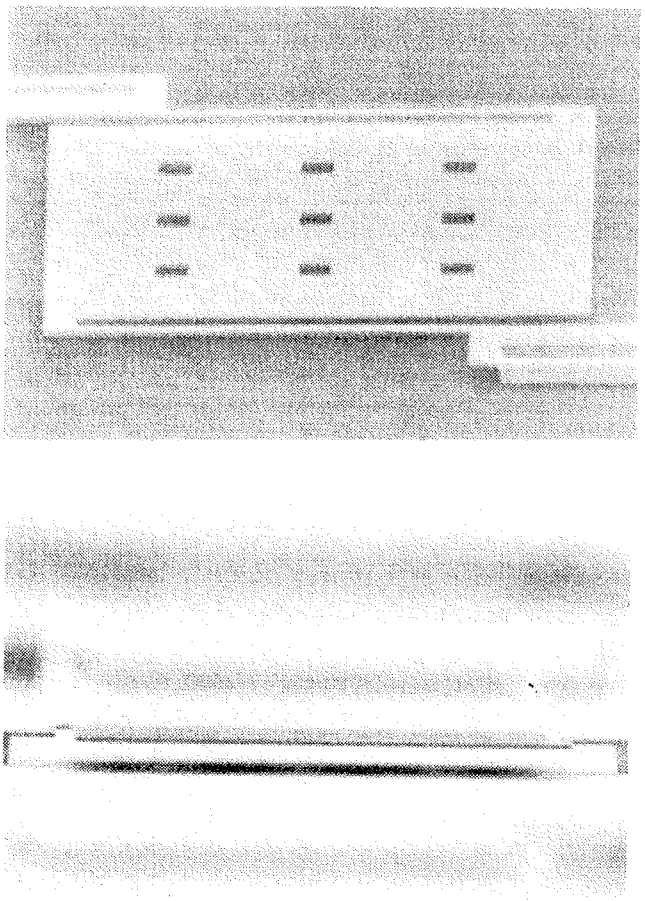

Fig. 4: SEM picture of 50µm x 50µm poly SiGe bolometer, supports are 400 nm thick and 1.5 µm wide.

The resistor element used is poly SiGe because of its advantageous properties as compared to poly-Si. Its stress can be tuned to the desired value at low temperature (figure. 5), which is not possible for poly-Si. It can be easily integrated with the driving electronics without running out of the thermal budget or damaging the existing electronics. Another attractive feature of using poly SiGe is its lower thermal conductivity, which en-

ables reducing the thermal conductance of the device to $7x10^{-8}$ W/K (which is only a factor of three higher than the radiation limit). Integrating poly SiGe bolometers into Focal Plane Arrays (FPA) yields an NETD of 65mK for an array of 320x240, comparable to the state of art /5/.In a thermopile, the increase in heat is detected by a Seebeck element. A poly-Si-to-Al Seebeck element can be made in a standard CMOS process flow, using the gate-poly and Al-metallisation. Also here, the use of poly-SiGe results in increased performance /6/. Bulk micromachined linear imagers with integrated signal processing capability have been demonstrated /7/. As compared to bolometers, the pixel size of thermopiles cannot be miniaturized to the same extent without sacrificing the NETD. For larger densities where small pixels are required, the bolometer principle is hence preferred.Si-based transducers are also used in image displaying. One approach is the Digital Micromirror Device (DMD), in which the change in tilt of tiny micromachined mirrors is used to modulate a light beam /8/. The other approach is using LCD´s as light modulators in transmissive or reflective displays.

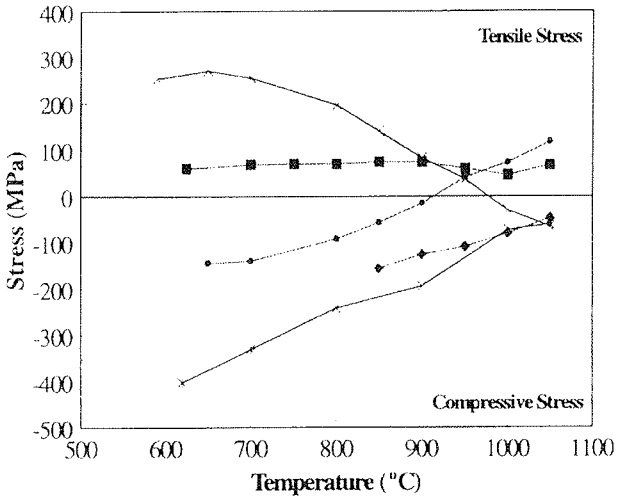

Fig. 5: Dependence of stress on annealing temperature (•APCVD poly SiGe grown at 650°C, ■RPCVD poly SiGe grown at 625°C, ◆APCVD poly Si grown at 850°C, ✳ LPCVD poly Si grown at 620°C and X LPCVD poly Si grown at 590°C).

Transmissive LCD displays are based on a-Si or poly-Si transistors, which are deposited on a quartz or glass substrate. Figure 6 shows a part of a transmissive display made in CMOS technology. Since the display need to be transparent, the only CMOS technology which could be used is a SOI technology from which the bulk of the silicon wafer is removed, using the buried oxide as an etch stop layer. A 1μm SOI technology was used. The active CMOS layer, less than 1μm thick was transferred to a transparent (glass) substrate. A parasitic effect of the display being transparent and illuminated by a light source, is the generation of photocurrents in every p-n junction. Using the SOI technology p-n junctions from source/drain to substrate are not present, but junctions from source/drain to channel are available. These photocurrents are parasitic currents compromising the operation of the logic. To suppress these currents a light shield over the CMOS areas is necessary.

In order to circumvent the transfer of technology and hence make use of an almost standard process, a CMOS-based reflective display is a very attractive approach /9/.

CMOS-based transducers are further encountered in image reproduction technology. Well-know developments are in inkjet technology. Micromachining is used in this case in order to create the miniature ink nozzles and containers /10/.

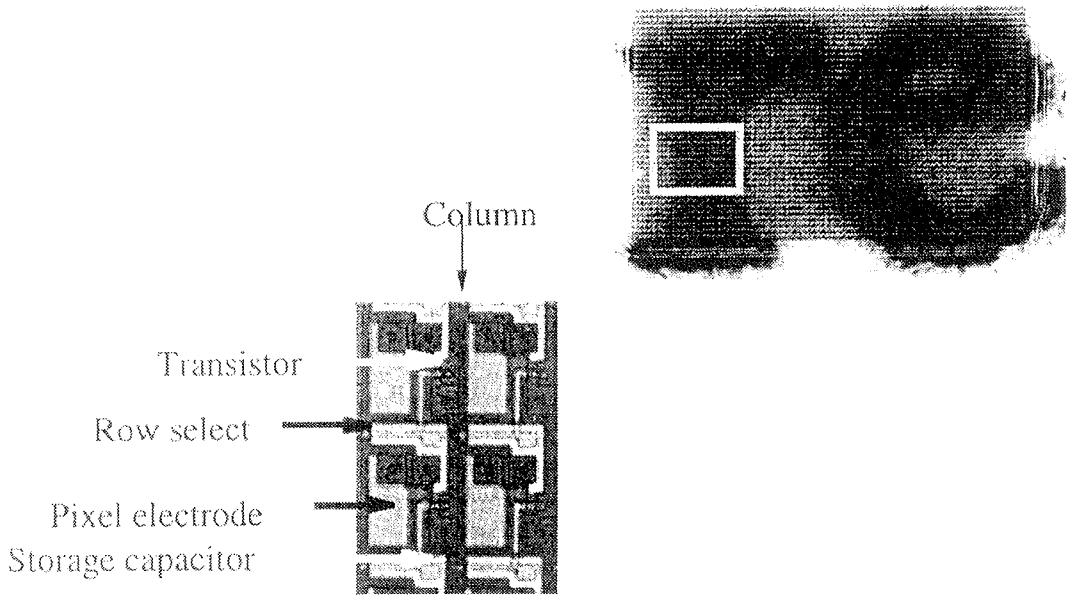

Fig. 6: Top left is shown a test array of the active plate for a LCD transmissive array. The inset right bottom shows a magnified view of 4 pixels.

3.2 Biochemical sensor arrays

The most recent area where integrated sensors are emerging, is biochemical sensor arrays. The characteristics of these devices are in several respects distinct. The sensor dimension is usually quite large (0.01 - 1 mm^2) due to the practical difficulties in handling sub-μL quantities of liquids. Also, the number of sensor sites is rarely higher than a few hundred. Lastly, the preference to use disposable devices makes the use of Si a possible but not exclusive choice. CMOS integration is hence not a mainstream for biochemical sensors, but nevertheless used in several devices.

An example is the Ion-Sensitive Field Effect Transistor (ISFET), which can be used as an ion sensor. The structure of an ISFET is similar to a MOSFET, the poly silicon gate is absent and the gate insulator is in contact with a sample liquid. Unlike the working principle of a MOSFET, the flatband voltage of an ISFET depends on the surface potential at the insulator-liquid interface. The surface of the gate insulator contains hydroxyl groups that can be protonated and deprotonated and thus an electrochemical relation between the electric field and the pH of the sample liquid exists. ISFETs can directly be integrated with MOSFETs in an opamp configuration /11/. Arrays of ISFETs were integrated with operational amplifiers in a standard 1.25μm CMOS technology (figure 7).

A sacrificial layer was used to protect the ISFET-gates during aggressive post-processing. Thin film Ag was deposited and patterned by a lift-off technique or by electroplating. Electrochemical Ag/AgCl reference electrodes are formed from it by electrochemical chloridation. The voltage of the sample liquid is kept constant by means of an immersed Ag/AgCl reference electrode. Pt electrodes were incorporated in the process flow to allow making also amperometric sensors. Thin and thick polymer micropools are structured by photo patterning and are used for electrolyte and membrane dispensing. Other ions (e.g. K^+, Ca^{2+}, and Na^+) can be measured by covering the device with an appropriate electrolyte layer and gas-permeable membrane.

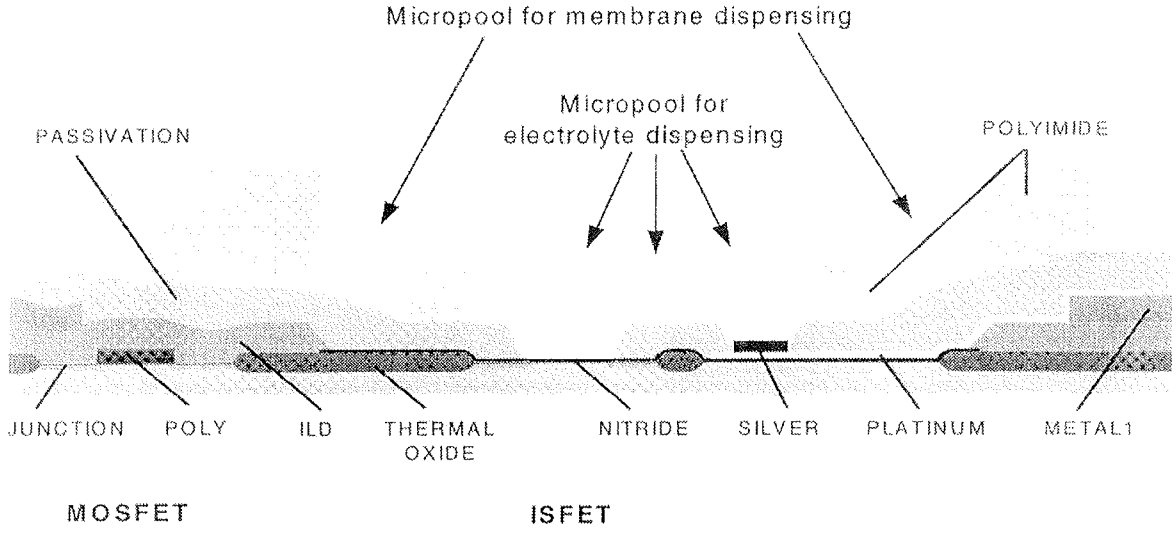

Fig. 7: Cross-section of an Ion-Sensitive Field Effect Transistor integrated in a 1.25μm CMOS technology

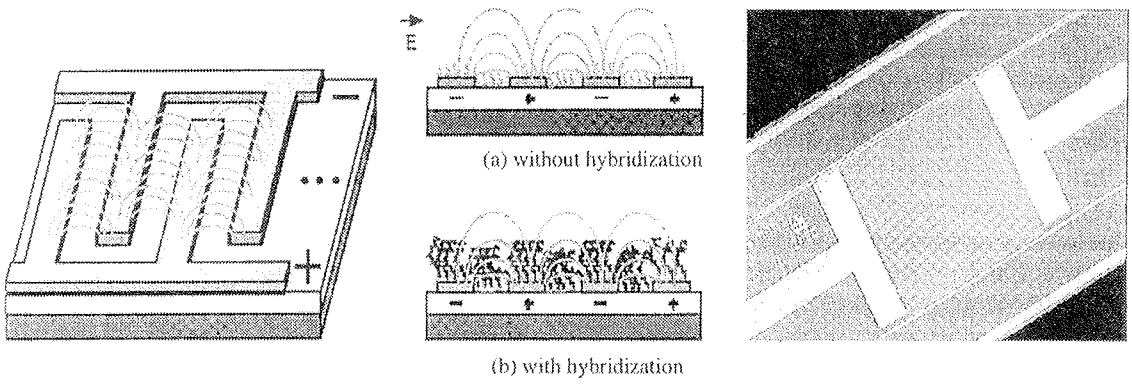

Fig. 8: Plan view (left) and cross-section (middle) of IDE sensor. The field lines are disturbed by hybridization at the surface. Photograph of IDE sensor (right)

All values for the nMOS parameters after the completion of the transducer specific processing are within the specifications and do not induce considerable shifts in the nMOS parameters. Using phosphate buffers between pH 6.0 and pH 8.0, the pH-sensitivity of a CMOS-processed ISFET-opamp module has been measured. The pH-sensitivity of the ISFET had a value of 53mV/pH.

Impedimetric sensors can also easily be integrated in CMOS. The basic structure is that of a planar interdigitated capacitor (figure 8). Nanoscaled interdigitated electrode arrays (IDEs) were made with Deep UV lithography. Electrode width and spacing from 500 nm down to 300 nm were achieved on large active areas (0.5mm x 1mm). 50 nm thick palladium electrodes or 40 nm thick gold electrodes were evaporated on 1.2 μm thermal SiO_2 and structured by lift-off. The interdigitated electrodes were between 300 nm and 500 nm wide, with spacings in the same order of magnitude. The response of the impedimetric sensors can be modeled electronically by an equivalent circuit consisting of an interface impedance, represented as a constant phase element, a solution resistance and a dielectric capacitance between the electrodes. Due to the distribution of the field-lines, information is detained about interface phenomena as well as about properties of the bulk in the vicinity of the electrodes. Genetic diseases and infectious agents can be traced by looking for specific DNA-sequences. The presence of these DNA-sequences or antigens/antibodies can be detected by looking for the binding of these molecules to selective probes. When target nucleic acid hybridizes to oligonucleotide probes or when antibodies bind to antigens, the change in electric properties, in the vicinity of an electrode, results in a change of impedance, enabling the measurement of a direct electrical signal.

In a series of experiments, the possibilities of impedimetric sensing of DNA hybridization with nanoscaled IDEs were explored. Thiol-linked oligo´s were coupled to gold IDEs by chemisorption. After coupling of the probes to the structures non-specific binding was avoided by blocking with cysteine. The solution resistance lowered by a relative decrease of approximately 38% and 18% respectively. After hybridization with PCR product the solution resistance lowers significantly by a relative decrease of approximately 50%. These results clearly demonstrate that the nanoscaled impedimetric sensors are capable of detecting DNA fragments. A similar technology can also be used for a different purpose in DNA sensing, e.g. when the electrodes are used not for sensing, but for controlling the hybridization /12/.

4. Conclusions

CMOS based sensors and actuators have found applications in a wide range of products. Well-developed markets are e.g. in automotive sensors; novel developments are in the area of uncooled IR imaging, reflective displays and recently biochemical sensor arrays. Most transducer-specific process steps such as micro machining can be incorporated in a CMOS flow. The post-metal processing approach is the most attractive, but will only reach its full potential if we can achieve lower temperature process for e.g. surface micro-machining, ISFET dielectrics, wafer fusion bonding. The research and development activities in the field of CMOS process development puts IMEC in an excellent position to contribute to the development of novel MST fabrication processes.

5. Acknowledgement

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