UDK621.3:(53+54+621+66), ISSN0352-9045

SILICON BULK MICROMACHINING FOR SENSOR TECHNOLOGIES

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TUTORIAL INVITED PAPER
MIDEM´99 CONFERENCE - Workshop on MICROSYSTEMS
13.10.99 - 15.10.99, Ljubljana, Slovenia

Keywords: sensors, sensor technology, MM, MicroMachining, Si technologies, silicon technologies, bulk machining, pressure sensors, flow sensors, microsensors, flow microsensors, gas sensors, hybrid technologies, microsystems

Abstract: Micromachining and related technologies are needed to develop a large variety of sensors and actuators, i.e. the basic components of Microsystems or MEMS (MicroElectroMechanical Systems) as they are also commonly called. Microsystems are designed and fabricated by integrating different microcomponents into one functional unit comprising of sensors, actuators, I.C.s for data processing etc. In this development a variety of micromachining technologies, ranging from the conventional silicon bulk and surface micromachining to LIGA and LASER techniques are employed, each one having specific merits for specific products /1/. This review focus on silicon bulk micromachining applied to the fabrication of sensors suitable for being integrated into Microsystems, which are under development at IRST Microsystem Division.

Mikroobdelava silicija v senzorskih tehnologijah

Ključne besede: senzorji, tehnologija senzorjev, MM obdelava najfinejša, Si tehnologije silicijeve, obdelava globinska, senzorji tlaka, senzorji pretoka, mikrosenzorji, mikrosenzorji pretoka, senzorji plina, tehnologije hibridne, mikrosistemi

Izvleček: Mikroobdelavo in podobne tehnologije potrebujemo za razvoj in izdelavo različnih senzorjev in aktuatorjev, ki tvorijo osnovne elemente tki. mikrosistemov, oz. kot jih pogosto kličemo MEMS (MicroElectroMechanicalSystems). Mikrosisteme načrtujemo in izdelujemo z integracijo različnih komponent v eni funkcijski enoti, ki se sestoji iz senzorjev, aktuatorjev, elektronike za obdelavo podatkov itn. Za izvedbo tega cilja uporabljamo različne tehnologije mikroobdelave silicija od konvencionalne površinske, oz. globinske do LIGA in laserskih tehnik, ki pa vsaka ima svoje prednosti za realizacijo določenih izdelkov. V tem pregledu predstavimo tehniko mikroobdelave silicija, ki jo uporabljamo za izdelavo senzorjev, primernih za integracijo v mikrosisteme, ki jih trenutno razvijamo na inštitutu IRST na oddelku za mikrosisteme.

1. Introduction

Micromachining and related technologies are needed to develop a large variety of sensors and actuators, i.e. the basic components of Microsystems or MEMS (MicroElectroMechanical Systems) as they are also commonly called. Microsystems are designed and fabricated by integrating different microcomponents into one functional unit comprising of sensors, actuators, I.C.s for data processing etc. In this development a variety of micromachining technologies, ranging from the conventional silicon bulk and surface micromachining to LIGA and LASER techniques are employed, each one having specific merits for specific products /1/. This review focus on silicon bulk micromachining applied to the fabrication of sensors suitable for being integrated into Microsystems, which are under development at IRST Microsystem Division.

2. Microsystem technologies for medium-small volume applications

Market studies (forecast) indicate that the world-wide Microsystem market is slated to reach about 3 billion Euros at the beginning of year 2000, while simultaneously enabling applications reaching a market value 5 to 10 times bigger. Undoubtedly these numbers are staggering and should make many companies eager to participate. But the large variance in market estimates is a warning that the market is still in its development phase, and that these forecast are based on assumptions that remain largely to be verified. The examples of the inkjet print head, of the manifold absolute pressure sensors and of the airbag crash accelerometers are routinely invoked to illustrate the market opportunities that Microsystem devices can enable. But the majority of these large volume applications are dominated by large Corporations. In this type of developments and large volume production the preferred technology is CMOS with a few post-processing steps to add the sensor layers. The monolithic approach represents the preferred solution especially when large matrix of sensors made of identical pixels, where massively parallel interconnections are needed, are to be fabricated in large volumes.

Small and Medium size Enterprises (SMEs) are also interested in microsystems and can survive by carving themselves small niche markets based on innovative products and technologies. In this case highly dedicated microsystems have to be produced in small-medium quantities. Due to cost and risk SMEs are forced to cooperate with Research Centres to reduce prototyping development cost and time to market. This creates a unique opportunities to link Research Centers and SMEs to join efforts in feasibility studies and prototypes design and development.

Dedicated microsystems aimed at niche markets represent a difficult task to be solved, both in terms of design, development technologies, market penetration and the ensuing financial profit. For this type of developments related to small volume production the hybrid approach is more suitable. Hybrid integration allows an independent optimisation of the different technologies required for the fabrication of the different types of sensors and actuators to be coupled with the IC driving electronics to form the microsystem. Furthermore, it takes advantage of an increasing number of basic components and subsystems made available on the market by specialised manufacturers. The idea is then that different suppliers will offer a catalogue of standardised micromodules, such as power supplies, sensors and sensors arrays, actuators, fluidic modules etc., and that the system producer concentrate in the development of only a few specific modules, if not available, and especially on the connecting of all these micromodules and related electronics, usually CMOS ASICs, to form the microsystem. In this strategy an increasingly important role is played by the optimum microsystem partitioning and by the packaging and interconnection(not only electrical!) technologies.

The microelectronics analogy of this foreseen approach is the gate array, which can be tailored to the desired performance by acting only on the metal interconnection level.

The hybrid solution based on standardised micromodules offers to SMEs the following main advantages:

- small investment to start a microsystem oriented activity;
- short development for prototyping and time to market;
- low cost manufacturing of small volumes,
- flexibility in designing new microsystems, and reuse of already established and optimised subunits.

All the above mentioned points are to be considered by SMEs in planning a successful exploitation of small volume production for microsystems aimed at niche markets

3.IRST approach to microsystems R&D

IRST intends to be an active partner in this emerging field. To this end during the few past years IRST-Microsystem Division has been active in developing silicon based micromachining technologies and sensor prototypes. Some of the most significant research and developments efforts and the results so far obtained are presented in this review.

Silicon micromachining represent a flexible technology suitable to address many different applications, yet mantaining a unique and fully manufacturable platform based on the mature know-how of the silicon VLSI processing.

Efforts aimed at adequate the IRST-Microsystem Division to successfully tackle and to take advantage of the sensors/microsystems emerging field resulted in a redefinition of the different technical tasks as follows.

a) IRST Microfabrication Facility

The Microfabrication Facility of IRST Microsystem Division is fully equipped to process small-medium volumes of standard CMOS and monolithic silicon integrated devices with a resolution of the order of 1 micron. To address sensor and microsystem developments a new automatic cassette to cassette double side proximity printing photolitography and micromachining dedicated wet-etch benches have been added to the silicon processing pilot line. Furthermore new technological steps mainly aimed at silicon surface and bulk micromachining have been developed and made available for internal prototyping and for external joint research and development projects. Among these new technologies, it seems worth mentioning the anisotropic etching in TMAH solutions, which has been optimised and is now routinely used in fabrication of the sensor micromachined prototypes.

b) TMAH anisotropic silicon etching

Tetra-methyl ammonium hydroxide, or TMAH, is an anisotropic silicon etchant that is gaining more and more attention in the fabrication process of mechanical microstructures and device isolation, as an alternative to the more conventional KOH and EDP etchants because of its high compatibility with conventional IC processes, due to the absence of metal ions in it. The possibility to passivate the aluminum metalization in properly saturated TMAH solution has also been demonstrated by doping the solution with appropriate amounts of silicon or silicic acid /2, 3/. This permits to etch devices with no protection of the aluminum metalization thus increasing the range of application of this etchant while simplifying both the post processing and the etch set-up configuration. As an example the micrograph shown in fig. 1 shows the results of an anisotropic TMAH etch performed on <100> silicon using only aluminum as the masking layer.

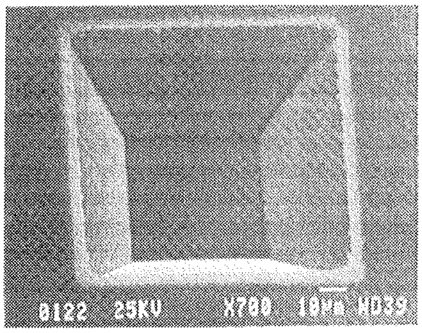


Fig. 1. Cavity produced by the dual-doped 5wt.% TMAH etch using an aluminum masking layer

c) Design and Modelling

Along with the fabrication of microdevices, another important area in the micromachined sensor development cycle is the use of micromechanical device simulators to be coupled with the more conventional TCAD tools for silicon device and processing simulation. Care is needed on how such tools can be combined to provide an overall design strategy for microdevice design and modelling and for the accurate simulation of all the fabrication cycle. The simulation activity in terms of electro-mechanical device characteristics is routinely carried out at IRST by using ANSYS and ISE-TCAD. In order to evaluate the results of some critical microfabrication process steps (pre-deposition, ion implantation, annealing) and the geometry of the etched 3D-structures, a process simulation with dedicated software tools (SILVACO and ACES) is also performed.

For the electro-mechanical simulation the software package ISE-TCAD is especially useful. This software is based on the finite element method and allows to obtain detailed stress and displacement maps on the membranes, cantilevers and on all the micromachined structures of interest. The simulation maps shown in this review are examples of the results mainly obtained by ISE-TCAD simulation.

d) Packaging and testing

The sensor prototypes developed at IRST-Microsystem Division are packaged and tested internally in order to have a feed-back on the device design and on the technological fabrication process. Once optimised, the device is tested to completely characterised its performance. Due to the large variety of different sensors under development, a number dedicated packaging techniques and of PC controlled characterisation benches, each one dedicated to a specific sensor typology, have been settled and are now routinely used. Modelling is usually needed for a detailed "in depth understanding" of the sensor behaviour. Such a phase involves also numerical simulation work on fluid dynamics and mechanics, with subsequent changes in the packaging solutions developed to meet the performance requirements. In addition, the packaging design has to be optimised to reduce cross-sensitivity between different measurands.

For small volume production the sensor packaging and mounting into an application specific microsystem is carried out externally by an IRST-spin off company, where the due attention to cost and reliability is given. The real challenge for sensor-microsystem manufacturer is to develop custom packaging technologies that meet all the necessary performance and reliability criteria, while keeping the cost of the microsystem assembly at a minimum. Additional requirements arise from the sensor interaction with the external environment to be tested. Hybrid packaging with dedicated IC or conventional electronics is routinely employed. The hybrid solution is usually preferred for niche markets, where a limited number of microsystems tuned to meet special requirements are to be delivered.

1. Examples of micromachined sensors under development at IRST Microsystem Division

a) pressure sensors

Piezoresistive silicon pressure sensors play an important role in many fields of applications, as automotive, process control and biomedical devices, due to their excellent performances, small size and low production cost /4,5/. The transduction of the pressure is accomplished by two pairs of piezoresistors which are placed close to the membrane edge in order to maximize the stress-induced effects (see fig. 2). The four piezoresistors are arranged in a Wheatstone bridge configuration (see fig. 3) where the resulting resistance change is easily converted in a voltage output.

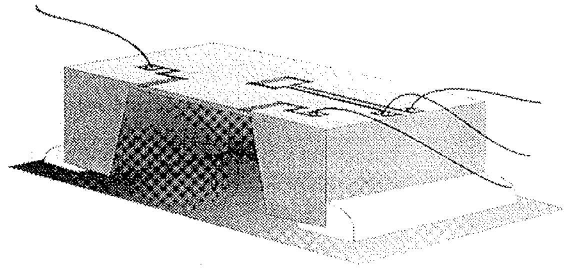


Fig.2. Device cross section.

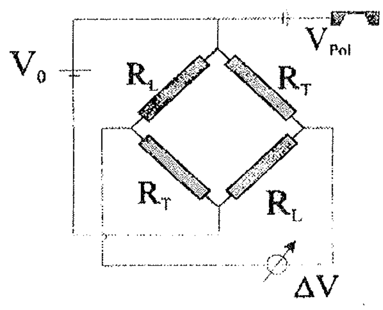


Fig. 3. Wheatstone bridge configuration

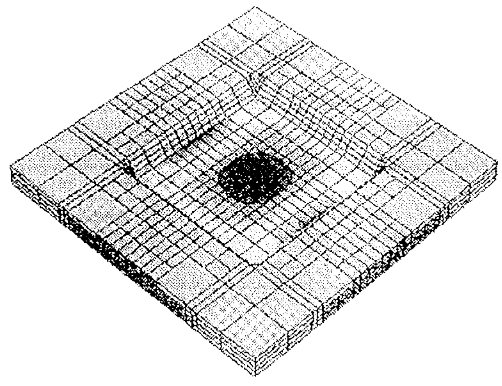


Fig. 4. Stress map simulated by ISE-TCAD. Highly stressed regions are dark. Backside view.

To achieve maximum sensitivity, the four piezoresistors should be centred on the membrane edge where the stress is maximum. 3D modelling of the stress and displacement on the membrane has been extensively used to optimise the piezoresistors layout. Example shown in fig. 4 refers to a silicon membrane area is 3200x3200μm^2 and the resistor dimensions are 100x500μm^2. The minimum distance between the resistors and the membrane edge is 100μm. Another important design parameter is the maximum load that can be applied to the membrane. This is related to the maximum stress induced in the structure and in turn to the maximum yield of silicon.

A 7-mask dedicated fabrication process, schematically illustrated in fig. 5, has been developed at IRST Microsystem Division for silicon micromachined pressure sensors prototyping and small volume production. The silicon wafers (n-type, 12 Ω·cm, 525 μm thick) are cleaned and a screen oxide (43 nm) is grown at 975°C in pure oxygen. Then a succession of three lithography and ion implantation steps is performed to dope the regions for n^+ contacts, p resistors and p^+ contacts (a). To electrically isolate the device a 700 nm thick LPCVD silicon oxide layer (TEOS) and a 100 nm thick LPCVD silicon nitride are deposited. At this point the contact holes are opened and a 600nm aluminium is sputtered and patterned (b). The frontside of the wafers is then covered by 800nm Low Temperature Oxide (LTO). Next the etching windows, defining the membrane size, are patterned and opened on the backside masking layers. A timed anisotropic etching forms the membranes of the desired thickness (c). Finally the wafers are diced, and the sensors chips are packaged (d) for testing.

No attempt has been carried out toward CMOS compatibility. The required electronics, tailored to specific applications, is available as a separate CMOS chip to be connected externally and mounted in the same sensor hybrid package.

b) flow microsensor

The flow microsensors, now under development, are based on well-known thermal anemometer principles, employing a central resistive heater, R_2, and two temperature sensing resistors, R_1 and R_3, placed on either side /6/. When there is no fluid flow, the heat produced by the central heater will be equally distributed to the symmetrically located temperature sensors. When a fluid flow exists, the symmetry of heat exchange will be modified resulting in an imbalance in temperature. This imbalance is used to determine the flow rate of the liquid.

The microheater fabrication process for flow sensor is schematically shown in fig. 6. The starting material is a 4 inch, 525μm thick, 16-24 Ω·cm, p-type, (100) oriented silicon wafer. A 300 nm TEOS oxide is first deposited by LPCVD, followed by thermal growth of 1150 nm SiO_2. Polysilicon (450 nm) is then deposited by LPCVD, doped with $POCl_3$ to yield a sheet resistance of 27 Ω/□, and subsequently patterned by photolithography to form the meander-type resistor heater. Upon 100 nm

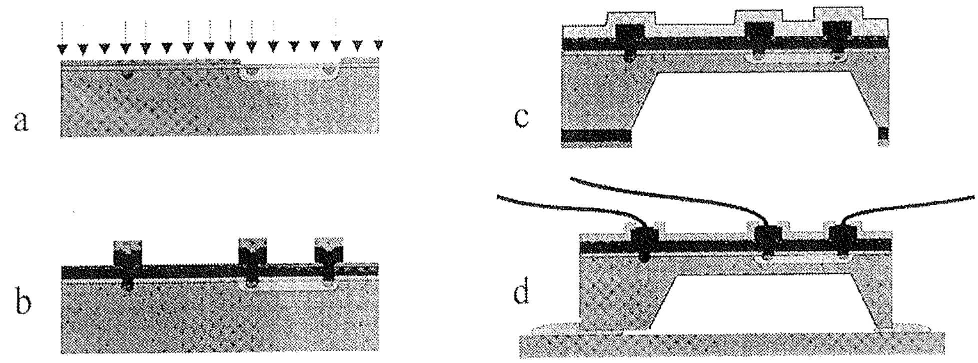


Fig. 5. Main process steps for the fabrication of a piezoresistive pressure microsensor.

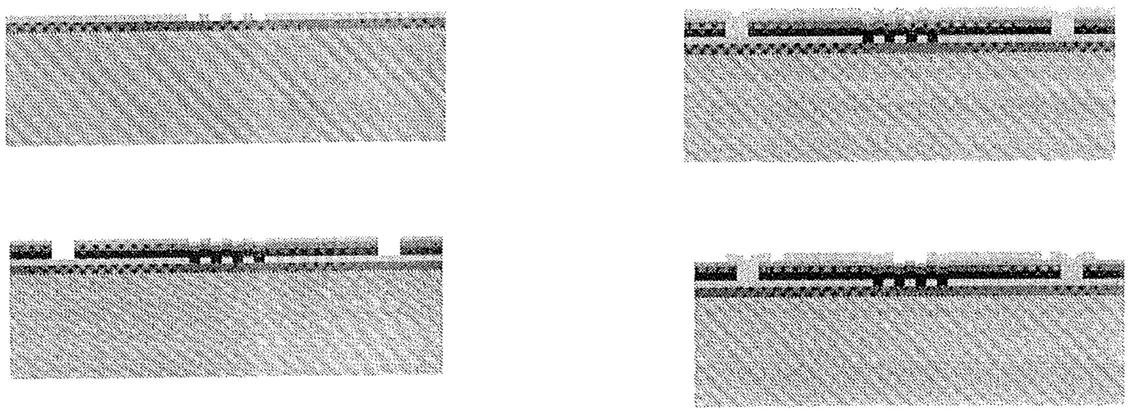


Fig. 6. MIS technological process steps for the realization of polysilicon resistor for flow sensors.

TEOS, 800 nm BPSG is deposited, patterned to contact polysilicon and then reflowed at 925 °C. A 100 nm TEOS and 150 nm Si_3N_4 layers are then LPCVD deposited and patterned to connect the resistor. By sputtering Ti and TiN (30 nm and 200 nm, respectively) and Al (360 nm) are performed to obtain the bonding pads for the polysilicon resistor. The frontside of the wafers is then covered by 800 nm Low Temperature Oxide (LTO) and patterned to contact the metal pads.

Also in this development no attempt will be made toward full CMOS compatibility. The required electronics, tailored to specific applications, will be designed as a separate CMOS chip to be connected externally and mounted in the same sensor hybrid package.

c) microheaters for gas sensors

Chemoresistive, thin- and thick-film gas sensors based on metal-oxide semiconductors necessitate suitable heating modules to achieve the relatively high temperatures (in the range of 300-400°C) required for optimal sensor sensitivity /7, 8/. Basic requirements for such heating modules are excellent temperature uniformity over the sensitive surface area, small dimensions, and minimal power consumption. The latter requirement is essential for portable battery operated gas monitoring systems. Microheater modules consisting of a dielectric stacked membrane micromachined from bulk silicon, with an embedded polysilicon resistors acting as heating and temperature monitoring elements have been developed and are now routinely fabricated by a dedicated process. The microheater enables a temperature up to 500°C to be achieved with a power consumption of less than 30mW. The simplified flow chart of the microheater fabrication process available in IRST is shown in fig. 7. The silicon is anisotropically removed from the backside by TMAH etching, leaving a $2.5x2.5mm^2$ thin diaphragm supported by a surrounding silicon rim. The $5x5mm^2$ chips resulting from wafer dicing are covered by the thick film sensor and mounted and bonded onto TO5 metal cans. A top-view photograph of a fabricated device is shown in fig. 8.

Also in this example the thermal behaviour of the structure was investigated through simulations performed using the finite-element analysis program SOLIDIS. Fig. 9 shows a contour plot of the simulated temperature distribution within the $150x210\ \mu m^2$ n+polySi heater area at a heating power of 27.5 mW. A maximum temperature of 490 °C is achieved. By thermal simulation in air and in vacuum it can be seen that, at 490 °C, almost two third of the electrical power provided to the module is dissipated by heat losses to the air.

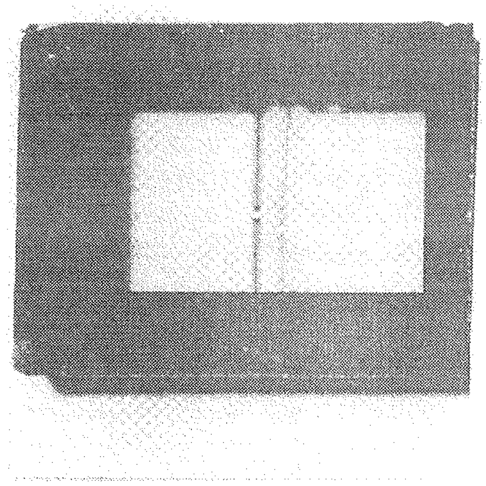


Fig. 8. Top-view photograph of a fabricated device

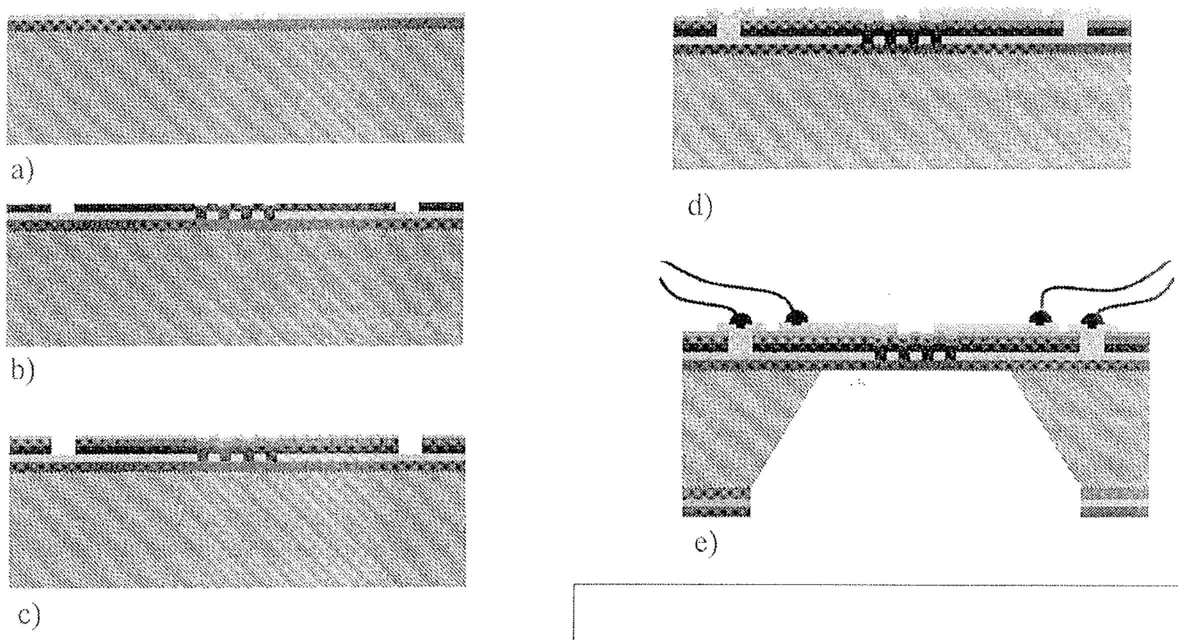


Fig. 7. Gas sensor microheater main technological steps

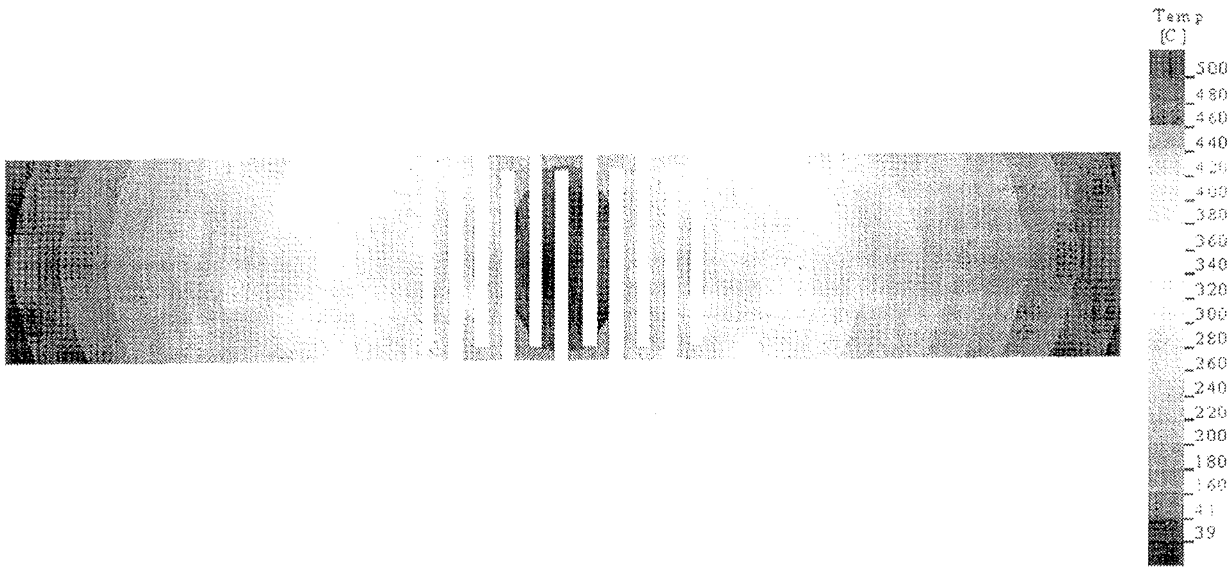


Fig. 9. 2D temperature map within the polysilicon resistor for a heating power of 27.5 mW

d) microcomponents for MW and MMW

Silicon bulk micromachining is becoming an interesting area of activity in the framework of microwave (MW) and millimeter wave (MMW) devices, because of its promising improvements for packaging, decrease of insertion losses and dispersion control /9, 10/. Simple configurations like coplanar waveguides (CPWs) offer such possibilities up to more than 100GHz, and they can be easily used for planar interconnections. Moreover, owing to an intrinsically improved ground control, CPW are favoured for the next generation of MMW subsystems, being suitable of applications for simple interconnections as well as for MMIC and sensor applications.

Coplanar waveguide structures were fabricated on dielectric membranes. The substrates were high resistivity (5 kΩ·cm) <100> p type Si wafers. The dielectric membrane, used to support the coplanar waveguide, was a three-layer of $SiO_2/Si_3N_4/SiO_2$ with an effective dielectric permitivity close to 1. On the backside of the wafers, the same three -layer is used as a hard mask for the TMAH anisotropic etching. 30 nm of Cr and 2.3μm of Au were thermally evaporated and then the desired structures were obtained by wet etching. An example of a 75 Ω micromachined coplanar waveeguide is shown in fig.10.

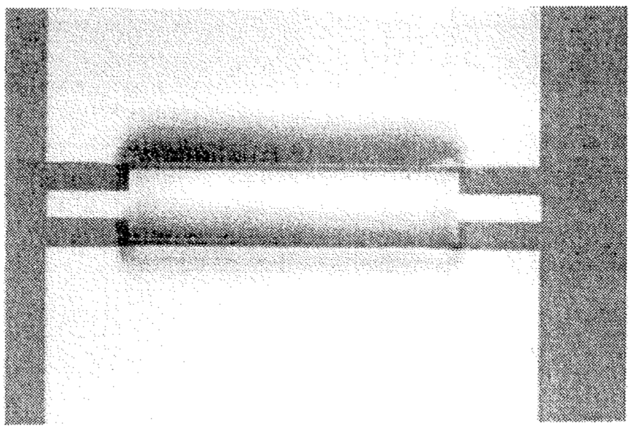


Fig.10. Top view of a coplanar waveguide over the dielectric membrane. The central section of the Au line over the membrane, is 1500 μm long.

e) biomedical microsystems

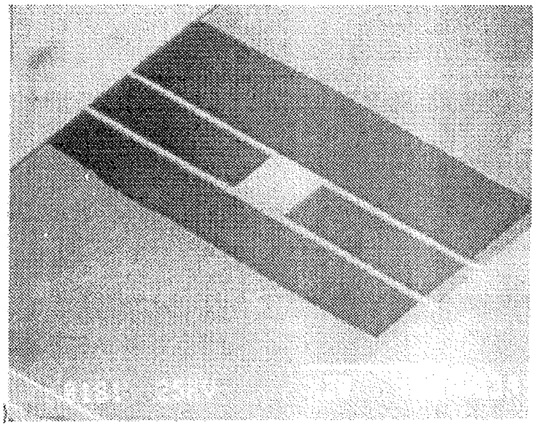
A new activity worth mentioning refers to biomedical application. The proposed research project will be directed towards the design, fabrication and characterisation of silicon integrated microsystems specifically designed for cancer detection and therapeutics. The term silicon microsystem here refers to microfabricated silicon based structures with biologically activated functions that are realised using standard integrated circuit processing techniques coupled with micromachining techniques /11/. The first project, now under development, refers to a microdevices where the integrated pressure and flow microsensing unit is to be used externally in order to detect urinary disfunction by simultaneously measuring bladder pressure and urine voiding rate as a function of time. These parameters render characteristic pressure-flow signature patterns related to a normal urodynamic condition, and to either abnormal constrictive or compressive obstructions. The device, fitted on a rigid tube attached either to an open-ended condom or onto a modified funnel, can be used to take instantaneous measurements during an annual prostate examination. The same device can be used for in-home monitoring, with the microsensor interfaced with a memory chip for recording yearlong pressure-flow data. The memory chip is then taken to a urologist for data analysis and interpretation on a yearly basis. In this way, changes in urodynamic behavior can be monitored, and any anomalies from the normal function can be identified for a specific period in time.

The miniaturisation of such a sensor allows for disposability and ease of use during bladder voiding. Most importantly, a take-home unit minimises the overall level of discomfort during regular prostate examinations. The fabricated microsensors will be tested parametrically in order to have a feed-back on the technological process: a complete functional characterisation of the devices behaviour will follow before developing the subsequent superficial treatment and the in-vivo tests. In addition, the design will be optimised to reduce cross-sensitivity issues such that measurements of pressure and flow can be taken without one measurand affecting the other.

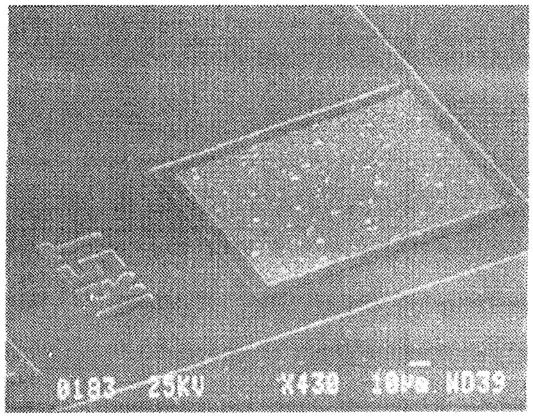
The prototype chip will be attached to a standard 40-pin dual-in-line package and a plastic tube with a hole cut in the sidewall was firmly attached to the sensor's active region. The hole in the tube will be fitted above the silicon membrane region forming a leak-proof flow channel over the sensor. Pressure sensitivity testing will be performed by sealing one end of the tubing while applying a known pressure using compressed air at the other end.

f) microcalorimeters for High Energy Physics

The above mentioned TMAH etching conditions for aluminum passivation were used to develop a micromachining module aimed to the realisation of three dimensional suspended microcalorimeters (also called microbolometers) in order to optimise the device performances in terms of energy resolution /12/. The dual-doped TMAH solution, beeng passivated with respect to aluminum, permits to simplify both the device fabrication process and the post-processing procedure. As it is shown in Fig. 11 (a) and (b), the microbolometers have been processed with no low temperature oxide (LTO) above the metal pads as metal protection layer. The <100> silicon etched surface shows no hillock protusion on it. Moreover, the absence of oxide protection layer reduce the stress on the suspended bridges.



a)



b)

Fig. 11 SEM micrographs of a suspended bolometer (a) and of an aluminum pad with no oxide protection (b).

The Si-implanted thermistor is made by integrating within the suspended layer a resistance doped just below the Metal Insulator Transition, corresponding to the sensitive volume of the thermistor, and by two contact diffusions and low-resistance metal connections for the thermistor electrical contacts. Because the temperature coefficient T_0 for a resistor following the Variable Hopping Range Coulomb gap model is extremely sensitive to dope not uniformly, in principle the resistance should have a box doping profile with a high doping volume uniformity. Furthermore, the doping profile should extend as deep as possible into the bulk silicon in order to obtain an adequate sensitive volume. These requirements can be reasonably satisfied by a series of successive implants with different doses and energies, followed by an appropriate annealing step. In our devices the multi-implant for the thermistor resistance is performed through a photoresist masking of the regions external to the active area. Five Phosphorous implants are necessary to obtain a flat (within few percentages) doping profile, ranging from 0.1µm to 0.6µm under the surface. The profile has been optimised by process modelling. A subsequent series of five Boron implants is necessary in order to partially compensate the thermistor resistance. After photoresist removal the multi-implant is electrically activated. This is accomplished by a thermal treatment aimed at full dopant activation and implant induced damage removal, but at the same time preserving as much as possible the box like implant profile. Prototipes with an energy resolution of the order of 15eV have been obtained.

Conclusions

Silicon micromachined sensors and devices already available for small volume production or under development at IRST Microsystem Division have been presented. No attempt is made toward CMOS compatibility. The IRST microsystem approach favours hybrid solution, where the components are fabricated by dedicated processing and separately mounted and interconnected together and with the IC driving electronics onto a dedicated package.

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Prispelo (Arrived): 15.10.99 *Sprejeto (Accepted): 25.11.99*