THERMAL BOUNDARY CONDITIONS IN SMART POWER DEVICES

Martin Knaipp, Franz Unterleitner,
Austria Mikrosysteme International AG, Unterpremstätten, Austria

Keywords: semiconductors, smart power devices, device models, thermal boundary conditions, selfheating, state of the art, device simulations, comparisons between formalisms, DD formalism, Drift Diffusion formalism, HD formalism, HydroDynamic formalism, SOR, Safe Operation Regime, increased temperature, degradation of device operation, permanent device failure, practical examples, experimental results

Abstract: This work gives a review of the state of the art device simulation including selfheating effects. A comparison between the Drift-Diffusion and Hydrodynamic formalism is given. Especially the influence of non-local effects in the lattice heating is shown. The influence of the interface and contact conditions on the final lattice temperature is described. It is shown that only a correct formulation of the boundary conditions enables energy conservation of the simulated device. But even in case of energy conservation, the contact conditions are the critical uncertainty in the description of the device behaviour.

Izbira termičnih robnih pogojev pri modeliranju inteligentnih močnostnih vezij

Ključne besede: polprevodniki, naoprave močnostne inteligentne, modeli naprav, pogoji termični mejni, samosegrevanje, stanje razvoja, simulacije naprav, primerjave med formalizmi, DD formalizem drita difuzije, HD formalizem hidrodinamični, SOR režim delovanja varnega, temperatura povišana, degradacija delovanja naprave, izpad naprave trajni, primeri praktični, rezultati eksperimentalni

Izvleček: V prispevku opisujemo trenutno stanje na področju termične simulacije elektronskih elementov z upoštevanjem efektov samosegrevanja. Podajamo primerjavo med tokovno-difuzijskim in hidrodinamičnim pristopom. Še posebej poudarimo vpliv nelokalnih efektov pri segrevanju kristalne mreže, kakor tudi vpliv kontaktov in medpovršin na končno temperaturo kristalne mreže. Pokažemo, da le s pravilno izbiro robnih pogojev omogočimo ohranitev energije simuliranega elementa. Vendar celo v takem primeru so pogoji na kontaktih kritična neznanka pri pravilnem opisu obnašanja elementa.

I. Introduction

In modern semiconductor devices the selfheating effects play the major role in the specification of the safe operation regime (SOR). The increase of the lattice temperature during the operation can cause a complete different device behaviour, an accelerated degradation or even a permanent device failure (e.g. second breakdown). At least the local lattice temperature of the chip is a critical factor which determines if the IC fulfill its specification.

To optimize the system performance, sophisticated device simulations are needed which should also include selfheating effects. Typical devices where selfheating plays a major role are smart power devices, electrostatic discharge structures (ESD) and structures with low thermal conductivity components like silicon on insulator devices (SOI).

Modern device simulators are tools to solve nonlinear coupled partial differential equation systems. Their numerical behaviour is optimized for the semiconductor equations to find a solution in the shortest time with an accuracy which can be defined by the user. The numerical discretisation scheme is so sophisticated that even variations in the carrier concentrations in a range of 20 orders of magnitude can be solved. This is not trivial and major efforts are carried out to find new robust numerical schemes to solve the specified equation systems /1/. The feedback from the device lattice temperature to the electrical behaviour is given by the various physical models which depend on the lattice temperature. Some examples are the carrier mobility, the densities of states and the band edge energies /2,4,5/.

The calculated solution inside the device strongly depends on the given boundary conditions. The specification of these conditions is not easy and has to be done by the user. The specification of electrical conditions is quite simple. In most time the potential drop in the interconnect metal (backend) can be neglected to describe the electrical device properties in a moderate current regime. The development of power devices is often done with a large scaled interconnect to avoid any potential drop in the metal or poly lines.

However the thermal boundary conditions cannot be defined as simple as the electrical case. The thermal influence of the backend cannot be reduced, and much knowledge is necessary to estimate realistic thermal conditions. In addition it is not easy to decide to which metal or poly line the user should simulate the devices. At least the final SOR is determined by the complete packaging of the device. This thermal packaging includes a temperature drop in the packaging material, in the bonding wires of the IO cells and in the pins of the chip. All these materials finally determine the local device temperature and therefore the boundary conditions of the semiconductor.

To simulate a modern semiconductor device the user has to provide the simulating structure to the device simulator. In the general case this structure consists of several segments. Each segment corresponds to a certain material. Typical materials are silicon, poly lines, oxides, interconnect dielectric, etc. However it is not always useful to describe even the complete silicon with one segment /3/. A typical example is the hetero bipolar transistor (HBT) with a silicon/germanium (SiGe) base. The major reason to describe silicon with several seg-

ments is the simulation time which can be kept low while including all necessary models. In case of the HBT only the base is evaluated with the sophisticated SiGe models while in the other segments the plain silicon models are used.

II. Segment Models

In this section a review of the heat source term is given within the Hydrodynamic (HD) and Drift-Diffusion (DD) model /2,5/.

The equation to describe the lattice temperature is the lattice heat flow equation (1). On the right hand side the heat source term H corresponds to a power density which heats up the device segments. The formulation of the heat source term depends on the used equation set. The complete equation (1) describes the transient behaviour of the selfheating. The heat conductivity κ depends weakly on the lattice temperature. The second term on the left side of (1) describes the time dependent part of the equation where the thermal heat capacity ρ defines the material dependent properties. In case of a stationary solution of the selfheating problem, the second term on the left side of (1) vanishes.

$$-\mathrm{div}\left(\kappa_L(T_L)\right)\cdot \mathrm{grad}\left(T_L(\vec{r},t)\right)+\rho_L\cdot c_p\cdot\frac{\partial T_L}{\partial t}=H(\vec{r},t) \tag{1}$$

In case of the DD model the source term is given in (2). When a stationary simulation is done, H only depends on the position. For pure silicon the electron and hole band edges E_C and E_V are often assumed to be constant. Only in high doped regions the band gap narrowing has to be included. In case of recombination, the recombination rate R_{net} is multiplicated with the bandgap E_g to give the recombination heat.

$$H(\vec{r})=\mathrm{grad}\left(\frac{E_c}{q}-\psi\right)\cdot\vec{J_n}+\mathrm{grad}\left(\frac{E_v}{q}-\psi\right)\cdot\vec{J_p}+R_{net}\cdot E_g \tag{2}$$

In the HD model the heat source term H is given in (3). The first two terms of (3) describe the carrier energy which is transferred to the lattice. The amount of the energy is proportional to the difference of the carrier and the lattice temperature. This means that the carriers can give their thermal energy to the lattice even if they are not accelerated by an electric field. The hot carriers relax with the cold lattice and the first two terms of (3) are therefore called relaxation terms. The terms $H_{n,eff}$ and $H_{p,eff}$ describe the net recombination heat of the corresponding carrier system. It is assumed that the recombination term heats up the lattice in case of recombination and cools down the lattice in case of carrier generation. The calculation of these terms is not easy because it is not so clear how to split the recombination or generation heat between the carrier energy systems and the lattice heat system. At least in case of high currents the heat transfer caused by recombination or generation is small compared to the energy transfer of the relaxation terms.

It is important to note that in space charge regions the carriers are heated up by the electric field. In these regions the final carrier temperatures can reach several thousand Kelvin. The reason why the semiconductor does not melt is the low energy density of the carriers because of their low concentration. On the other hand, in regions with high carrier densities (e.g. in case of high injection) only a moderate carrier heating can be achieved.

$$H(\vec{r})=\frac{3\cdot k_B}{2}\cdot\left(n\cdot\frac{T_n-T_L}{\tau_{\varepsilon,n}}+p\cdot\frac{T_p-T_L}{\tau_{\varepsilon,p}}\right)-H_{n,eff}-H_{p,eff} \tag{3}$$

As long as the carriers give their thermal energy to the lattice, the first two terms of (3) are positive values. However, it is possible that carrier temperatures are below the lattice temperature as shown in the example section.

III. Interface and Contact Models

A) Interface Model

The interface model described in this section deals with the interface of two adjacent semiconductor segments. In the general case there are different values of the band edge energies on each side. An example is the emitter/base interface of a Si/SiGe HBT device, where a carrier current crosses the interface. The boundary condition for the potential at the interface is simple because there is no interface dipole charge and so the electrostatic potential on each side of the interface must be the same. However the carriers move at their band edge energies which might change abruptly at the interface.

Because of this abrupt change the heat source term for the DD model according to (2) leads to an infinite large power density at the interface. Fortunately the heat transfer must not be calculated explicitly. The limes of this boundary problem leads to a surface divergence of the lattice thermal heat flux density S, which in turn changes the slope of the lattice temperature at the interface. On both sides of the interface the lattice temperatures are set equal. Equation (1) therefore reads for the DD hetero interface model:

$$\mathrm{div}\kappa_L\cdot\mathrm{grad}(T_L)=\mathrm{div}\cdot\vec{S_L}=\frac{\vec{J_n}}{q}\cdot(E_{c1}-E_{c2})+\frac{\vec{J_p}}{q}\cdot(E_{v1}-E_{v2}) \tag{4}$$

In case of the HD model the non-local effects have to be taken into account. This means that the abrupt change of the band edge energies cause a surface divergence of the carrier energy flux and not of the lattice thermal heat flux. The change of the carrier energy flux at the interface defines the shape of the carrier concentrations and their temperatures across the interface. Again the lattice temperatures on both sides of the interface are equal. At least the HD interface model only affects the carrier energy flux, and the lattice is only incorporated by the volume model according to (3).

B) Contact model

The two commonly used thermal contact models are the isothermal contact condition and the condition of a thermal contact resistance. These two conditions can be applied for ideal electrical conductors, for ideal electrical isolators and real electrical conductors (e.g. adjacent semiconductor segments). The option for adjacent semiconductor segments makes it possible to calculate the selfheating only in defined segments, to achieve shorter simulation times. The isothermal condition specifies a certain contact temperature for the contact boundary. This corresponds to a Dirichlet boundary problem of (1).

In contrast the specification of a thermal contact resistance defines a Neumann boundary problem for the energy flux of (1). The physical meaning of this condition is that the amount of heat flux, which crosses the boundary, is proportional to the difference of the boundary temperature and the temperature of a specified thermal heat sink.

The specification of these setup conditions seems to be simple, but each condition can lead to numerical and physical problems if a wrong specification is used. In case of the isothermal condition it is possible to simulate an overheated device with an arbitrary small current. The reason therefore is a too small chosen contact area, which leads to wrong simulation results. If a thermal resistance is defined and the resistance is too high, the device may heat up to arbitrary high temperatures even if the device current is low and the contact areas are large. This can result from an inaccurate definition of the simulation structure as described in a previous section.

If an electric current crosses the boundary, the simple thermal contact models have to be extended to electro/thermal contact models. These models include the energy transfer when the carriers move from the contact metal to the semiconductor. The energy diagram of the metal/n-doped semiconductor contact is shown in Fig.1.

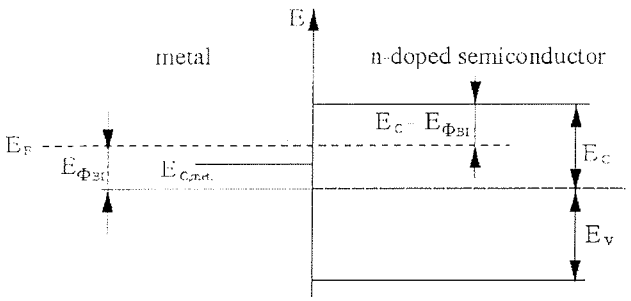

Fig.1: Bandedge energy diagram on a metal/n-doped semiconductor contact.

In case of a contact current the carriers gain or loose energy because of the difference between the metal Ferminiveau E_F and the corresponding conducting band E_C or E_V of the semiconductor. It should be noted that the intrinsic level of the semiconductor is shifted by the Build-In energy $E_{\Phi BI}$. In case of a n-doped semiconductor the barrier of the electrons is much lower compared to the barrier of the holes. If we assume a n-doped device with nearly equivalent electron and hole currents, it is easy to see that the hole current gives the main part of the carrier contact heating or cooling.

A similar contact bandedge energy diagram can be given for a p-doped semiconductor. Only when all current semiconductor/metal boundaries are incorporated by this model, an energy conservation of the device can be shown as described in (5).

In this equation the electrical power dissipation of m electrical contacts is equal to the lattice heat flux of n thermal contacts. The vector A corresponds to the boundary normal area and defines the sign of the power

$$\sum_{i=1}^{m} \vec{A}_i \cdot \vec{J}_i \cdot U_i = \sum_{j=1}^{n} \vec{A}_j \cdot \vec{S}_{L,j} \qquad (5)$$

dissipation. Equation (5) also holds for hetero devices and even for multi segment structures.

IV Examples

This section will give two examples which should show the effects explained in the previous sections. First a simple two segment silicon diode with an abrupt p/n junction is described. The second example shows the selfheating of a hetero bipolar field transistor. Both were simulated with the stationary semiconductor equation set, which means that there is no transient thermal and electrical behaviour .

A) The Diode

The example was chosen because a bias applied in forward direction results in high electron and hole currents. This allows to verify the contact and interface conditions as described in section II. The device is modeled as a two segment structure with a step junction at the segment interface and a constant doping in each segment of about 1.0e17cm^{-3}. Two contact resistances are applied with values of R_{th} = 6.9e-5 [K cm^2/W] on each side. The device has a length of 60 μm and a contact area of 6 μm^2.

Fig.2 shows the diode with an applied forward voltage of +0.6 V at the anode (left side). The left part of the figure shows the lattice heating while the right side shows the band edge potentials of the device. The most upper line of the band edge potentials corresponds to the hole potential which is followed by the device potential and the lowest line corresponds to the electron potential. In thermal equilibrium that means without an applied voltage, the potential drop at the junction corresponds to the Built-In potential which is about 0.82V. One should be aware that in the vicinity of the junction the potentials are continual functions without any unsteadiness at the physical junction. The right side of Fig. 2 shows that at a contact bias of 0.6V the junction voltage drop is already reduced to 0.22V. This voltage drop causes a high diffusion current over the junction with an electron to hole current ratio of nearly 2.5. This ratio is mainly determined by the different mobilities of

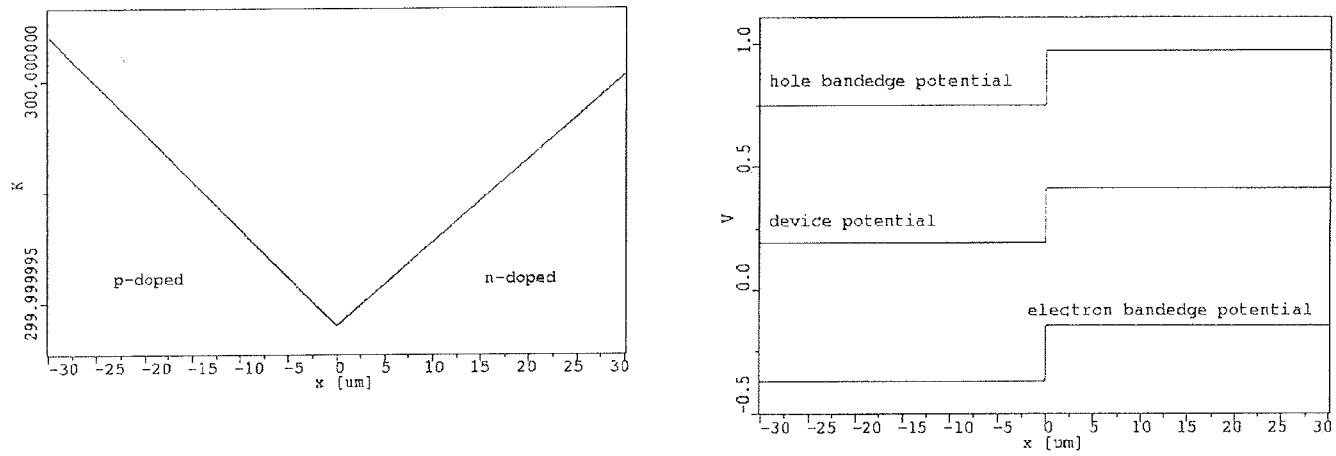

Fig. 2: Lattice temperature (left diagram) and band edge potentials (right diagram) of a diode in forward direction. The applied cathode voltage is 0.6V. The electrons move from the right to the left.

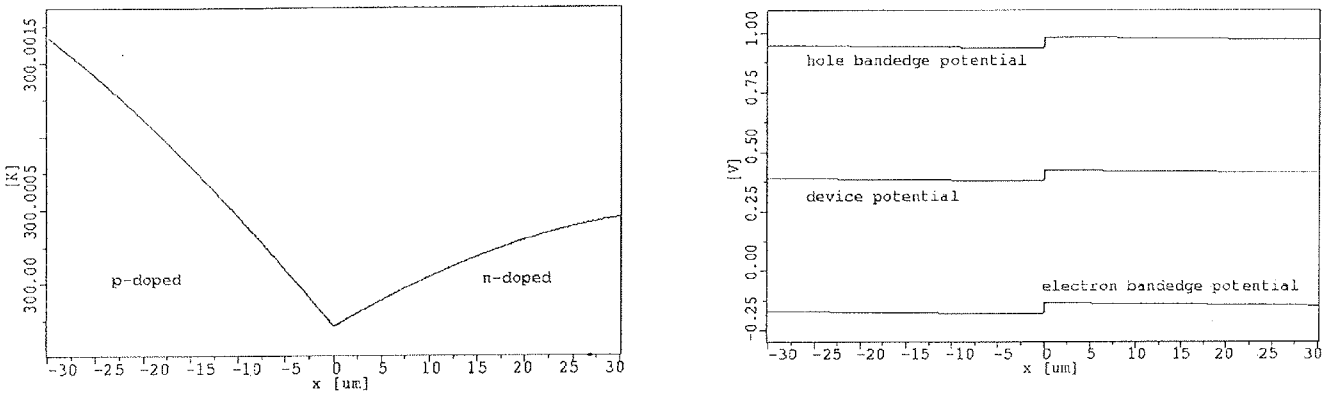

Fig. 3: Lattice temperature (left diagram) and band edge potentials (right diagram) of a diode in forward direction. The applied cathode voltage is 0.8V. The electrons move from the right to the left.

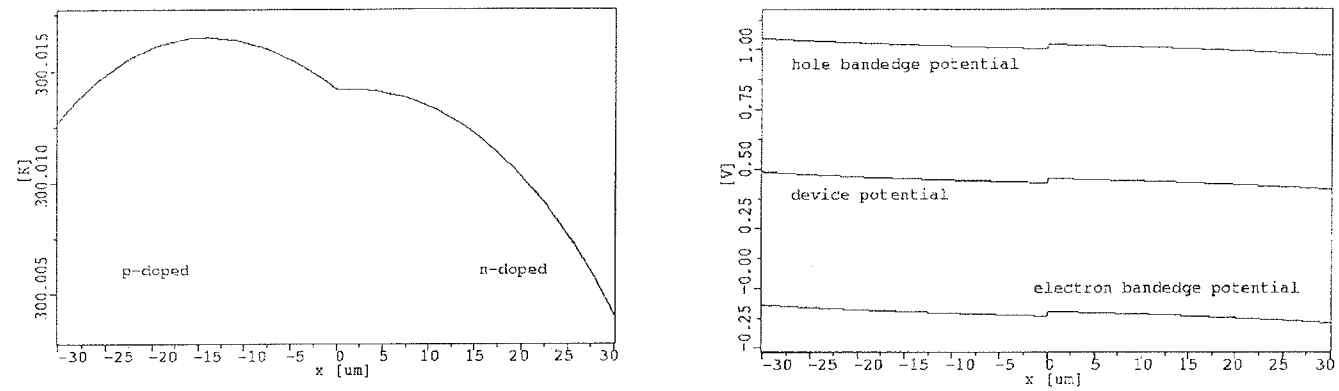

Fig. 4: Lattice temperature (left diagram) and band edge potentials (right diagram) of a diode in forward direction. The applied cathode voltage is 0.9V. The electrons move from the right to the left. The maximum lattice temperature is in the p-doped side. From this point the lattice heat flux flows to the anode contact and the heat sink of the p/n junction.

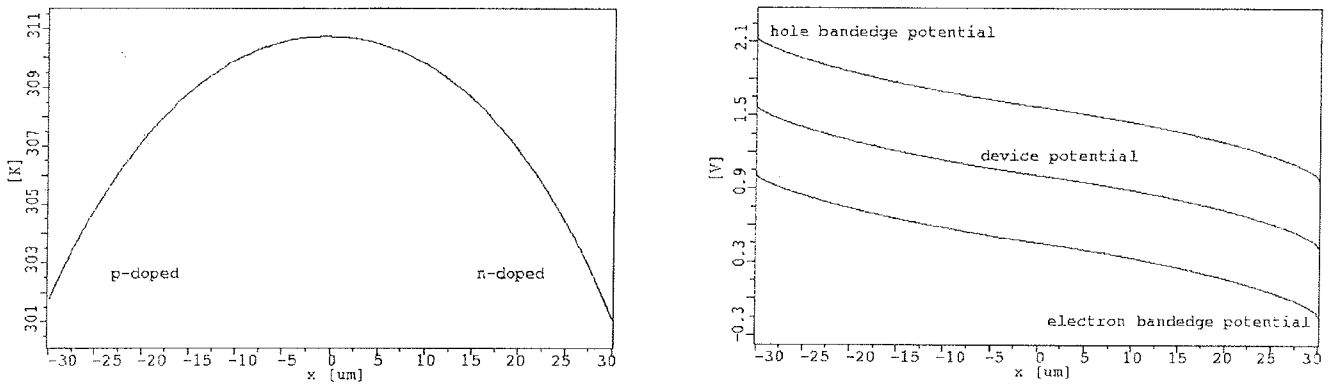

Fig. 5: Lattice temperature (left diagram) and band edge potentials (right diagram) of a diode in forward direction. The applied cathode voltage is 2.0V. The electrons move from the right to the left. The maximum of the lattice temperature is at the p/n junction. The device overheating is relatively high compared to the increase of the contact temperature. In a more realistic application the contact resistance would be higher so that the final lattice temperature would be also higher.

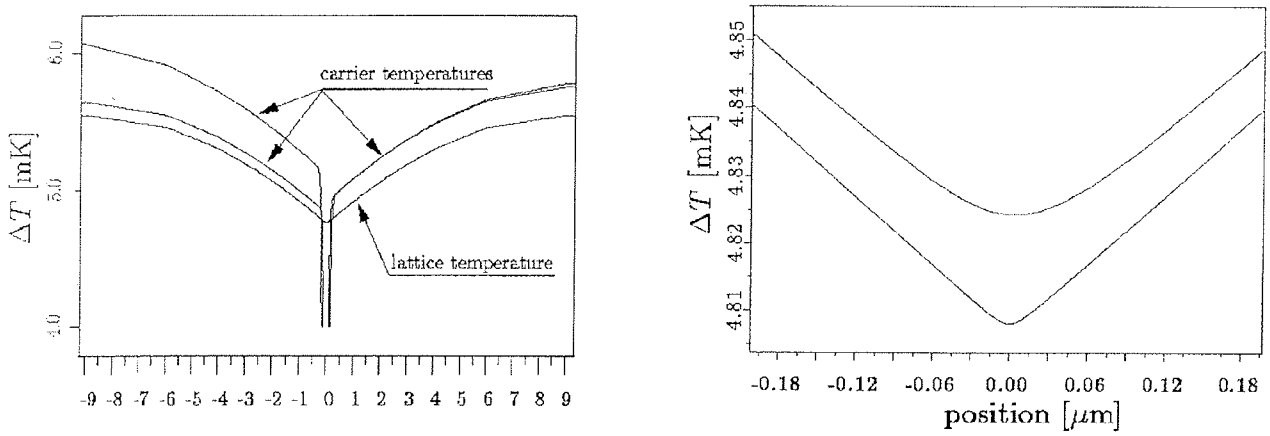

Fig. 6: Lattice temperature and carrier temperatures (in case of the HD simulation) of the diode with an applied voltage of 0.8V in the region of the p/n junction. A comparison between the DD and HD lattice temperature is given on the right side, which shows in more detail the lattice temperatures in the area of the p/n junction.

the electrons and holes. While the electrons move from the right to the left side, they have to overcome the cathode/n-doped semiconductor barrier. In the contact area they have to move against the electric field. This results in a lattice cooling because the energy gained by the carrier is needed to overcome the barrier. At least the net energy transfer from the carrier to the lattice is positive because the barrier for the holes, which leave the semiconductor at the cathode side, is much higher compared to the electron barrier.

One can see that the final lattice heating is highest at the anode contact of the device. This corresponds to a higher electron current, which finally results in a higher net heating of the anode contact. At the p/n junction a heat sink causes a strong lattice cooling. This sink is the remaining barrier of the Built-In potential drop where both carrier types have to overcome a potential barrier, which leads to the strong cooling effect. It should be noted that the net device heating is positive which means, that there is a lattice heat flow out of each contact. However this heat flow is not shown in the figure since only the silicon segment is calculated and not the heat flow inside the idealized contact. An indicator for a lattice heat flux out of the device is a raised contact temperature caused by the thermal contact resistance.

Fig. 3-6 show the increase of the lattice heating caused by the higher applied voltages. The Built-In potential nearly vanishes at high forward biases (and also the heat sink at the p/n junction), and the current is mainly caused by a drift current. At least the anode contact temperature is higher than the cathode temperature, which is the result of the higher electron current.

Fig. 6 shows the difference behaviour of the applied HD and DD equation set. The applied cathode voltage is

0.8V. In the figure the cooling of the p/n junction is shown. On the left side the temperatures of the lattice and of the carriers (in case of the HD simulation) are shown. At the junction the carriers are cooled down strongly because they have to overcome the Built-In barrier. This strong cooling is the result of the low carrier heat capacity. When the carrier temperature is below the lattice temperature the carriers are heated up by the lattice. The consequence is that the lattice looses thermal energy, which results in the lattice cooling at the p/n junction. The lattice cooling caused by the carriers is the result of the heat source term of the HD model (3) where the difference of the carrier and the lattice temperature becomes negative. The right side shows the shape of the lattice temperature in case of the HD (upper curve) and the DD simulation (lower curve). It should be noted that the carrier energy relaxation length l is the product of the saturation velocity v_{sat} = 10^5 m/s and the energy relaxation time τ_E =0.6 ps, which is about 0.06 μm. This value corresponds to the radius of the temperature distribution in the area of the junction.

B) The Hetero Bipolar Transistor

The last example shows the selfheating simulation results of a SiGe HBT with different specified boundary conditions. The simulated device consists of three segments, two silicon segments for the emitter and collector regions and a segment for the SiGe base. The two-dimensional device has a n-doped emitter (10e19cm^{-3}), a p-doped base (10e19cm^{-3}) and a low doped collector (2.0e17cm^{-3}). A buried layer, which starts below the low doped collector region gives a low device resistance. The base has a graded germanium fraction of 0%-20%. The germanium inside the base causes an accelerating field for the electrons which results in a fast transition time of the electrons trough the base.

To study the selfheating effects the applied voltages should enable high current densities. For this reason the base and collector voltage are about 1V, while the emitter is grounded. In this regime the base push out effect dominates the device characteristic, which causes a reduction of $\beta = I_C/I_B$ (β roll off). At this operating point the hole current supplied by the base is about a factor 13 lower than the collector current. To simulate more realistic conditions a thermal collector resistance of R_{th} =1.5e-4 [K cm^2/W] is specified. This condition assumes that the generated heat is transferred through the silicon bulk to the outside of the device. Because of the backend, the emitter and base contacts have a much lower ability to transfer the generated heat outside of the active area. In Fig. 7 the band edge and device potentials are shown.

The maximum potential drop is in the low doped collector region. The electrons move towards a positive potential and so the maximum power density in the collector region is at position x=-0.2, where the high doped buried layer starts. A second heat source is located in the SiGe base, where the electrons are accelerated by the drift field. The holes inside the base move towards a positive potential, which results in a lattice cooling. At least the fraction of the hole current is

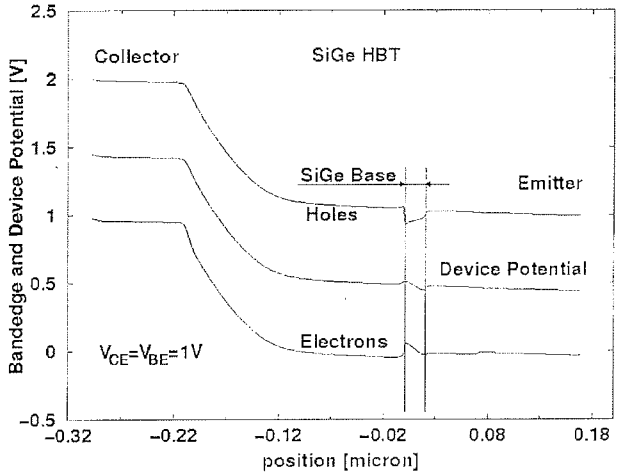

Fig. 7: Band edge potentials and device potential of the simulated SiGe HBT. The germanium fraction inside the base is graduated. The mole fraction is about 0% at the emitter/base interface and reaches the maximum value of 20% at the base/collector interface.

small compared to the electron current, so that the net energy transfer inside the base heats up the device. Fig. 8 shows the two dimensional temperature distribution of the heated device.

To estimate the sensitivity of the boundary conditions, the device heating is simulated with two different contact conditions. The sections of the two vertical temperature distributions is given in Fig. 9. The lower curve is the simulation result with a Neumann condition at the emitter contact, which means that there exists no heat transfer over the contact. This assumption is not realistic since a current crosses the contact. The specified Neumann condition neglects any contact heat and acts

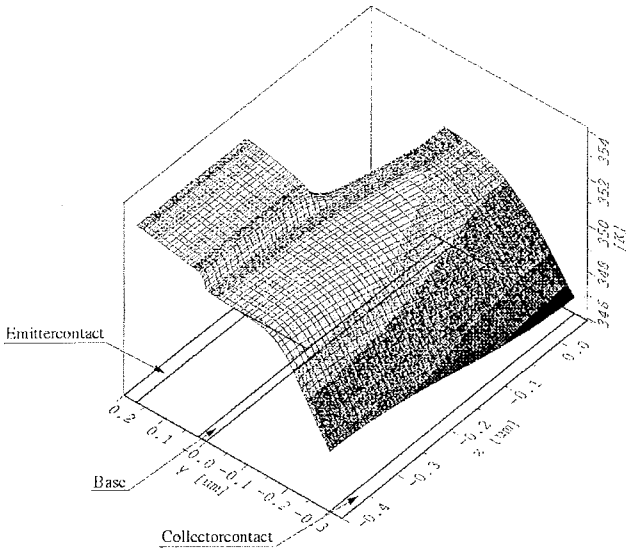

Fig. 8: Two-dimensional device heating with an applied electro/thermal contact model at the emitter contact which ensures energy conservation inside the device.

like a semiconductor/vacuum boundary. At least the thermal heat flow has a horizontal tangent towards the emitter contact.

In the second condition an electro/thermal contact with a very high thermal resistance is specified for the emitter contact (about 8 orders of magnitude higher than the collector contact). The simulation result is shown in the upper curve of Fig. 9 and ensures energy conservation. The contact heat, which leads to a lattice heating for both carrier types, causes a change in the slope of the lattice heat flux at the semiconductor/contact boundary. With these conditions nearly the complete generated heat leaves the device outside the collector contact. The final temperature distribution is higher compared to the Neumann condition, although in both simulations nearly no heat flux flows out of the emitter contact.

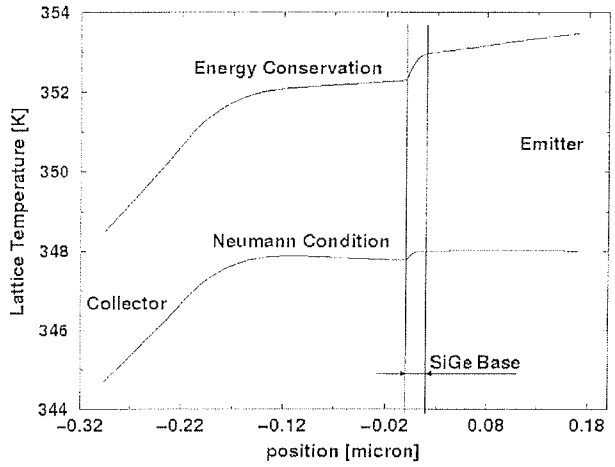

Fig. 9: Lattice temperatures of the two different emitter contact models. The vertical cross section of the device belongs to the position x=-0.4μm in Fig. 8.

A last a point has to be discussed to explain the lattice temperature distribution around the base area. Looking at Fig. 8 and Fig. 9 one would expect a heat sink near the base/collector junction. The sink exists because the electrons have to overcome the base/collector barrier. This barrier is the result of the decreased bandgap inside the base caused by the germanium fraction. But the second and much more dominant effect is the reduction of the thermal heat conductivity caused by the germanium atoms. At the maximum mole fraction of 20% the thermal heat conductivity is approximately reduced by a factor 10. The difference between a thermal heat sink and a variation in the heat conductivity is, that in the first case local minima in the lattice temperature distribution can appear. In the second case the sign of the slope of the lattice temperature does not change.

Acknowledgment

For the device simulations the generic device simulator MINIMOS-NT was used. MINIMOS-NT is a development of the Institute for Microelectronics, TU-Vienna. The author would like to thank the members of the institute for their fruitful discussions in the topic of self-heating.

References

/1/ W.S. Choi, J.G. Ahn, Y.J. Park, H.S. Min, C.G. Hwang. A Time Dependent Hydrodynamic Device Simulator SNU-2D With New Discretization Scheme and Algorithm, Trans. Computer-Aided Design,1994, Vol 13, No 7, p. 899-908

/2/ M. Knaipp. Modelling the Influence of Temperatures in Semiconductor Devices (written in German). PhD. Thesis. 1998, Institute for Microelectronics, TU-Vienna. http://www.iue.tuwien.ac.at/diss/knaipp/diss/diss.html

/3/ T. Simlinger. Simulation of Heterostructure Fieldeffect-transistors (written in German). PhD. Thesis,1996, Institute for Microelectronics, TU-Vienna. http://www. iue.tuwien.ac.at/diss/simlingerldiss/diss.htm 1

/4/ K. Kells. General Electrothermal Semiconductor Device Simulation PhD. Thesis, 1994, Hartung-Gorre 1994, ISBN:3-89191-787-2

/5/ S. Selberherr, Analysis and Simulation of Semiconductor Devices Springer 1984, ISBN:3-211-81800-6

Dr. Martin Knaipp
Process Engineer
Research & Development
Austria Mikro Systeme International AG
Schloss Premstätten
A-8141 Unterpremstätten
Austria
Fax.: ++43 (0) 3136 52501, 53650
Phone: ++43 (0) 3136 500-681
E-Mail: martin.knaipp@amsint.com

Franz Unterleitner
Austria Mikrosysteme International AG
Schloss Premstätten
A-8141 Unterpremstätten
Austria
Phone: ++43 (0) 3136 500-327
E-Mail: franz. unterleitner@amsint.com

Prispelo (Arrived): 25.04.00 *Sprejeto (Accepted): 17.05.00*