RECENT DEVELOPMENTS IN SILICON RADIATION DETECTORS AT IRST

G. U. Pignatel[a], M. Boscardin[b], G.-F. Dalla Betta[b]
[a]Dipartimento di Ingegneria dei Materiali, Universita di Trento, Trento, Italy
[b]IRST, Divisione Microsistemi, Povo, Trento, Italy

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Abstract: In the last few years, the Institute for Research, Science and Technology (IRST) has been involved in a research program, supported by the Italian Institute of Nuclear Physics (INFN), aimed at setting up the technological capabilities for the production of double-sided silicon detectors for high energy physics experiments. We report on the most relevant achievements of this R&D activity, with emphasis on some recent results from the development of detectors oriented to ALICE (A Large Ion Collider Experiment) and ATLAS (A Toroidal LHC ApparatuS) experiments at LHC.

Najnovejša dognanja pri razvoju silicijevih detektorjev sevanja v IRST

Ključne besede: HEP fizika energij visokih, Si detektorji sevanja silicijevi, ALICE eksperimenti v trkalnikih z ioni velikimi, ATLAS aparati z LHC toroidnim, LHC trkalniki hadronski veliki, detektorji na osnovi mikrotrakasti dvostranski, tehnologija izdelave, rezultati eksperimentalni

Izvleček: V zadnjih nekaj letih je IRST (Institute for Research, Science and Technology) vključen v raziskovalni program, ki ga podpira Italijanski institut za jedrsko fiziko (INFN), katerega cilj je razviti tehnološke kapacitete za proizvodnjo dvostranskih silicijevih detektorjev sevanja za uporabo pri fizikalnih poskusih z visokoenergijskimi delci. V tem prispevku podajamo najnovejša dognanja razvojno-raziskovalnega dela s posebnim poudarkom na rezultatih, ki smo jih dobili pri razvoju detektorja za eksperimenta ALICE (A Large Ion Collider Experiment) in ATLAS (A Toroidal LHC ApparatuS) pri LHC

1. Introduction

Silicon radiation detectors have been extensively used as tracking devices in high energy physics experiments for quite a long time. In the last few years, considerable efforts have been dedicated by many research groups to the study and the improvement of the radiation hardness of these detectors in view of their massive application at LHC and for other high luminosity applications /1/. The possibility for these devices to be efficiently operated in very harsh radiation environments for the full lifetime of the experiments has required to cope with new design and processing aspects /2/.

Since 1997, we have been conducting a research program, supported by INFN (Italian National Institute for Nuclear Physics), aimed at setting up the technological capabilities for the production of double-sided microstrip detectors suitable for the challenging demands of the future high energy physics experiments. Within this framework, the main efforts have recently been dedicated to the development of microstrip detectors designed for ALICE, an LHC experiment aimed at the study of heavy ion collisions. Moreover, IRST has also been committed to the fabrication of ATLAS pixel detector prototypes.

In this paper the most relevant achievements of these technological developments will be presented. In particular, the main design and processing issues will be discussed and some selected results from the electrical characterization of microstrip and pixel detectors will be reported.

2. Development of a double-sided microstrip detector technology

Some preliminary results have already been reported at MIDEM Conference /3/, which demonstrated the feasibility of production of double-sided microstrip detectors at IRST. In fact, in spite of the lack of experience in double-side wafer processing, the first prototypes exhibited good electrical characteristics as well as a reasonably low defect rate, not far from the typical figures of high-quality double-sided detectors /4/. Further work has been going on since then, allowing for the fabrication process to be improved in many respects. In particular, two batches of double-sided microstrip detectors (SD2, SD3) were processed, allowing different technological options and design solutions to be evaluated.

Most of the technological development work was conducted using a dedicated wafer layout, consisting of three different microstrip detectors and several test structures. In particular, in order to have a first-hand comparison with detectors fabricated by other manufacturers, a reference detector was designed adopting as a model the layer 1 detectors for the Silicon Vertex Detector of the Babar experiment /5/, which were being

tested at INFN-Trieste. Although this design was not intended for operation in extreme radiation environments, it was deemed appropriate for the evaluation of the technology. This detector, in the following referred to as SB, consists of 384 strips, parallel on both sides of the wafers. The strip length is 5.1 cm, whereas the strip pitch is 50 μm; the strip width is 22 μm on the p-side and 14 μm on the n-side. The overall area occupation of the detector is 2.12×5.64 cm^2 (including the scribe-lines). Strip isolation on the ohmic-side is obtained by means of individual box-shaped p-stops. Strips are biased by poly-Si resistors placed at the opposite ends of alternate strips and all connected to a common metal bias-line. An implanted guard-ring surrounds the detector active area in order to properly shape the electric field and collect the edge leakage current.

Other detector layouts were considered, and several test structures were also present on the wafer, including: (i) standard test structures, intended as general diagnostic devices, among which a diode with guard-ring, gated-diodes and MOS capacitors (with both poly-Si and metal gate), coupling capacitors, Van der Pauw resistors, etc; (ii) dedicated test structures, aimed at the analysis of some particular aspects of the detector design and at radiation tolerance studies.

2.1 Fabrication technology

Detectors were processed at IRST on 100 mm-diameter, FZ, 300-μm-thick, <111>-oriented, n-type silicon wafers, with nominal resistivity of 6 kΩ·cm. The fabrication process can be outlined as follows:

- field oxide growth (wetO_2, 1 μm);
- p^+ (p-side) and n^+ (n-side) strip definition and field-oxide dry etching;
- screen oxide growth (dryO_2, 70 nm);
- p^+ (p-side) and n^+ (n-side) strip implantations;
- n-type scribe-line (p-side) definition, field-oxide dry etching and implantation;
- p-stop (n-side) definition, field-oxide dry etching and implantation;
- main oxide growth (dryO_2, overall thickness 100÷130 nm);
- TEOS deposition (100÷150 nm) for stacked capacitors;
- polysilicon deposition (350 nm), doping by ion implantation, patterning and dopant activation;
- annealing (N_2, 750°C) and TEOS deposition (800 nm);
- contact opening, metallization and sintering.

Some modifications to the above sequence were implemented as process splits, concerning: (i) the etching of the implant windows on the field oxide (dry vs. wet); (ii) additional, high-temperature (1000°C, dry O_2) annealing steps following the main p^+ and n^+ implantations; (iii) different stacking dielectrics for coupling capacitors (SiO_2-TEOS vs. SiO_2-Si_3N_4); (iv) different doses and energies for the implantations; (v) different starting materials (<111> vs. <100> substrates).

Fig. 1 shows a schematic cross section of the double-sided detector structure: as can be seen, the previously described process allows integrated coupling capacitors to be obtained having a recessed structure with a stacked-dielectric insulator (SiO_2-TEOS), aimed at providing both high specific capacitance and good yield /6/. It is also worth noting that a thick oxide (SiO_2-TEOS stacked layer) covers the p-stop regions; since in many detector designs a superposition of the metal pads with the p-stop can occur, this technological feature can be effective in reducing the risk of metal contacts to the p-stops.

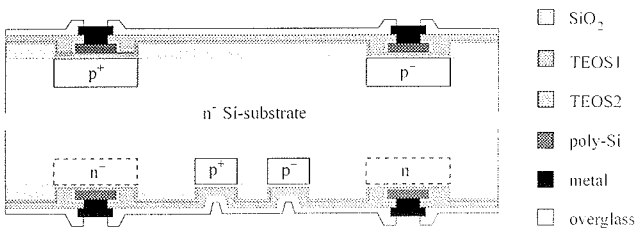

Fig. 1. Schematic cross section of a double-sided detector structure (not to scale).

2.2 Experimental results

The electrical characterization of the microstrip detectors was carried out with a semi-automatic test equipment by using standard procedures. The following measurements were performed on each detector: (i) total leakage current (bias-line & guard-ring); (ii) operating voltage and breakdown voltage; (iii) strip coupling capacitance and interstrip capacitance; (iv) strip (metal) series resistance. Finally, the so-called AC and DC scans were performed by using dedicated probe-cards and the total number of defects was evaluated on each detector. The AC scan consists of measuring the current on the AC pads, so as to check for shorts between adjacent metal lines and for the integrity of coupling capacitors; the DC scan allows to measure other key parameters of individual strips, including leakage current, poly-Si bias resistance and interstrip resistance. The criteria adopted for detector evaluation are representative of the electrical specifications for the detectors to be used in a real high-energy physics experiment and are described in detail in Ref. /5/.

The mean value and the standard deviation of the most relevant electrical parameters measured on the SB detectors from batches SD2 and SD3 are summarized in Table 1. The reported values are all within the considered specifications. A detailed description of the experimental results can be found in /7/. As an example, Fig. 2 shows the distribution of the effective strip bias resistance for all the tested SB detectors from batch SD3. The bias resistance value for most of the strips is included in the range from 6 to 8 MΩ, evidence of adequate process control.

Moreover, the defect rate was considerably reduced with respect to the first prototypes /4/. In fact, the total fraction of inefficient strips is in the order of a few %, with many detectors featuring values close to 1%. It is worth

noting that the incidence of strips with isolated, process-related defects is generally lower than 3 %, whereas the presence of a higher number of defects is to be attributed to accidental mechanical damage of the wafers. The detector quality could be further improved by reducing the number of defects due to lithographical problems, such as shorts between metal and implant lines, and interruptions of strips and p-stops, the latter representing now a significant fraction of the overall number of defects.

Table 1. Main electrical parameters measured on SB detectors.

Parameter	Unit	Mean value	Std. Dev.
Bias line leakage current	nA	165.1	38.1
Guard ring leakage current	nA	16.1	3.4
Breakdown voltage	V	189.0	31.1
Operating voltage	V	29.5	3.3
Coupling capacitance (p-side)	pF/cm	35.1	1.4
Coupling capacitance (n-side)	pF/cm	20.1	1.0
Interstrip capacitance (p-side)	pF/cm	1.13	0.03
Interstrip capacitance (n-side)	pF/cm	1.04	0.02
Poly-Si bias resistance	MΩ	6.7	1.2
Metal resistance	Ω/cm	32.0	1.2

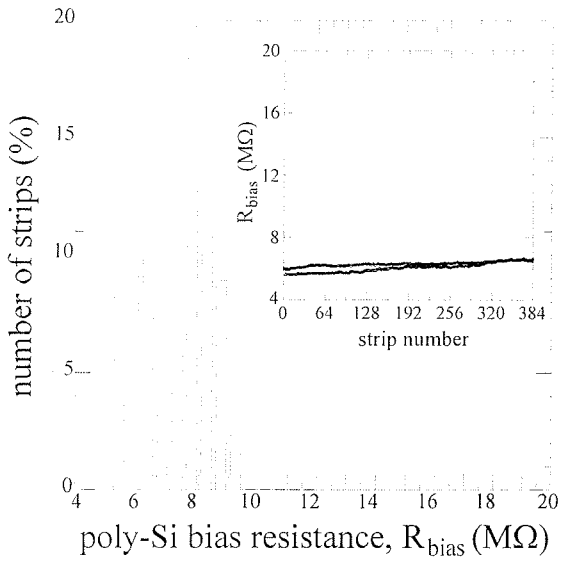

Fig. 2. Distribution of the strip bias resistance for SB detectors, with a typical scan in the inset.

The stability of the leakage currents was also tested at room temperature on a few detectors both on wafer and after dicing. For these measurements, detectors were kept reverse-biased at 80 V, i.e. well beyond the full depletion voltage, for 17 hours or longer. All of the tested detectors exhibited a very stable behavior. As an example, Fig. 3 shows the bias-line and the guard-ring current curves as a function of time for an SB detector after dicing: the variations of the leakage current in the last 2 hours of the measurement were about 0.12% and 0.9% for bias-line and guard-ring, respectively. Similar results were obtained for the other tested detectors, with maximum leakage current variations never exceeding 2.5% in the last 2 hours of the measure-ments. Moreover, no appreciable differences could be observed between undiced and diced detectors.

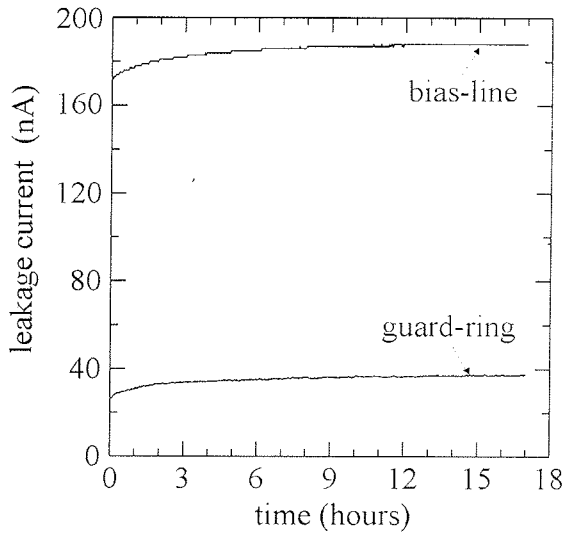

Fig. 3. Bias-line current and guard-ring current vs. time for SB detectors reverse biased at 80V.

3. ALICE microstrip detectors

Within the previously depicted framework, we have recently focused our attention to the development of double-sided, AC-coupled, microstrip detectors oriented to ALICE, an LHC experiment aimed at the study of heavy ion collisions. The Inner Tracking System of ALICE consists of six cylindrical layers of silicon detectors; in particular, the two outermost layers will be equipped with double-sided microstrip detectors /8/.

3.1 Detector design and fabrication

A dedicated wafer layout has been designed, containing the ALICE detector, two "baby" detectors (2.1 x 2.1 mm^2) suitable for beam telescope applications, and several test structures. The layout of the ALICE detector was designed according to the specifications outlined in the TDR /8/. The detector consists of 768 strips, tilted on both sides to obtain a stereoscopic angle of 35 mrad. The strip length (projection on the short edge of the detector) is 40 mm, whereas the strip pitch is 95 μm. As

for the strip width, two different values were adopted on both detector sides in order to evaluate the impact of this parameter on the detector performance. Narrow strips, 30μm and 35μm wide on the p-side and the n-side, respectively, are used in one half of the detector, whereas the other half features wider strips, 50μm and 49μm wide on the p-side and the n-side, respectively. The total detector area, including scribe-lines, is 75 x 42 mm^2.

Since radiation damage is not expected to be of major concern for ALICE, strips are biased by punch-through at both ends, thus avoiding extra processing steps associated to poly-Si resistors. An implanted guard-ring surrounds the bias-line. Strip isolation on the ohmic-side is obtained by means of individual box-shaped p-stops. In the narrow-strip half of the detectors, an additional individual p-stop implant is inserted inbetween the box-shaped p-stops.

Two batches of ALICE detectors were fabricated at IRST. A photograph of a processed wafer is shown in Fig. 4, with the large ALICE detector surrounded by the two telescope detectors and by several test structures. The fabrication technology is the same as outlined in Section 2, apart from the poly-Si related steps, which were not implemented. The only technological split is concerned with the coupling capacitors, which were based on either SiO_2-TEOS or SiO_2-Si_3N_4 stacked layers.

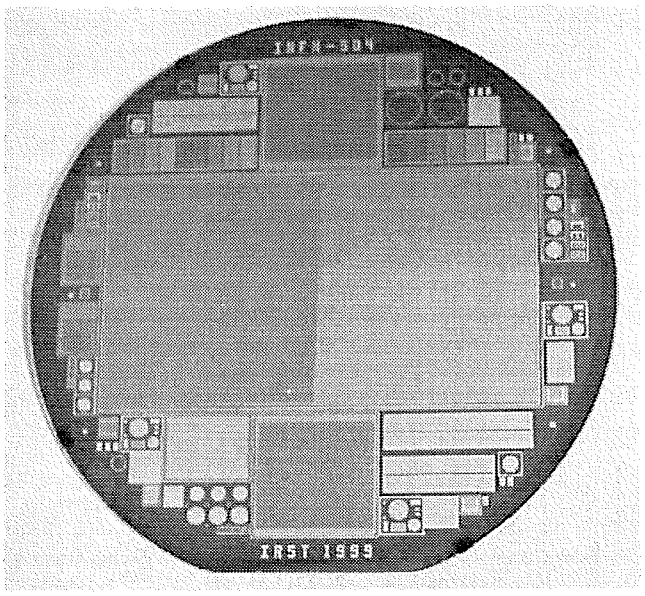

Fig. 4. Photograph of an ALICE microstrip detector wafer (p-side).

3.2 Experimental results

Preliminary measurements on test structures allowed to assess the good quality of the fabrication process. In particular, low leakage current values, in the order of 1nA/cm^2 at full depletion, were measured on 4-mm^2 test diodes with guard-ring: the corresponding values of bulk generation lifetime are about 30 ms. Diode breakdown voltage is generally higher than 200 V. The value of the surface generation velocity, extracted by means of gated diodes, is in the order of 24(3.5) cm/s on wafers employing TEOS(Si_3N_4) for coupling capacitors, corresponding to a surface leakage current density of about 40(6) nA/cm^2.

The electrical characterization of the detectors was carried out at INFN-Trieste. The total leakage current of the detectors (bias-line & guard-ring) were measured first, confirming the low values measured on test structures: in particular, the bias-line current was typically in the order of 500 nA at full depletion, whereas the guard-ring current was lower than 15 nA. The AC and DC scans were performed at an operating voltage of 40V by using dedicated probe-cards. The electrical specifications reported in /8/ were adopted as criteria for the detector evaluation.

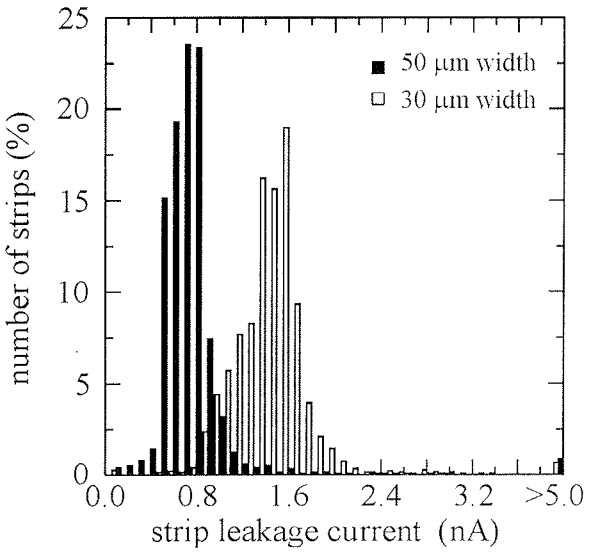

Fig. 5. Distribution of the strip leakage current for ALICE detectors.

Fig. 5 shows the distribution of the strip leakage current of all the tested detectors; two distinct groups of strips having different leakage current values can be observed, corresponding to the two different strip width values. As a matter of fact, due to a non negligible contribution from surface generation, strips featuring a lower width/pitch ratio are characterized by a higher leakage current /7/. The same difference between the two halves of the detectors in terms of leakage current can also be observed in Fig. 6, showing a typical scan of this parameter. However, the average value of the strip leakage current is well below 2 nA in both cases (see Table 2, referring to detectors featuring a SiO_2-Si_3N_4 stacked insulator for coupling capacitors), and only a small fraction of the strips, lower than 1%, exceeds the specification value (5 nA). The interstrip resistance and the equivalent resistance of the punch-through bias structure were also extracted from DC scans, the resulting values largely exceeding the minimum values required by the specifications.

Fig. 7 shows a typical scan of coupling capacitors: the current measured on good capacitors, biased at a voltage of 20 V across the dielectric, is lower than 100

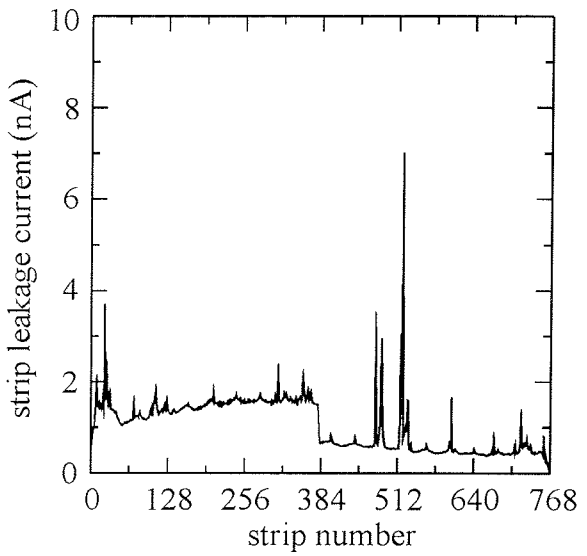

Fig. 6. Typical scan of the strip leakage current on the p-side of an ALICE detector.

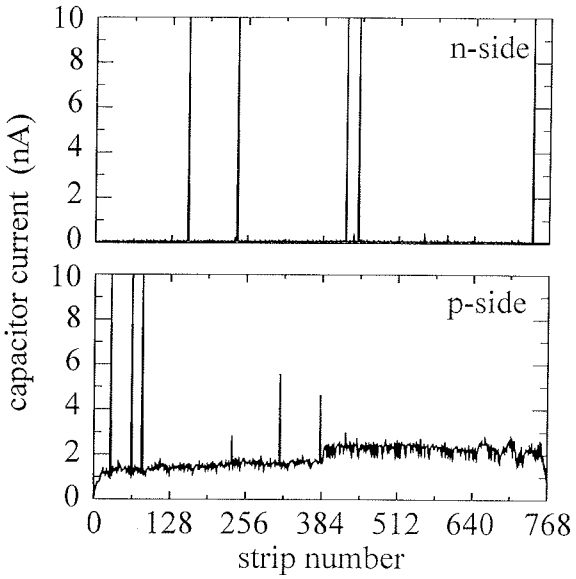

Fig. 7. Typical scan of the coupling capacitor current on the p-side and the n-side of an ALICE detector.

Table 2. Main electrical parameters measured on ALICE detectors.

Parameter	Unit	Narrow strips	Wide strips
Leakage current	nA	1.4	0.7
Coupling capacitance C_{AC} (p-side)	pF	171	286
Coupling capacitance C_{AC} (n-side)	pF	153	207
Parasitic capacitance C_p (p-side)	pF	5.7	7.8
Parasitic capacitance C_p (n-side)	pF	7.5	9.3
Ratio C_{AC}/C_p (p-side)		30	36.7
Ratio C_{AC}/C_p (n-side)		20.4	22.3

pA on the n-side, while it is ranging from about 1 nA to 2 nA on the p-side, accordingly with the strip width. Such a difference in the current values between the two sides of the detector is to be attributed only to measurement inaccuracies related to the use of probe-cards. The average fraction of bad capacitors, exhibiting current spikes reaching the upper value on the scale in Fig. 7, is below 1% on both detector sides, according to the quality of the fabrication process. The total fraction of inefficient strips in the tested detectors is lower than 3%, with an average value close to 1%.

Table 2 reports also the average values of the coupling capacitance and of the strip parasitic capacitance, the latter comprising both the interstrip and the back-plane contributions. As can be seen, both these parameters are higher in the case of wide strips; however, the ratio of the two capacitance values is higher than the specification value (20) in both cases. It is worth noting that the coupling capacitance on the p-side is much higher than on the n-side, due to the lower thickness of the thermal oxide on the p-side. Since the intrinsic breakdown voltage of the coupling capacitors is higher than 200V, a value which largely exceeds the one required by the specifications (100V), the oxide thickness on the n-side could be reduced in order to enhance the coupling capacitance. Further details on the experimental results are reported in /9/.

4. ATLAS pixel detectors

4.1 Device description

Pixel sensors were designed by the ATLAS Pixel Collaboration to be efficiently operated in very harsh radiation conditions /10/. These detectors are of the n-on-n type, i.e., n^+ pixels are obtained on the n-side of wafers, whereas a large p^+-n junction is present on the p-side, surrounded by a multiguard termination structure. With respect to the standard p-on-n pixel detectors, these devices require a more complicated, double-side fabrication technology; moreover, the pixels being of n-type, an adequate isolation between them is necessary, which is based on the moderated p-spray technique /11/. In addition to this, as suggested by recent studies on the radiation hardening of silicon, silicon substrates require to be oxygen enriched /12/.

Several batches of ATLAS pixel sensor prototypes have been processed at IRST starting from fall 1998 /13/. With respect to the formerly available microstrip detector process, featuring p-stop blocking implants in between n^+ strips on the detector ohmic side, the fabrication of ATLAS pixel sensor prototypes, requiring p-spray isolation, has imposed a different technological approach. Moreover, the pixel detector design was not fully compatible with IRST layout rules, particularly in the punch-through bias structures placed at one end of the pixels in order to allow for the sensor testing before bump-bonding /10/.

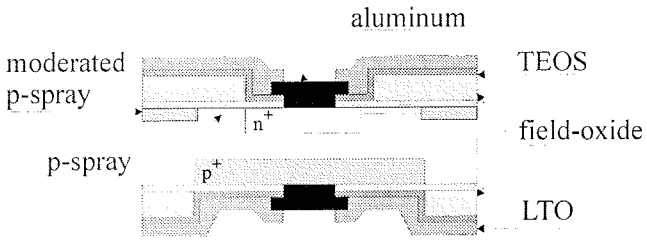

Fig. 8. Schematic cross section of an ATLAS pixel detector structure (not to scale).

Detectors were processed on 100 mm-diameter, FZ, 250-μm-thick, <111>-oriented, n-type silicon wafers, with nominal resistivity of 5 kΩ· cm. At the beginning of the processing sequence, half of the wafers has undergone a preliminary thermal treatment, consisting of a 24 hour oxidation-diffusion process at 1150°C /12/, in order to enrich the oxygen content up to a concentration of about 10^{17} cm^{-3} for radiation hardness purposes. With reference to the schematic cross-section of a single pixel, shown in Fig. 8, the fabrication process can be outlined as follows:

- screen oxide growth (wetO_2, 200 nm); n-side: p-spray implantation (B, 4.5×10^{12} cm^{-2}, 70 keV), moderated p-spray definition and implantation (B, 4.5×10^{12} cm^{-2}, 70 keV);
- TEOS deposition (800 nm); p-side: p^+ diode definition, TEOS dry etching, screen oxide growth (dryO_2, 40 nm), p^+ implantation (B, 5×10^{14} cm^{-2}, 70 keV);
- n-side: n^+ pixel definition, TEOS dry etching, reoxidation (p^+ drive-in), n^+ implantation (P, 5×10^{15} cm^{-2}, 120 keV), reoxidation (n^+ drive-in);
- TEOS deposition (300 nm), segregation annealing (N_2, 6 hours, 750°C), contact definition and opening;
- metal deposition, definition and dry etching; LPCVD-Low Temperature Oxide (LTO) deposition, passivation layer definition and dry etching; contact sintering in forming gas.

4.2 Experimental results

In the following, experimental results will be reported which refer to the second pixel prototypes. The wafer layout for these devices (see photograph in Fig. 9) contains: (i) 3 large sensors (16 cm^2), called tiles, differing in the design and dimensions of the punch-though biasing structures (in the following they will be referred to as SMD, LAD and NOD); (ii) 12 smaller sensors (1 cm^2), called single-chips; (iii) several test structures, including diodes with guard-ring, gated diodes and MOS capacitors.

Preliminary measurements were carried out at IRST to assess the process quality before delivering wafers to the interested groups of the ATLAS Collaboration. Test structures were measured first; all the technological parameters evaluated from the characterization of these devices indicated that the fabrication process is adequate for good quality detectors. Moreover, only minor differences could be observed between oxygenated and standard wafers in terms of both bulk and surface properties.

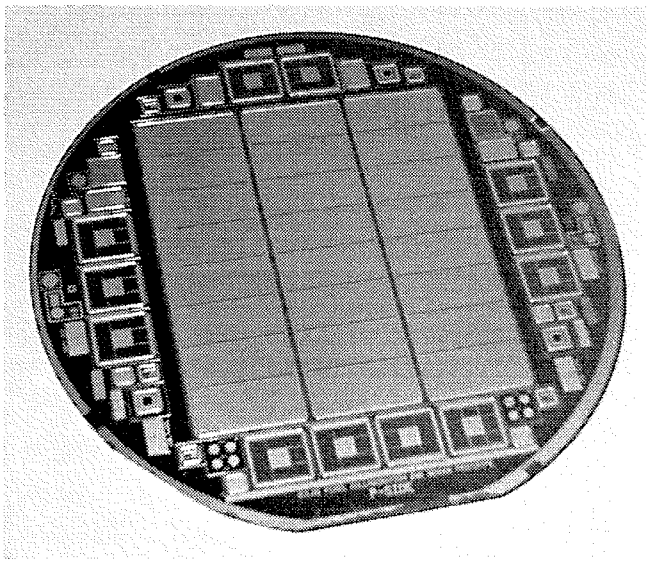

Fig. 9. Photograph of an ATLAS pixel detector wafer (p-side).

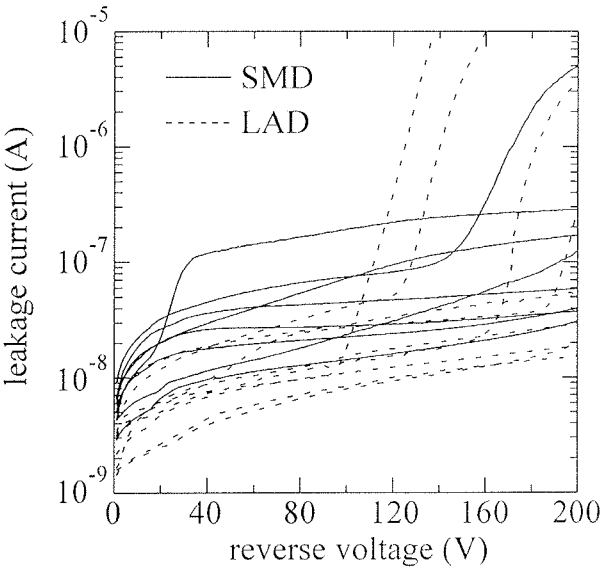

Fig. 10. Typical leakage current curves of SMD and LAD single chips.

The I-V curves of all the single-chips and tiles were then measured using the single-side set-up described in /14/. As an example, Fig. 10 shows some typical leakage current curves for SMD and LAD single-chips: the leakage current values at 150V are normally ranging from 10 to 100 nA. In spite of the non saturating behaviour of the curves, due to a non negligible surface current contribution from the n-side interpixel regions, these leakage current values would comply with the technical specifications of the ATLAS pixel prototype sensors /11/. Fig. 11 shows the breakdown voltage distribution, defined as the voltage at which the measured current exceed 1 μA, for all the single-chips. As can be seen, while the distribution for SMD and LAD detectors is similar, with a low number of early failures

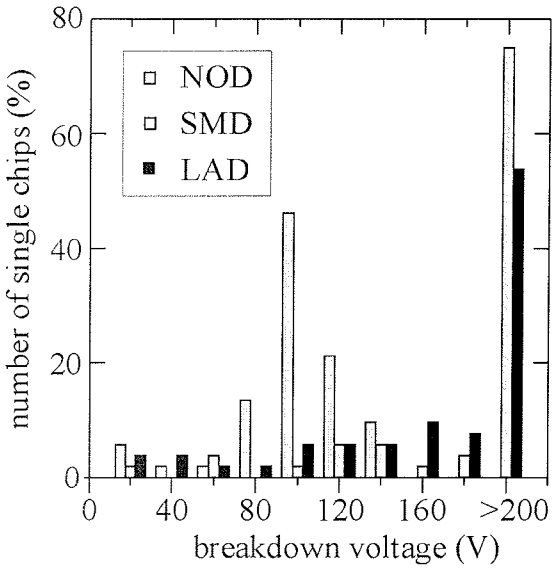

Fig. 11. Distribution of the breakdown voltage of the three types of single-chips.

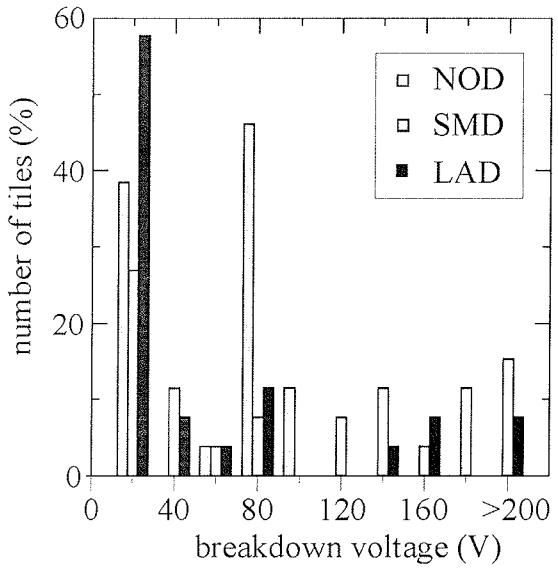

Fig. 12. Distribution of the breakdown voltage of the three types of tiles.

and with most of the chips featuring a breakdown voltage higher than 200V, NOD detectors exhibit a distribution peaked at about 100 V, with no detector reaching 150 V. The weakness of NOD detectors, which was also reported by other manufacturers, although not fully understood, is probably to be attributed to a layout problem.

Fig. 12 shows the breakdown voltage distribution, defined as the voltage at which the measured current exceed 10μA, for all the tiles. As expected from single-chip results, no tile of the NOD type exceeds 100 V of breakdown voltage. On the contrary, the behaviour of SMD and LAD detectors is generally worse than that of the corresponding single-chips, with many detectors suffering early breakdown problems as the full depletion voltage is reached and only a few tiles exhibiting a breakdown voltage higher than 150 V. The reason for this considerable degradation in the characteristics of tiles with respect to the corresponding single-chips is not easy to understand, although it is likely to be attributed to the presence of defects on the n-side of the wafers. On one hand, on a statistical basis, the number of defects encountered on 1-cm^2 single-chips can justify the low yield on 16-cm^2 tiles; on the other hand, these defects could not be observed by means of optical inspection of the wafers and, moreover, the measurement of the total leakage current alone does not allow to identify the type of defects and their position. Light emission microscopy measure-ments are currently being carried out in order to gain deeper insight into the cause of early breakdown events.

5. Conclusions

We have reported on the most recent results from an R&D program on radiation detector technologies at IRST Laboratory. In particular, a fabrication process for double-sided, AC-coupled microstrip detectors has been developed and several batches of good quality detectors with a low defect rate have been manufactured. Within this framework, ALICE detector prototypes have been fabricated and succesfully tested. Moreover, a few spares for the layer 1 and 2 detectors for the Silicon Vertex Detector of the Babar experiment are currently being fabricated.

More recently, IRST has also been committed to the fabrication of ATLAS pixel detector prototypes. Results from the electrical characterization of detectors and related test structures have evidenced that, in spite of the lack of specific experience in the p-spray isolation technique, IRST technology is potentially adequate for the fabrication of these detectors. Nevertheless, the number of process-related defects should be decreased in order to fulfill the detector specifications (in particular in terms of breakdown voltage) with a satisfactory fabrication yield.

Acknowledgements

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References

/1/ Lindström et al., "Radiation hardness of silicon detectors - A challenge from high energy physics", Nuclear Inst. and Meth. in Phys. Res., vol. A426, pp. 1-15, 1999.

/2/ R. H. Richter and G. Lutz, "Silicon radiation detectors - Physics and structures", Informacije MIDEM, vol. 29, nr. 1, pp. 1-9, 1999.

/3/ M. Boscardin et al., "First results on double-sided AC-coupled Si strip detectors", Proc. of MIDEM Conference, pp. 205-210, Rogaska Slatina (Slovenia), 1998.

/4/ G. F. Dalla Betta et al., "Feasibility study for double-sided silicon microstrip detector fabrication at IRST", Nuclear Inst. and Meth. in Phys. Res., vol. A431, pp. 83-91, 1999.

/5/ D. Barbieri et al., "Silicon sensors for the BaBar vertex tracker: design, electrical tests and production quality control", Il Nuovo Cimento A 112, pp. 113-130, 1999.

/6/ G. F. Dalla Betta et al., "A comparative evaluation of integrated capacitors for AC-coupled microstrip detectors", Nucl. Instr. and Meth. A, vol. A411, pp. 369-375, 1998.

/7/ G. F. Dalla Betta et al., "Development of a fabrication technology for double-sided AC-coupled silicon microstrip detectors", to appear in the Nucl. Instr. and Meth. A.

/8/ ALICE Technical Design Report of the Inner Tracking System (ITS), CERN/LHCC 99-12, ALICE TDR4, 18 June 1999.

/9/ M. Boscardin et al., "Development of ALICE microstrip detectors at IRST", presented at Frontier Detectors for Frontier Physics - 8th Pisa Meeting on Advanced Detectors, La Biodola (Italy), May 2000, to appear in the Nucl. Instr. and Meth. A.

/10/ T. Rohe et al., "Sensor design for the ATLAS-Pixel detector", Nucl. Instr. and Meth. in Phys. Res., A421, pp. 224-228, 1998.

/11/ The ATLAS Pixel Sensor Group, "Technical specifications of the ATLAS pixel prototype sensors", 16 February 1999.

/12/ G. Casse et al., "Introduction of high oxygen concentrations into silicon wafers by high temperature diffusion", Nucl. Instr. and Meth. in Phys. Res., A438, pp. 429-432, 1999.

/13/ M. Boscardin et al., "Fabrication of ATLAS pixel detector prototypes at IRST", presented at the International Workshop on Semiconductor Pixel Detectors for Particles and X-rays, Genova (Italy), June 2000, and submitted for publication in the Nucl. Instr. and Meth. A.

/14/ F. Hügging et al., "Design and test of pixel sensors for operation in severe radiation environments", Nucl. Instr. and Meth. in Phys. Res., A439, pp. 529-535, 2000.

G. U. Pignatel
Dipartimento di Ingegneria dei Materiali,
Universita di Trento,
Via Mesiano 77, 38050 Trento, Italy
M. Boscardin, G.-F. Dalla Betta
IRST, Divisione Microsistemi,
Povo, I-38050 Trento, Italy

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