SYSTEM DESIGN CONSIDERATIONS FOR LOW-POWER, BP Δ–Σ A/D CONVERTER USED FOR COHERENT DETECTION SYSTEMS

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Key words: BP Delta-Sigma A-D converters, BandPass Delta-Sigma A-D converters, coherent detection, power optimization, decimators, decimation filters, BW, Bandwidth, adders, running sum architecture

Abstract: Design considerations for low-power coherent detection system using BP Δ–Σ A/D converter are presented. Some optimization steps for reducing power consumption are explained together with some system and circuit level simulation results. A 6^{th} order modulator design and corresponding 4^{th} order running-sum decimator are presented. Suggestions are made for further reduction of power consumption, which is estimated to be less than 500μW for 6^{th} order modulator with S-C loop filter implementation, oversampling ratio D=256, S/N=110dB at f_{ovs}=64kHz and bandwidth BW=260Hz.

Zasnova sistema za koherentno detekcijo z uporabo BP Δ–Σ A/D pretvornika z nizko porabo moči

Ključne besede: BP Delta-Sigma A-D pretvorniki pasovno propustni analogno-digitalni, detekcija koherentna, optimizacija moči, decimatorji, filtri decimacijski, BW širina pasovna, seštevalniki, arhitektura s seštevalniki

Izvleček: V članku je opisan postopek načrtovanja sistema za koherentno detekcijo z uporabo BP Δ–Σ A/D pretvornika na sistemskem nivoju. Predstavljeni so nekateri optimizacijski postopki na visokem hierarhičnem nivoju s pomočjo katerih lahko zmanjšamo porabo moči takega sistema ter rezultati nekaterih simulacij. Zasnovi BP Δ–Σ modulatorja šestega reda in pripadajočega decimatorja četrtega reda sta izbrani glede na postavljene zahteve in ostale pripadajoče kriterije. Podani so predlogi za zmanjšanje porabljene moči. Ocenjena poraba moči je približno 500μW za eno bitni modulator s filtrom šestega reda implementiranim s tehniko S-C, razmerjem vzorčevalne frekvence proti mejni D=256, razmerjem S/N=110dB pri vzorčevalni frekvenci f_{ovs}=64kHz in pasovno širino BW=260Hz.

1. Introduction

With down-scaling of integrated circuit technology in recent years analog signal processing circuits are more and more replaced by digital signal processing circuits because of several advantages: flexibility, programmability reliability, noise immunity, reduced power consumption, easier and more reliable design and test if automated procedures are used. The key operations in such systems are A/D conversion and for narrow band signals appropriate subsampling of correctly band-limited spectrum. In our case, simple coherent detection circuit and BP Δ–Σ modulator followed by simple and efficient digital decimation filters are used to transfer input double side band signal with suppressed carrier and limited bandwidth to a digital stream of data, which can be further processed by appropriate DSP algorithm. The technique has several advantages compared to traditional analog implementation: lower power consumption, easier integration and because of that higher reliability, better flexibility etc. It is essential to reduce power consumption as much as possible. The only way to do that is to perform optimization on each hierarchical level from the system to the layout.

We are trying to design a coherent detection system with as small power consumption as possible. The signal that must be down-sampled is double side band signal with suppressed carrier and with the bandwidth BW≤260Hz centered at 16kHz. The purpose of the system is to perform coherent detection of a low-frequency signal that causes modulation of the carrier, bring it down to the base-band and convert it to the digital domain using high resolution A/D converter with S/N>110dB. As usual this can be done in many different ways and it seems that most promising approach regarding silicon area and power consumption is BP Δ–Σ A/D converter and coherent detection.

In section II principles of coherent detection using BP Δ–Σ A/D converter are shortly explained and some system level simulation results are presented. Design steps for 6^{th} order BP Δ–Σ modulator are shortly presented in section III with some key parameters regarding architecture, stability, speed, power consumption. Section IV deals with possible realisation of the decimator. Section V summarises simulation results and presents the conclusions.

2. System for coherent detection

Block diagram of possible system for coherent detection of narrow-band signals is presented on figure 1.

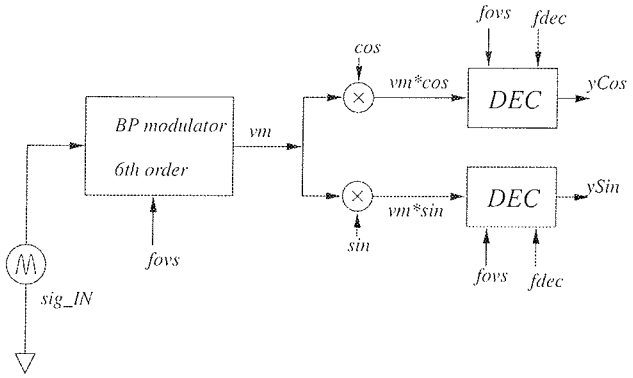

Fig. 1: Coherent detection system

BP modulator can be implemented with continuous time or S-C loop filter. Using S-C realisation makes A/D conversion more accurate and less sensitive to the process parameters and temperature variations compared to continuous time implementation, but requires additional filtering (anti-aliasing filter) to prevent folding of unwanted components to the base-band of the BP modulator. The continuous time gm-c loop filter reduces power consumption even further because it does not require anti-aliasing filter since all out-of-band components are attenuated efficiently by its loop filter. In addition the speed of the transconductance element needs to be smaller compared to the operational amplifier used in S-C implementation. Unfortunately CT approach it is less stable and less accurate. In this article S-C implementation is proposed for the reasons of accuracy. Sampling frequency of the BP modulator is selected as low as possible: $f_{ovs}=4f_{osc}$, thus a very simple method of coherent detection is available: multiplication of a bit-stream with coherent sine wave. It can be easily accomplished before the decimation filtering using frequency $f_{Cos}=f_{ovs}/4$ realised as another bit-stream with values taken from table 1 /4/. Coherent detection with defined relation among signal frequencies is reduced to the generation of simple streams of +1, 0 and -1 and 1 bit multiplication between bit-stream and Sin or Cos signal. Multiplying v_m by Cos or Sin signals is followed by filtering and down sampling. Some additional digital signal processing not described in this article gives further information about frequency and phase of demodulated signal: $x=v_mCos$ and $y=v_mSin$.

***Table 1:** Sin and Cos signal generation*

K	Cos	Sin
0	1	0
1	0	1
2	-1	0
3	0	-1
4	1	0

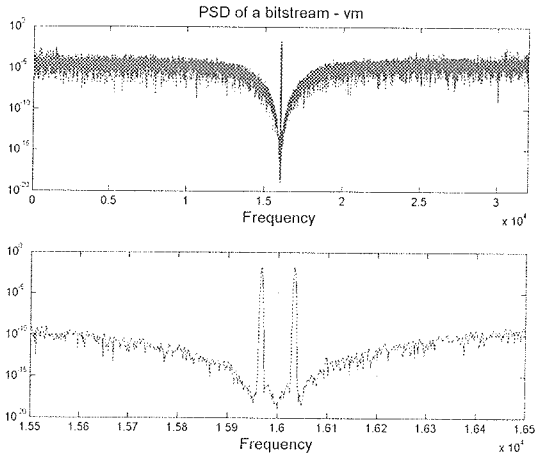

Fig. 2: Spectrum of a bit-stream v_m

The spectrum of a bit-stream v_m after BP $\Delta-\Sigma$ A/D converter is very rich and shown on figure 2 for the case of 2 spectral components of equal power with frequencies $f_{ovs}/4-f_x$ and $f_{ovs}/4+f_x$ (see detail on figure 2). Frequency f_x is a frequency of modulation signal that carries the information. The whole spectrum is composed of 2 spectral components in the band of interest, quantisation noise, thermal and 1/f noise and aliased crosstalk, which is much smaller than any other component if designed properly. Ideally the Cos or Sin signals are sine waves with only one spectral component with frequency f_x. Let us discuss the process of multiplication with our coherent signals. One can imagine that every spectral component in the v_m is multiplied by a sine wave with frequency $f_s/4$, which is in fact a stream of +1, 0 and -1. The band below $f_s/4$ is by multiplication reversed and placed to the same band and also translated to the band between $f_s/4$ and $f_s/2$. The band above $f_s/4$ is transferred between 0 and $f_s/4$ and $f_s/2$ and $3f_s/4$ and aliased back to the band $f_s/2$ to $f_s/4$. The spectrum after multiplication is shown on figure 3. 1/f noise and offset components are transferred around frequency f_s and are later attenuated by decimation filter. The noise power after multiplication with a coherent sine-wave is composed of all noise sources from the band below and above f_{osc} and are included in the simulation results presented on figure 3 /1/. The upper portion of the spectrum can not be seen because of the logarithmic scale. Similar spectrum exists for v_mSin. Frequency components above 125Hz must be attenuated using appropriate decimation filter.

Possible realisation of the decimation filter is $sinc^4$ characteristics with accumulate and dump architecture. Transfer function is presented on figure 5. A 4^{th} order is used because in that case the slope of the decimation filter is bigger than the slope of quantisation noise produced by 6^{th} order BP modulator. Short description of the implementation of the decimation filter is given in section IV. The spectrum y_{Cos} after $sinc^4$ decimator, down-sampled to $f_{dec}=f_{ovs}/R=250Hz$, with modulation frequency f_x=33Hz is presented on figure 4. Similar spectrum with different phase is obtained on the output y_{Sin}. Further digital signal processing of both signals can extract all necessary infor-

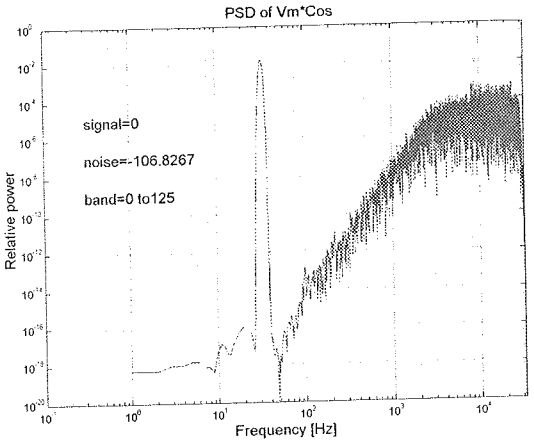

Fig. 3: Spectrum of v_mCos for f_x =33Hz

mation about frequency and phase of the rotation. Since all signals are very low frequency, serial digital signal processing can be used to save silicon area.

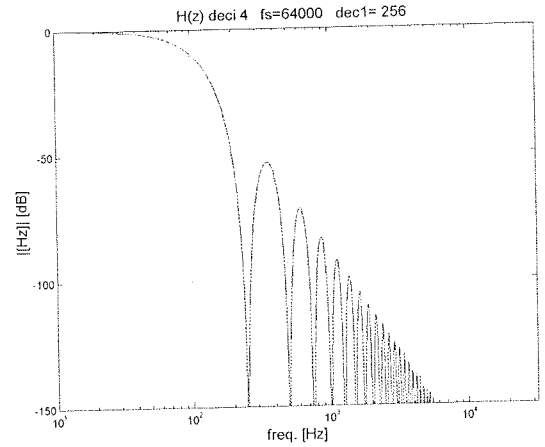

Fig. 4: Decimator frequency characteristics

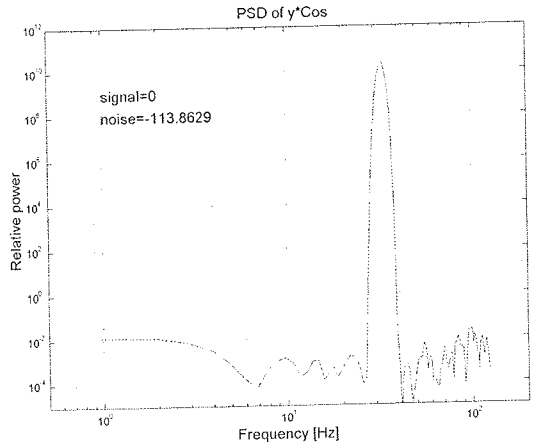

Fig. 5: Down-sampled spectrum of the rotation signal after decimator

3. 6th order modulator

A 6th order 1 bit BP modulator with oversampling ratio R=256 can fulfil the requirements: $S/N \geq$ 110dB in a band of 125Hz. Figure 6 plots possible noise transfer function with poles and zeroes defined in table 2 and on figure 7. Signal transfer function (STF) depends on realisation, stability constraints, area and power consumption and will be presented in near future with special emphasise on power consumption optimisation and stability constraints. For S-C implementation the jitter does not present a problem, so normal comparator is used for one-bit A/D, while 1 bit D/A is implemented by non-return-to-zero S-C stage charged to the reference voltage and controlled by the outcome of the A/D conversion process or in other words by the bit-stream. The positions of poles and zeros are for the time being selected according to the Lee's rule of thumb /5/, which requires that the $|NTF(e^{j\omega})|<2$ for the whole band of interest. Since this condition is pessimistic and does not give insight into the real stability of the modulator it will be refined in the design and simulation steps that still needs to be implemented.

***Table 2:** Poles/Zeros of possible Noise Transfer Function*

Poles	Zeros
-0.2151\pm j0.8333	-0.0048\pm j1.0000
+0.0000\pm j0.7499	+0.0000\pm j1.0000
+0.2151\pm j0.8333	+0.0048\pm j1.0000

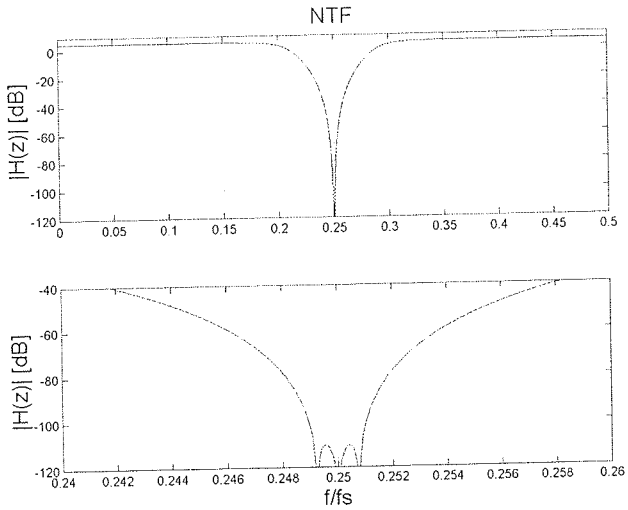

Fig. 6: Noise transfer function (NTF)

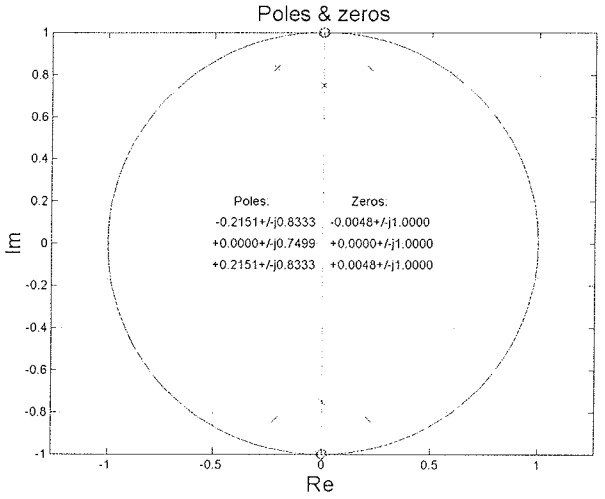

Fig. 7: Poles and zeros of noise transfer function (NTF)

4. Decimator

There are many possible realisations of the decimation filters. Efficient solution in terms of area and complexity is *sinc* decimator /3/, which does not need any multiplication and the only arithmetic operation needed is 2's complement addition. Here $sinc^4$ (figure 8) is implemented because we have 6th order BP modulator with transfer function presented on figure 4. The slope of the frequency characteristics of the integrators before down sampling is bigger than the slope of the quantisation noise and thus guaranties enough attenuation of high frequency quantisation noise as well as other noise contributions. Very simple programmable accumulate-and-dump architecture has been implemented, so the oversampling ratio can be easily changed by simply taking every R^{th} sample from the IIR part and processed it by FIR low-frequency section of the decimator. Number of bits needed for correct operation is:

$$n_{bits} = \frac{\log_{10}\left(R^M r_i\right)}{\log_{10}(2)} = 32bits$$

Where R is decimation ratio, M is decimator order, $r_I = 1$ is number of bits at the input and n_{bits} is number of bits needed for internal registers of the decimator, so that the overflow is correctly processed. IIR and FIR parts can be processed serially since the sampling frequency is rather low. Programming of the decimator is possible by changing the oversampling ratio from *R=2 to 256* and taking different bits from the last register of IIR to the first register of FIR every R^{th} oversampling clock cycles. Figure 5 is the result of processing the signal v_m*Cmos* with real $sinc^4$ decimator. If attenuation at 125Hz is not acceptable this can easily be corrected by simple digital all-pass filter following the decimator. The decimator realised in 0.6μm CMOS technology with f_{ovs}=64kHz consume approximately 20μA average current and the rest (80μA) are reserved for the modulator.

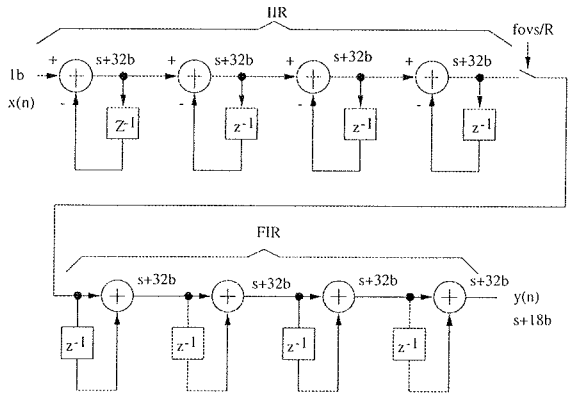

Fig. 8: Block diagram of sinc^4 *decimator*

5. Conclusions

A system design considerations and some important steps for the power consumption optimisation of a coherent detection system using 6^{th} order BP modulator and 4^{th} order $sinc^4$ that can be used for mixed-signal processing of a narrow band double-side band signals with suppressed carrier are presented in the article. Possible architecture is evaluated and some system and circuit level simulations were performed to show the usefulness of the approach. Architecture of the BP modulator and decimator has been defined and important system level simulation results have been presented. The realisation of proposed architecture is feasible, so circuit design of a BP modulator will follow using S-C and gm-c implementation of the loop filter with big attention to the power consumption optimisation and stability constraints.

References

/1/ Strle D., "Capacitor area and power-consumption optimisation of high order modulators", Informacije MIDEM, 31(1), 129-135, 2001.

/2/ Reese G.M., Marek E.L., Lobitz D.W., "Three dimensional finite element calculations of an experimental quartz rotation sensor", Proceedings of Ultrasonic symposium, 419-422, Oct. 1989.

/3/ Norsworthy S.R., Schreier R., Temes G.C., "Delta-Sigma Data Converters,", IEEE press, 1997.

/4/ Jurgen A.E.P van Engelen, R.J. van de Plassche, E.Stikvoort, A.G. Venes, "A sixth-order continuous-time bp sigma-delta modulator for digital radio if", IEEE JSSC 39(I"), 1753-1764, Dec. 1999.

/5/ K.C.H. Chao, S. Nadeen, W.L.Lee, C.G. Sodini " A Higher Order Topology for Interpolative Modulators for Oversampling A/D Converters," IEEE Trans on CAS, vol. 37, no. 3, pp 309-318, March 1990.

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