FLIP CHIP, CSP AND WLP TECHNOLOGIES: A RELIABILITY PERSPECTIVE

Horatio Quinones and Alec Babiarz

Asymtek Headquarters, Carlsbad CA, USA

INVITED PAPER
MIDEM 2002 CONFERENCE
09.10.02 - 11.10.02, Hotel Klub, Lipica

Key words: packaging, bonding, interconnect, assembly, flip chip, chipscale package

Abstract: Several factors have caused wire bonding to remain the predominant first level interconnect solution across a wide range of systems, from low-end consumer applications to high-end computing systems. Early on, system performance demands were such that the electrical and thermal limitations of wire bonding interconnect did not prove restrictive. Spurred on by US OEM investments in large-scale assembly houses in low cost Far Eastern countries, the wafer and assembly processing equipment industry developed rapidly for wire bonding and soon established a global presence. On the other hand, IBM had invested significant resources in capturing an early lead and maintaining an exclusive hold on the intellectual property rights to several key steps in the design and fabrication processes for flip chip (FC) silicon die and associated packaging. The process required critical control in sputter deposition of the multiple terminal metals to create the C4 bump for FC. Equally important were the design methodologies for FC and the technology of FC packaging materials. The mismatch in thermal expansion between silicon and polymer based substrate materials led to ceramic as the preferred choice of substrate material. Starting in the late sixties. The widespread use of FC technology in IBM systems naturally assured a performance edge over competitive offerings using wire-bonding right through the seventies and early eighties. However, the premier large Japanese OEM's, namely Hitachi, Fujitsu and NEC began narrowing USA C4 lead during the eighties, thanks to their own versions of comparable flip chip interconnect and multichip packaging. Nonetheless, application of FC or flip chip solder interconnect remained solely within the domain of leading mid-range and main-frame systems where I/O density, stringent reliability, electrical switching noise and thermal dissipation needs of bipolar based systems were the critical drivers. Other areas of flip chip application included automotive, and, in commodity products like high volume watches, using for example, thermocompression bonding on a polyimide carrier, driven primarily by size constraints, cost and the absence of reliability constraints. Reliability challenges for the FC technology, i.e., harsher environments, smaller geometries, higher performance, are rising constantly. Numerous developments have been implemented since the early days of FC. Underfilling or encapsulation of the FC has been perhaps the single most significant improvement. The implementation of this technology made Flip Chip on Board (FCOB), a reality. Organic packages with FC are very common in the market today. This talk paper surveys the history of FC from its early days and includes emerging technologies derived from the FC, including CSP, WLP. We will also address jet technology as way of underfilling FC and CSP packages.

Pogled na tehnologije FLIP CHIP, CSP in WLP s stališča zanesljivosti

Ključne besede: montaža, bondiranje, povezovanje, zapiranje, tehnologije zapiranja flip chip in chip scale

Izvleček: Bondiranje je še vedno prevladujoča tehnologija povezovanja na prvem nivoju v mnogih elektronskih sistemih, od cenenih širokopotrošnih do zapletenih računalniških. V preteklosti se je namreč izkazalo, da električne in termične omejitve bondiranja niso omejevale funkcionalnosti na nivoju sistema. Velike investicije ameriških firm v montažne kapacitete na Daljnem Vzhodu so povzročile hiter rast in razvoj industrije naprav za povezovanje, ki je kmalu tudi sama prerasla v globalno industrijo. Na drugi strani pa je firma IBM vložila ogromna sredstva v razvoj ključnih korakov tehnologije, ki omogoča FC (Flip Chip) tehniko montaže silicijeve tabletke na substrat. Med drugim je bilo potrebno razviti nekatere kritične korake nanosa različnih kovinskih plasti, ki so omogočale izdelavo kroglic za FC. Enako pomembne so bile metodologije načrtovanja za FC in tehnologije materialov za FC način zapiranja. Neujemanja temperaturnih koeficientov med silicijem in polimernimi materiali je privedla k uporabi keramičnih materialov za FC substrat v poznih šestdesetih. V sedemdesetih in osemdesetih letih je široka uporaba FC tehnologije znotraj firme IBM seveda omogočila ustrezno tehnološko in konkurenčno prednost pred ponudbami njenih konkurentov, ki so temeljile na tehnologijah klasičnega bondiranja. Šele koncem osemdesetih let je nekaterim vodilnim japonskim velikanom, kot so NEC, Fujitsu in Hitachi, uspelo zmanjšati ta tehnološki zaostanek, ko so razvili lastne tehnologije FC povezav in multichip ohišij. Kakorkoli, tudi nadalje je uporaba FC tehnologije bila omejena le na srednje velike in velike računalniške sisteme, kjer so gostota vhodov/izhodov (I/O), zahteve po zanesljivosti, majhen električni preklopni šum in visoke zahteve po termični stabilnosti teh v glavnem bipolarnih sistemov zahtevale tak pristop. Uporaba FC tehnologije se je prijela tudi na drugih področjih elektronike, kot so avtomobilska industrija ter proizvodnja ur, kjer so majhnost sistema in nizka cena, manj zanesljivost, bile glavne gonilne sile. Zanesljivostni izzivi za FC tehnologijo so vse večji, kot so denimo delovanje v težkih razmerah okolja, vse manjše geometrije in vse boljše karakteristike. Prvim razvojnim korakom FC tehnologije so sledile številne izboljšave. Ena od najpomembnejših izboljšav je sigurno bila upeljava tehnike zalivanja tabletke s spodnje strani. Ta korak je pravzaprav omogočil montažo FC ohišja na substrat - FCOB (Flip Chip On Board). FC tehnike zapiranja na organski osnovi so dandanes zelo prisotne na trgu. V tem prispevku podajamo zgodovinski oris razvoja FC tehnologije od njenega nastanka do opisa nekaterih novih tehnologij, ki so se razvile iz nje, kot so CSP in WLP. Opisali bomo tudi tehnologijo brizga kot možnost zalivanja FC in CSP ohišij.

Introduction

Upon the introduction of transistors into the electronic packaging, and circuit integration on portable products, minituarization of integrated circuits became a necessity. Along with this microelectronic packages came an even more important demand perhaps, namely the performance and reliability of such products. The inconsistent, and often defect from manual wire-by-wire bonding no longer could support mass production. A faster bonding process was necessary, a method where simultaneously interconnects could be manufactured. A natural solution such as the FC process was implemented on Solid Logic Technology (SLT). The idea of having the active devices facing the interconnection, i.e., the flipping of the die was very novel idea. Protection of these devices became a major subject, and the discipline of ball limiting metallurgy (BLM), commonly referred these days as the under-bump-metallurgy (UBM) emerged. Problems of electrical shortage solder running on the surface metal line conducting media. Implementation of stiff interconnections was utilized to overcome this problem, but as technology evolved, geometries became larger wearout mechanisms became an issue in the form of low cycle fatigue. FC technology needed a solution, and once more, the soft solder interconnection was used, only this time it was attached to what we refer to day as "thin film" on a thick ceramic substrate (die carrier). Co-fired metallurgy and the thick ceramic carrier made up a package FC land that prevented solder running. In the last few years the concept of die circuit redistribution has been popular in the industry. This redistribution is done either to convert wire-bonded designs that consist die and large, peripheral arrays to fully populated array, or simply to allow usage of most area of the die for high-density interconnection (HDI). Although this package type has been used extensively for several years without been considered other than a subset of FC, nowadays is denominated as Wafer Level Package (WLP). WLP may be sometimes being referred as a Chip Scale Package (CSP). All these variations are indeed, based on the FC technology concept. In fact, very often the geometry aspect ratio is kept unaltered.

Wirebonded Packages

History

Wirebonding is the most common die connection technology today in the microelectronic industry and the most common wirebonded assembly in organic packages. The die is mounted backside down with epoxies and metals onto the substrate. Wires are bonded on one at a time, in one of mainly three processes: Ultrasonic bonding (UB), thermocompression bonding (TCB) and thermosonic bonding (TSB). Wirebonding was the first technique to be applied for assembly of devices. As early as 1957, Bell Labs in New Jersey (USA) use the technique and it was referred as Thermocompression Bonding, the other types of Wirebonding were introduced soon after when lower temperatures were required by some thermally sensitive devices. These bonders were manually operated and very labor intensive. Gold silicon eutectic between the die and the die carrier was used to attach the die prior to wire bonding. Gold and aluminum wires were the only choice. Wire bonds yields have improved and so also has their reliability. Most reliability detractors for the wirebonding technology are manufacturing defect related. Refined manufacturing practices have increased the reliability performance of this technology. Die bond, whether is metal solder, epoxy, or glass can fail during thermal cycling.

Reliability Issues in Wirebonding

Perhaps, the most widely known reliability problem for wirebond involves the *Au-Al* interface. The formation of the intermetalic $Au\text{-}Al_2$ (purple plague) during the Au material bonded to Al metallization. Although, this compound may be inconsequential to the wirebond reliability, its presence may indicate the bond integrity has been otherwise degraded already. The embrittlement of these wires make them more vulnerable to induced fracture when TC and mechanical loading. Another concern is the diffusion that occurs at higher temperatures. The Al diffuses into the *Al*-rich $AuAl_2$ phase, leaving behind Kirkendahl voids that arise from the different interdiffusion kinetics. When this voided coalesce, an electrical open may occur. Minimizing the time spent at high temperatures, improves the reliability of these packages significantly. Gold plating impurities, in particular thallium form low temperature melting eutectics that will weaken grain boundaries in the thermocompression ball bonding. For cases where injection molding is used to encapsulate the package, wire sweeping is a mayor defect producer. Significant improvements have been made with wirebond rates by the implementation of automated bonders. Improvement on the purity of materials used in the wirebonding technology to accommodate changes in the die passivation and termination, bump metallurgy is extending and widening the use of it. The use of aluminum ball bonding to improve bonding rates and the use of copper wires to bond to copper thin and thick films is gaining acceptance in today's packages. Wirebonding sweeping occurring from fluid and gas flow as in the case of injection molding or convection cooling has been identified as a major problem. Thin wires are especially susceptible to such manufacturing processes and to regular machine operation.

Flip Chip Interconnection

History

Early in the 1960's the solder bump interconnection technology was sighted as a replacement to the traditional wirebonding /1/. A solution for the expensive, unreliable and low productivity WB process was needed. The VLSI era demanded more functionality and reliability of the ever-increasing I/O count. Rent's rule forecasting of an order of

magnitude increase in number of integrated circuits per decade, stressed the need of alternatives to the rather low density capabilities of one and two row wirebonding technology. The introduction of FC technology, which requires a bump formation prior to attachment, seems as a deterrent to the acceptance of the FC interconnection at first. However, this technology will make the die become a standalone package. Protection of this new package would become a challenge, and under bump metallurgy (UBM) discipline became "a science." The common peripheral design of wirebonded die of the early sixties was, in a sense, an "under design" for the FC. Area arrays of different footprints could now be accommodated with the new bump technology. The active devices in the die will now face the connections, i.e., the die needed to be flipped. Surface tension of the soft solder dictates the amount of gap collapse between the die and the die carrier along with the geometries of the lands, i.e., UBM and the die carrier wet able area. The nomination of C4, Controlled Collapse Chip Connection seems a natural description of these bumps. The technology first used in the Solid Logic Technology (SLT) to replace the slow, unreliable and low manual productivity wirebonding technique. The glass passivation that came along with the C4 introduction made a sealed package. Package hermeticity required for wirebonding could perhaps be avoided for many applications by the new sealed technology. The electrical shorting between unpassivated die edges and solder problem was alleviated by the use of a non-collapsible stiff copper ball instead of soft solder that went though reflow. Reliability problems from low cycling fatigue forced the use of soft solder as the die geometry got larger and harsher environments needed to be survived. A thick glass dam that limited the flow of the solder during reflow to the edges of the die physically retained the solder was added. Densities of about eighteen thousand 25 μm bumps on 50μm pitch have been reported. PbSn has been the most popular choice for the C4 metallurgy. Indium alloys have also been used, although with limited applications. Copper, palladium and Nickel are common choices for the UBM. Cr and Ti usually surround terminal metals in the die and Au is used for protection on most of these metals. We must be aware that the C4 bumps serve not only electrical connections, but also as mechanical support for the die. Hence, there have to be enough bums to support the bulky die. Dummy bumps are often used for this purpose. A great advantage of the reflowable bump technology is its self-alignment capabilities from the high surface tension of the materials involved. A 50% misalignment between the pads can easily be accommodated by the FC bumps.

Reliability Issues in FC

The reliability issues on FC are quite different from the previous technology namely wire bonding where yields and manufacturing defect were predominant. FC technology must survive strains imparted by mismatch in expansion of the die and the die carrier. These displacement mismatches arise from different coefficient of expansion (CTE), temperature excursions and temperature gradients the package experience during regular operation.

$$\delta_{cb} = r^* |\alpha_b \Delta T_b - \alpha_c \Delta T_c|$$

Such displacement mismatch increases with the size of the package. In general, bumps further away from the centroid of the package, point where there is no relative displacement between the joined components, also called neutral point, will however, for some cases during actual power on/off cycling, where high temperature gradients may be present, buckling can cause interior bumps to experience highest strains and consequently shorter cycle fatigue life have higher strain and hence shorter life. /2/

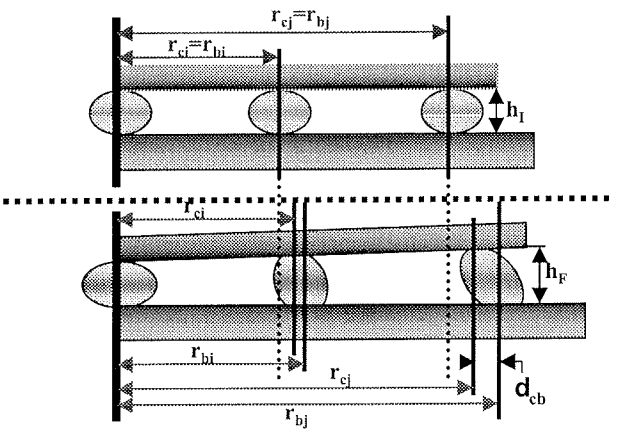

Figure 1. Displacement mismatch between die and die carrier.

The bump geometry for non-encapsulated packages plays a very important role in distributing the applied strains throughout the material. The height of the bump plays a key role in fatigue life, a quadratic relation exist between bump height and fatigue endurance.

$$\text{Life} \prec \gamma^{-2} (f \cdot e^{\Delta H/kT})^{\frac{1}{3}}$$

Recall the average strain of a bump is inversely proportional to its height, and the work done by the interconnection can be derived to be a quadratic function of the strain.

$$U = \int du = \tfrac{1}{2} \int_{\Omega} d\phi \cdot \{\varepsilon\}[K]\{\varepsilon\}^T$$

The material physical properties along with the geometry put some restrains on the current carrying capability of the FC bump. Problems from fusing at very high current levels, and failures due to electromigration mechanisms during machine operation at lower DC currents are potential reliability detractors. Some alloys are more susceptible to the environment, including corrosion, moisture abortion, and dendrite growth. Hermiticity or some environmental protection may be needed. Lead free alloys, for instance, are particularly prom to dendrite growth in the presence of electrical potentials and moisture; some Indium alloys tend

to corrode easily under some environmental conditions. Although, the fatigue life of indium alloys is generally somewhat better than PbSn alloys, the hermeticity requirements for the former has made it less attractive. The radioactivity of Pb based alloys has received special attention due to the generation of soft errors from the alpha-particle emission. The traces of uranium and thorium and daughter element, i.e., polonium may found in this material are the root cause of this intermittent problems. Energy of up to about 8.9 MeV can be imparted by these emitted alpha particles. The intermitant nature of this mechanism can have serious consequences in data storage and active devices.

MATERIAL	Activity(α/cm^2-hr)
C4 Solder (PbSn, 97/3)	0.05 - 10.0
Alumina (Al_2O_3)	0.1
Die Underfill Material	0.002 - 0.02
Plastics	0.04
Silicon Wafer	< 0.004

Table 1. Alpha particle emission rates for some materials used in electronic packaging.

The major wearout mechanisms that affect the FC interconnections are: cyclic creep, corrosion, electromigration and metal migration. The effects of these mechanisms on the package integrity and reliability depend upon several factors: solder type, defect densities, stresses and environment. The introduction of die underfill to improve the reliability of the C4 bump, as well as of a that of a large family of interconnections derived from the C4 concept including, CSP, BGA, CBGA, open a complete new application field to the packaging industry /3/. Various processes have been used to accomplished FC encapsulation including jetting of abrasive underfill materials as well as the less popular forced-flow underfill for some small die and low I/O count.

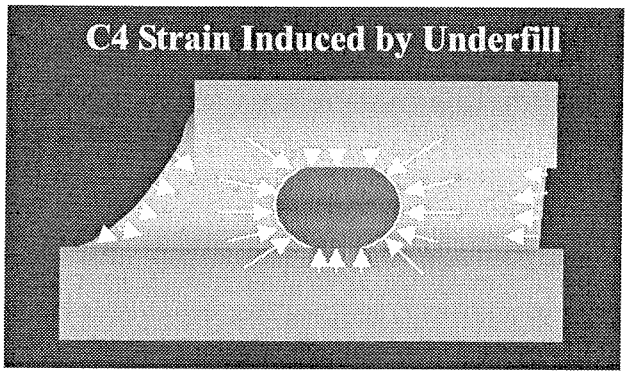

Figure 2. Hydrostatic state of stress resulting from underfilling shrinkage during curing.

Encapsulation makes possible direct chip attach (DCA) to organic carriers with high CTE mismatch to the die, larger geometries, harsher environments and more reliable packages. Nearly one order of magnitude improvement in fatigue resistance can be accomplished with underfilling

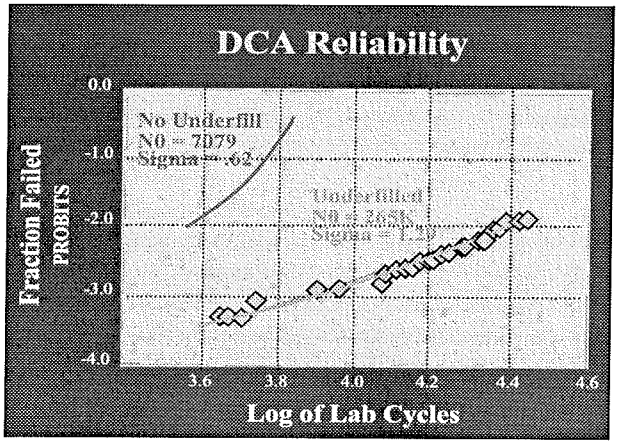

Figure 3. Low cycle fatigue data for no underfilled and underfilled die. (Data from IBM Microelectronics).

Mechanical robustness provided by encapsulants on SMD makes package reliable on many consumer products i.e., cellular phones, laptops, etc. Automotive and avionic applications where high mechanical loads are applied, i.e., vibration and mechanical impact may require underfilling to protect the interconnections from premature fracture/5/.

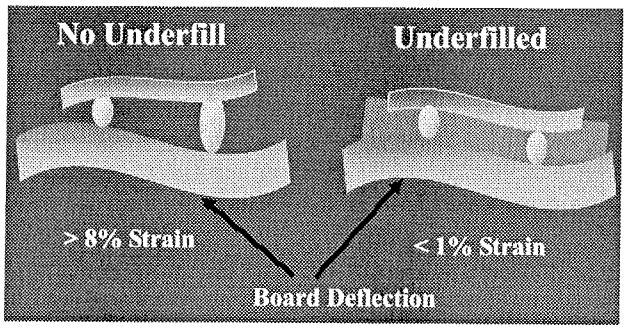

Figure 4. Package deflection from mechanical loading, impact shock resulting from a drop test.

Redistribution layers for the silicon die are becoming a very popular way to utilize peripheral designs and convert them into area arrays footprints, although, this concept have been used for several years as a die design for array packages, today this redistribution techniques is better known as wafer level package (WLP). Cross talk and other electrical detractors need to be addressed when an old peripheral design is converted into fully arrays. Interconnections used in WLP can be larger than those used in C4's. Board densities and low I/O count do not required small bumps. This choice of bump may become closer to the C4 dimensions as high-density boards (HDB) become more popular and package minituralization is required.

Jetting Abrasive Underfill Materials

It was for some time a challenge to be able to jet abrasive materials consistently for extended periods of time due to

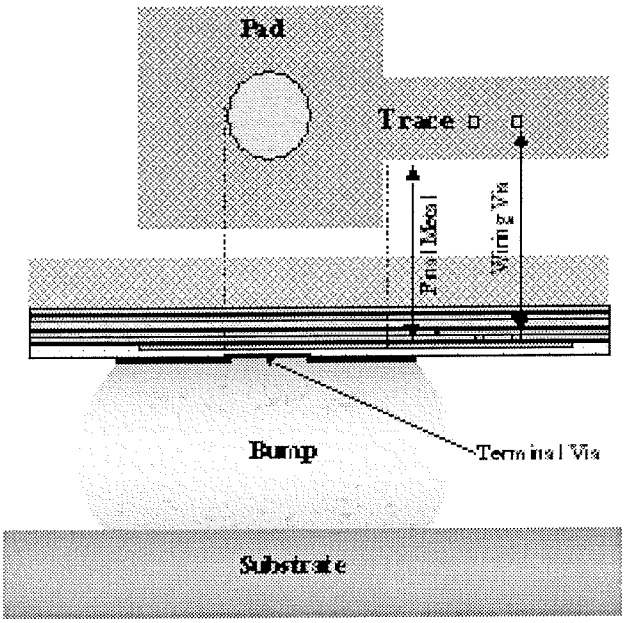

Figure 5. Wafer Level Package showing a two-layer redistribution.

the fact that the materials in contact with the abrasive fluid develop wearout that eventually affect the outcome of the jetted material. Although, this is indeed a fact with the present materials used, the relevant issue is that of the time -to-affect the jetted material characteristics including geometry, volume and mass. Hence, one needs to understand the evolution of such wearout mechanism as function of actual operation and then determine its field mean life. Figure 11 depicts needle wearout evolution resulting from jetting abrasive underfill material, Dexter 4549.

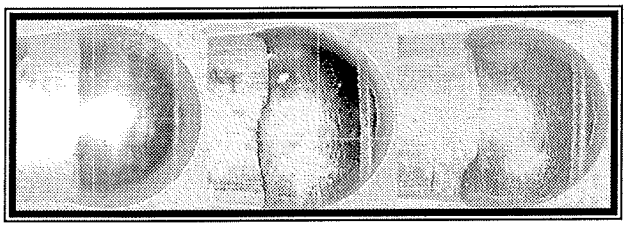

Figure 6. Needle head wearout by the jetting of abrasive underfill material

One can observe the increase on the area of that contour where the needle meets the seat of the jet by displacing the abrasive fluid present prior to impact. Similar wearout can be observed on the nozzle; there the inner diameter has increase and some changes on the geometry (radius of curvature increased) that eventually will affect the volume of material jetted. This nozzle diameter increase is perhaps the parameter that would affect the size volume and shape of the material jetted the most for a given configuration. Some increase in dot size was observed early in the life time test but after a couple of million activations this increase plateau and little to no mass increased was observed subsequently up to about nine million cycles. It was observed that if a new nozzle the size of the dots is similar to that of the dots obtained at the beginning of the test.

Conclusions

- Wire bond technology is a robust and proven to be very reliable. Manufacturing defects, yields may be the main detractor. The reliability is highly dependent on the infant mortality rate.
- FC, CSP and WLP have a common reliability detractor: bump fracture during operation.
- FC main reliability detractor is and has always been, low cycle fatigue.
- Encapsulation of the FC package improves fatigue resistance to the point that today's environments and geometries make the fatigue endurance almost a non-existing mechanism.
- CSP and some large bump WLP have longer fatigue life as expected from their larger bump geometries.
- CSP, WLP and DCA often need to be encapsulated to survive mechanical loading during manufacturing and regular field operation.
- As the package size increase, many of these packages using bump interconnections may need underfilling. Strain levels will increase and hence, fatigue life could be the main reliability detractor for non-encapsulated packages.
- A new jetting technology for underfilling packages including abrasive materials have been demonstrated.
- Small die requiring very low amounts of encapsulation material may be consistently underfilled by using jetting technology instead of the traditionally needle dispensing.

References

/1/ R. Tummala, E. Rymaszewski, "Microelectronics Packaging Handbook.

/2/ K. C. Norris, A. Lanzberg, "Reliability of Controlled Collapse Chip Interconnections," IBM J. Res. Dev. 13, 30 May 1969, pp. 226-238.

/3/ H.Quinones, "Flip Chip-BGA Packaging Workshop Pro," Centre for Management Technology, Singapore, July 1996.

/4/ Alec Babiarz, "Best Dispensing Practices for Flip Chip Underfill," The 3rd IEMT-IMC Symposium, Japan, April 1999.

/5/ H.Quinones, K.Puttlitz, "Flip Chip Solder Interconnections: A Reliability Perspective," Packaging Conference, Orlando Fl, 1996.

Prispelo (Arrived): 09.10.2002 Sprejeto (Accepted): 20.11.2002