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REVIEW OF VARIOUS REALIZATIONS OF INTEGRATED MONOLITHIC TRANSFORMERS

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Key words: integrated transformer, coupling coefficient, planar structure, stacked structure.

Abstract: The integrated transformer is an essential component in many RF integrated circuits. Planar and stacked transformers on a silicon substrate are widely used in low-noise amplifiers, active mixers, voltage control oscillators, filters, etc. This paper gives an overview of different configurations of integrated transformers, their layouts and fundamental electrical characteristics. This review, also, compares the advantages and disadvantages of various integrated monolithic transformer realizations regarding the occupied area on chip, the coupling coefficient, the inductances values and the parasitic effects. Some possibility for improvement of transformer performances, such as using patterned ground shield or design structures with variable width of turns in the primary and secondary winding are proposed, too.

Pregled različnih izvedb integriranih monolitnih transformatorjev

Ključne besede: integrirani transformatorji, koeficient sklopitve, planarna struktura, nakopičena struktura

Izvleček: Integrirani transformator je bistven element v mnogih RF integriranih vezjih. Planarni in nakopičeni transformatorji na silicijevi rezini se uporabljajo pri izvedbi malošumnih ojačevalnikov, aktivnih mešalnih vezjih, napetostno krmiljenih oscilatorjih, filtrih in podobno. V prispevku podajamo pregled različnih možnih konfirguracij integriranih transformatorjev, njihov razpored na površini in osnovne električne značilnosti. Primerjamo tudi prednosti in slabosti različnih izvedb tovrstnih transformatorjev glede površine, ki je zasedajo na čipu, koeficienta sklopitve, vrednosti induktance in parazitnih efektov. Predlagamo tudi nekatere izboljšave transformatorskih lastnosti, z uporabo ozemljenega oklopa ali načrtovanjem strukture s spremenljivo širino linij v primarnem in sekundarnem navitju.

I. Introduction

Constant growth of wireless applications brought to an intensive need for mobile communications and mobile communication devices. According to some research data /1/, the annual worldwide sales of cellular phones have exceeded the figure of $2.5B and in Europe only the profit from equipment and service for mobile communications has overcome $30B. Due to growing need for wireless communication devices radio frequency and wireless market is continuing its development. As well known, there are three main generations of mobile systems, as shown in Fig. 1 /2, 3/.

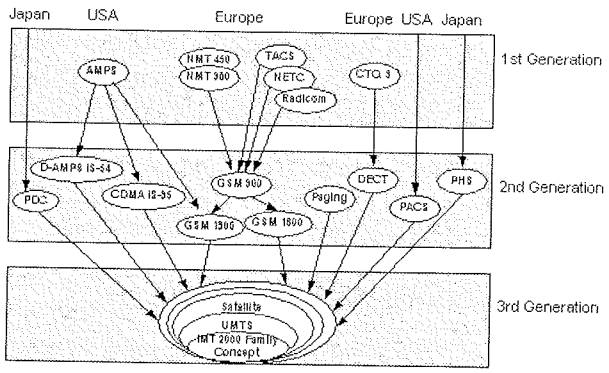
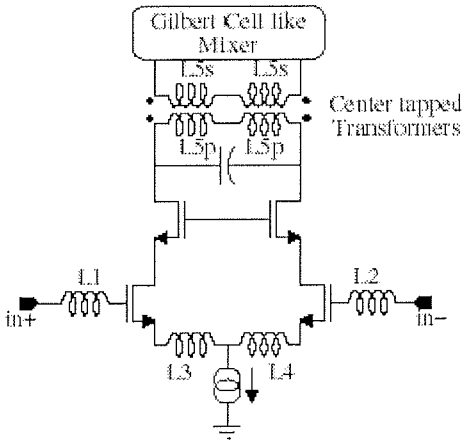


Fig. 1. Mobile communication generations /2/.

Nowadays, the second generation of mobile systems is widely established, using GSM (Global System for Mobile Communications) as a most successful digital wireless service. But different standards that are in use worldwide are quite inadequate for successful interconnecting. So, it was suggested that the third generation of mobile systems should give a worldwide high-performance standard UMTS. UMTS is to provide data rates up to 144Kbits/s, 384 Kbits/s and 2 Mbits/s in macrocellular, microcellular and indoor environments respectively. This would unlock services such as real-time video, mobile entertainment, etc /4/. But, there are many difficulties present that apply to implementation of this technology.

Mobile communication is mainly concentrated on long distance range applications. For short-range distance between the emitter and the receiver, such as in wireless LAN (WLAN), different standards have been introduced. In industry, for WLAN are used standards sanctioned by WECA (the Wireless Ethernet Compatibility Alliance) based on standard created by the 802.11 committee of the IEEE. According to this standard spectrum around 2.4GHz (for Wi-Fi or IEEE802.11a) and 5GHz (for HiperLAN or IEEE802.11a) are used with transmission speeds of 11Mbps. Another standard for short-range communications (10-100m) is Bluetooth. It uses 2.4GHz ISM band and has transmission speed of 780kbs/s. These standards intend to take primate in mobile communications for low band applications.

Silicon based RF (radio frequency) integrated circuits are becoming more and more competitive in wide band frequency range. An essential component of these IC (integrated circuits) is integrated (or on-chip) transformer. They are widely used in mobile communications, microwave integrated circuits, low noise amplifiers (LNA) /5, 6/, active mixers /7, 8/, baluns (give balanced output for unbalanced input) /9, 10/. They are required in impedance matching, signal coupling, and phase splitting applications. Transformers are proved effective for miniaturized sensors, actuators, filters and power converters that should be integrated on chip modules and installed in various electronic systems /11-17/. In Fig. 2 are shown some of the most common applications of the monolithic transformer in LNA and active mixer /8/.



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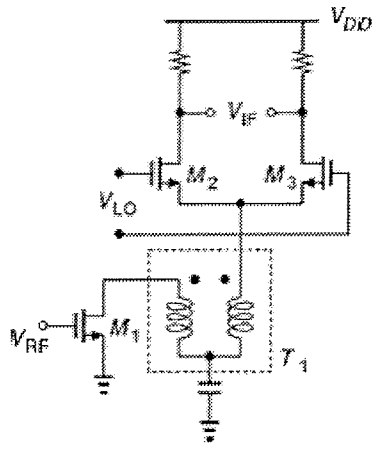


b)

Fig. 2. Integrated transformer in a) LNA application b) active mixer.

In LNA circuit transformer provides an inductive feedback path aiming to improve the linearity and the stability of the circuit. Fig. 2b shows a useful example, where transformer having current gain is placed in the current path of an active mixer.

Although significant efforts have been made in order to improve the characteristics of on-chip transformers, it is still a great problem to bring in piece the opposite demands for low cost, low supply voltage, low power dissipation and low distortion, but high frequency of operation in RF implementation of these transformers /15/. Commonly used transformers are fabricated on lossy silicon substrate hence they are from the start limited to a lower quality factor, coupling coefficient and high parasitic effects between the component and the substrate. However, low cost of Si IC fabrication over GaAs or quartz IC fabrication still dictates the usage of silicon substrates.

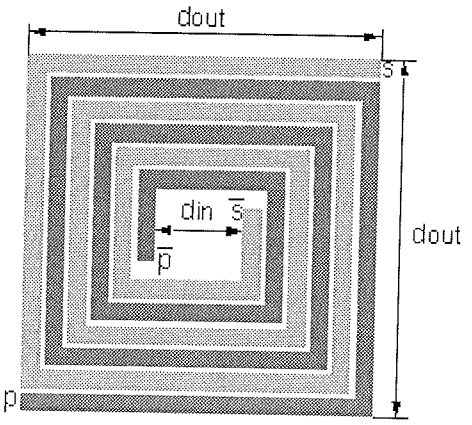
Arbitrary transformer layouts also impact the transformer characteristics. These layouts include parallel windings, interleaved windings, overlay windings and concentric spiral windings and they result in planar or stacked configurations. Planar transformers generally have lower self-inductance, parasitic capacitances and coupling factor, but higher resonant frequency compare to stacked which engage less chip area and has higher inductance values and lower quality factor. Width of the windings, spacing between coils and material used for their fabrication also has influence on overlay characteristics of the transformer.

In order to give the general insight in transformer configurations various constructions will be presented in this paper. We will closely clarify the influence of substrate conductivity, mutual coupling, symmetry and process parameters on transformer behaviour. We also propose some techniques for improvement of integrated transformer performances.

II. Fundamental Characteristics of Integrated Transformers

As well known, monolithic transformer is one of the indispensable elements of many RF ICs. Fig. 3 represents a typical configuration of monolithic planar transformer, its electrical equivalent symbol and layout in the chip /12/.

Transformer is characterized by the inductance (*Lp*, *Ls*) and the voltage (*Vp*, *Vs*) of the primary and the secondary winding and its operation is based upon the mutual inductance of the windings. According to the *Lenz* law variations of the magnetic flux produced by the current flow in the primary winding i_p induce a current i_s in the secondary winding that flows out the terminal $\bar{S}$. They also provide a positive voltage V_s between the secondary terminals. It is important to emphasize that DC signals are blocked by the transformer therefore linking windings at different voltages is possible. There are two ways of connecting the primary and the secondary terminals - in non-inverting or inverting manner. The phase of V_s depends on the choice of the reference terminal. In non-inverting connection an AC signal source and the ground are on primary terminals P and $\bar{P}$, giving a minimal phase shift of the signal at the S output while $\bar{S}$ is grounded. An inverting connection differs in as much that terminal S is now grounded and at the $\bar{S}$ output



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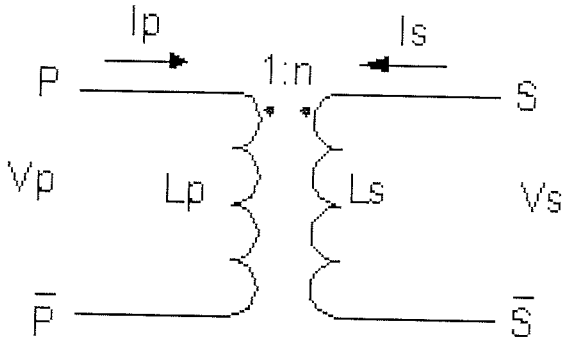

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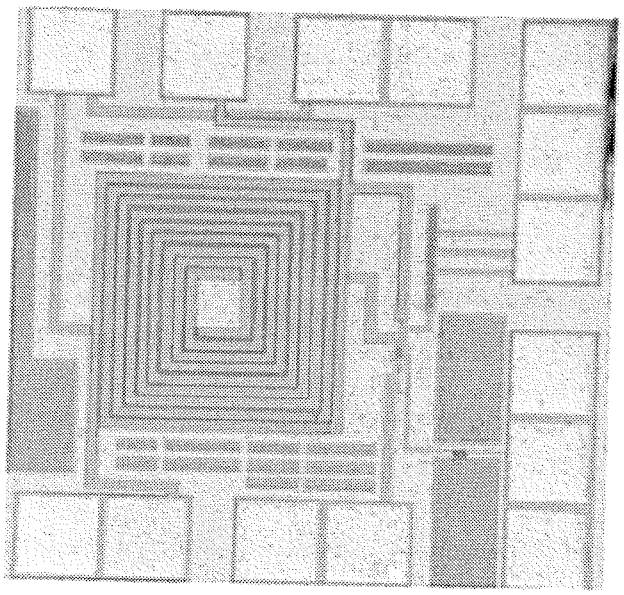

c)

Fig. 3. Monolithic planar transformer a) physical layout b) schematic symbol c) the view on the chip.

produced signal is in antiphase to the signal applied to the primary. Phase shifting is just one of the by-products that take place when using this two constructions /18, 19/.

Due to its common use, it is crucial that insertion losses of the transformer are brought to a minimum. These losses are invoked with finite metal resistance, finite inductances of coils, substrate dissipation and magnetic coupling factor. The metal ohmic losses can be reduced by using high conductive materials for windings or by increasing its thickness. Substrate losses are minimized by utilizing substrate materials with high resistivity or placing isolation layers (made usually by silicon-dioxide) between the substrate and the transformer coils.

There are three main electrical parameters that describe every monolithic transformer - the transformer turns ratio *n*, *k*-factor and *Q*-factor. The transformer turns ratio is related with the current and voltage transformation between the windings as shown (in accordance with symbol 1 : n in Fig. 3b)

$$n = \frac{V_s}{V_p} = \frac{i_p}{i_s} = \sqrt{\frac{L_s}{L_p}}. \qquad (1)$$

Lp and *Ls* represent the inductance of primary and secondary winding of the transformer. Generally, value of the ratio *n* is around 1 for symmetrical structures, but in the case of step-up or step-down transformer topology it can be greater or less than 1, respectively.

The strength of the magnetic coupling between the primary and the secondary is represented by the *k*-factor, which is closely related with the mutual inductance as well as with the self-inductance of the windings

$$k = \frac{M}{\sqrt{Lp \cdot Ls}}. \qquad (2)$$

In the expression (2) *M* stands for mutual inductance of the primary and the secondary coil. The value of *k*-factor primarily depends upon the width and spacing of the metal traces and the substrate thickness. By increasing the number of turns in transformer and decreasing the space between the windings higher values for *k*-factor can be achieved. For the ideal transformer *k*-factor is 1, but for the most fabricated constructions *k* is in range 0.75 to 0.9 /18/.

Quality factor, *Q*-factor, is more technology than geometry dependent factor and it can be calculated by the following equation

$$Q = -\frac{\mathrm{Im}(Y_{11})}{\mathrm{Re}(Y_{11})}. \qquad (3)$$

Y_{11} represents input admittance of the transformer. *Q*-factor is dimensionless and it is proportional to the ratio of the resultant magnetic energy stored in the transformer to the energy dissipated per unit time cycle /20/. Reaching high values for *Q*-factor represents a problem. Great efforts have been made in order to improve this parameter, but the results are not still satisfying.

III. Various Realizations of Integrated Transformers

Prior to integrated transformers on-chip inductors on silicon substrate have been fully analyzed. Many researches have been performed in order to explain, define and illustrate design, modeling and optimization of integrated inductors. But in spite of the many similarities between inductors and transformers significant difference caused by magnetically induced losses are present between their equivalent models. Therefore, only some of the experiences that are used for improvement of inductors can be implemented for transformers, so there are still many unknown rules that are present in the field of monolithic transformer theory.

As inductors, on-chip transformers are usually fabricated by deposition of conductive metal layers on silicon substrate. These metal coils are mainly square and can be placed in planar or stacked configuration. The planar configuration engages larger area on chip in order to achieve higher inductances and *Q*-factor and to minimize the substrate losses. On the other hand, vertically stacked constructions require less chip area for same values of inductance and have high mutual inductance, but a lower *Q*-factor. Which of these layout structures are to use is strongly dependent on the application in which transformer is needed.

A. Tapped (nested) Transformer

Tapped transformer is illustrated in Fig. 4. This is planar transformer and its secondary winding is placed around the primary. Thus, the common periphery between two windings is limited to just a single turn. Due to such configuration, mutual coupling between adjacent conductors mainly contributes to the self-inductance of each winding and not to mutual inductance between the windings. This implies a lower *k*-factor (not higher than 0.6). Both windings can be implemented on the top metal layer and therefore the parasitic capacitance between substrate and windings is minimized. Another disadvantage of this layout is non-symmetrical structure. Tapped transformer can be useful in high-performance broadband amplifiers and other three terminal applications.

B. BifilarTransformer

Bifilar transformer is illustrated in Fig. 5. This is also planar transformer and it is constructed from two parallel conductors that are interleaved. Therefore, mutual coupling between windings have higher influence on mutual inductance. As a result *k*-factor has higher values than in tapped configuration. Self-inductance values of the primary and secondary windings are not equal, because of the non-equal length of the metal. In this structure windings are also placed on the top metal layer. This implies an asymmetrical structure, which can be corrected in the manner shown in the interleaved structure.

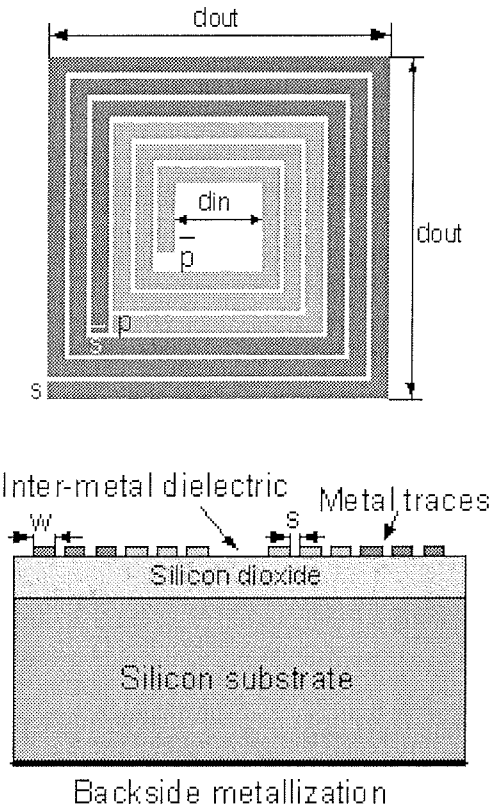

Fig. 4. Tapped transformer.

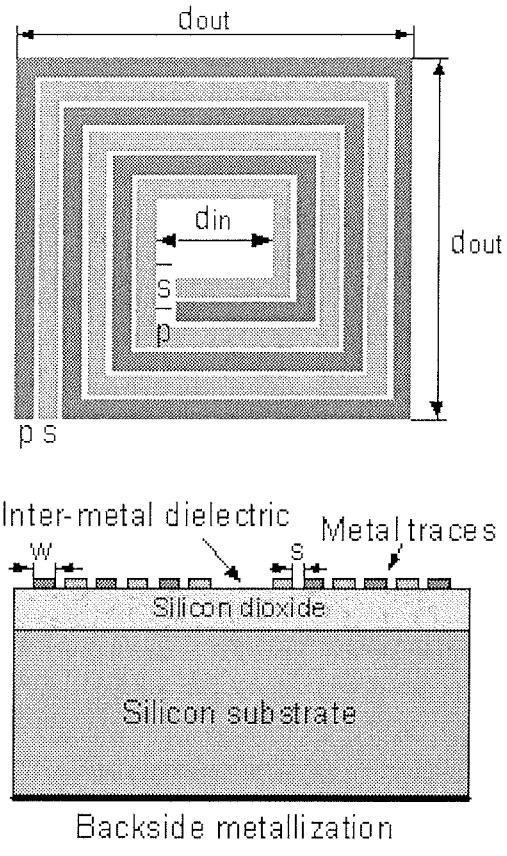

Fig. 5. Bifilar transformer.

C. Interleaved Transformer

This is the most commonly used layout and with it full symmetry of the transformer is achieved. As shown in the Fig. 6 primary and secondary winding are identical and therefore they have almost identical self-inductance value. This configuration gives *k*-factor approximately around 0.7 /21/. Again, placing the primary and the secondary winding on the top layer can minimize the parasitic capacitance between windings and the substrate. Another advantage of this design is that the transformer terminals are an opposite sides of the physical layout, which facilitates connections to other circuitry. It is frequently used in four terminal applications.

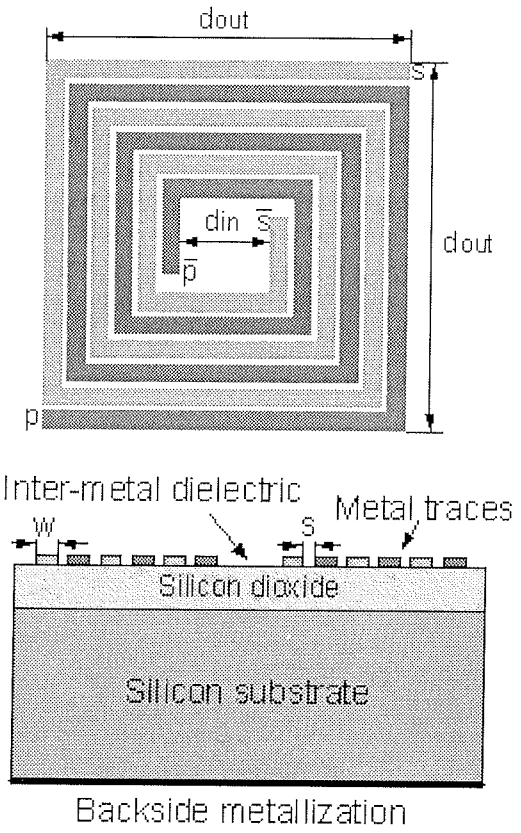

Fig. 6. Interleaved transformer.

To gain higher step-up ratio, transformer shown in Fig. 7 is commonly used. As depicted 1:5 turns ratio is designed with one secondary winding and five individual turns for the primary (connected in parallel). This configuration leads to drastic failure of the primary inductance value and slightly decreases the *k*-factor by increasing step-up ratio /18/. Therefore, the input impedance must be low in order to efficiently couple a signal into the primary of the transformer. The step-up transformer is an ideal feedback element for RF amplifiers.

D. Stacked Transformer

Stacked transformer, or vertical-coupling structure /22/, represents a multiple conductor layer structure, as shown in Fig. 8a and Fig. 8b. This configuration has the advan-

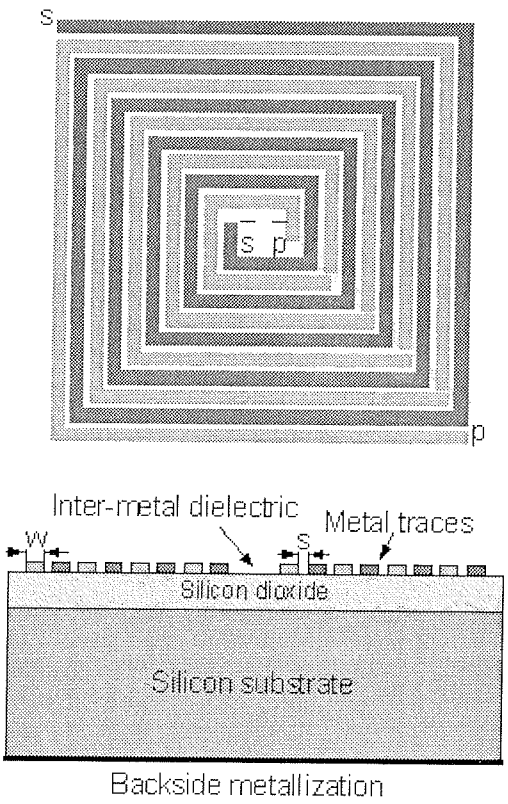

Fig. 7. The step up, 1:5 interleaved transformer.

tage of area efficiency and higher mutual coupling between the windings due to placing the primary coil on top of the secondary. Typical thickness of the dielectric between the layers is 1μm. Stacked transformers mainly have high *k*-factor, up to 0.9, and high mutual inductance, but low self-resonance frequency and therefore relatively small bandwidth /23/. For its fabrication three metal layers are needed, compared to tapped, bifilar and interleaved structure, which require two metal levels. This is not a symmetrical structure. The primary and the secondary winding are placed in adjacent metal layers causing different distances from the substrate. Also, their thickness often differ implying asymmetry in the electrical response of the transformer and unequal resistance of the windings. The lower winding shields the upper one from the influence of the conductive substrate causing difference in the parasitic capacitance to the substrate. In order to improve its characteristics the windings are placed in slightly offset position (horizontally or diagonally shifted), resulting in higher *Q*-factor and resonant frequency, Fig. 8c.

Also, better characteristics of this transformer can be gained by placing the primary winding on lower metal layer. In this manner the substrate losses are slightly increased, but the parasitic capacitance between the windings becomes significantly decreased, thus the self-resonant frequency increases /8/. Non-symmetrical configuration of the stacked transformer can be a limiting factor of its usefulness, but current trends in silicon technology are focused on improving its characteristics and performances.

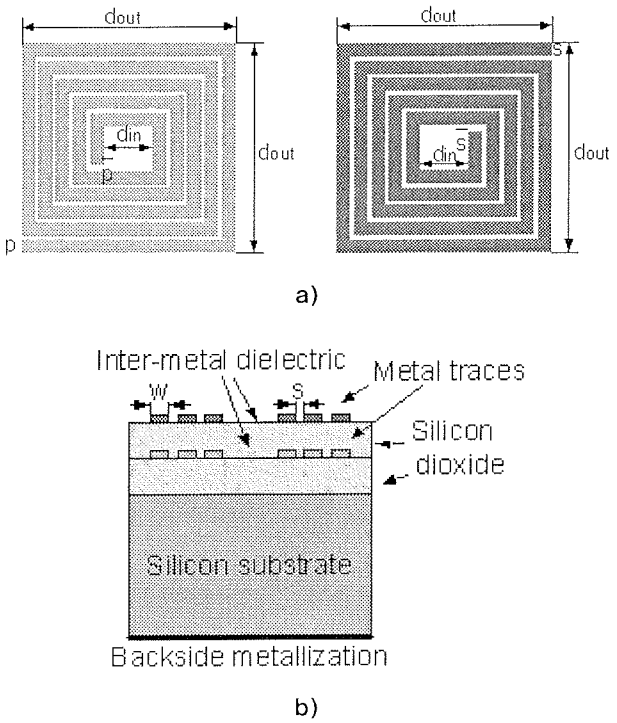

Fig. 8. Stacked transformer a) layout
b) non-offset position
c) offset position of the windings.

Another structure of the stacked transformer can also be used. Fig. 9 /8/ depicts transformer with 1-to-2 step-up ratio. This configuration uses three different metal layers for placing the windings. As shown in Fig. 9 secondary windings are interconnected by via and slightly offset compared to the primary winding placed in between. The number of spirals used for each winding impacts the voltage (or current) gain at a desired frequency. The concept of stacked transformer can be applied, also, to more metal layers to achieve higher voltage gain.

E. Stacked Interleaved Transformer

Fig. 10 represents another realization of monolithic transformer /24, 25/. This is a symmetrical structure and it occupies small area on chip. It consists of two interleaved transformers that are stacked on top of one another. In this structure both the primary and the secondary winding are

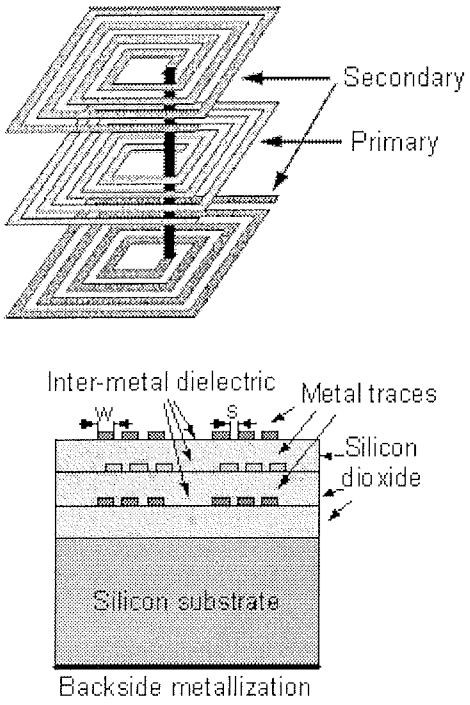

Fig. 9.1: 2 stacked transformer structure.

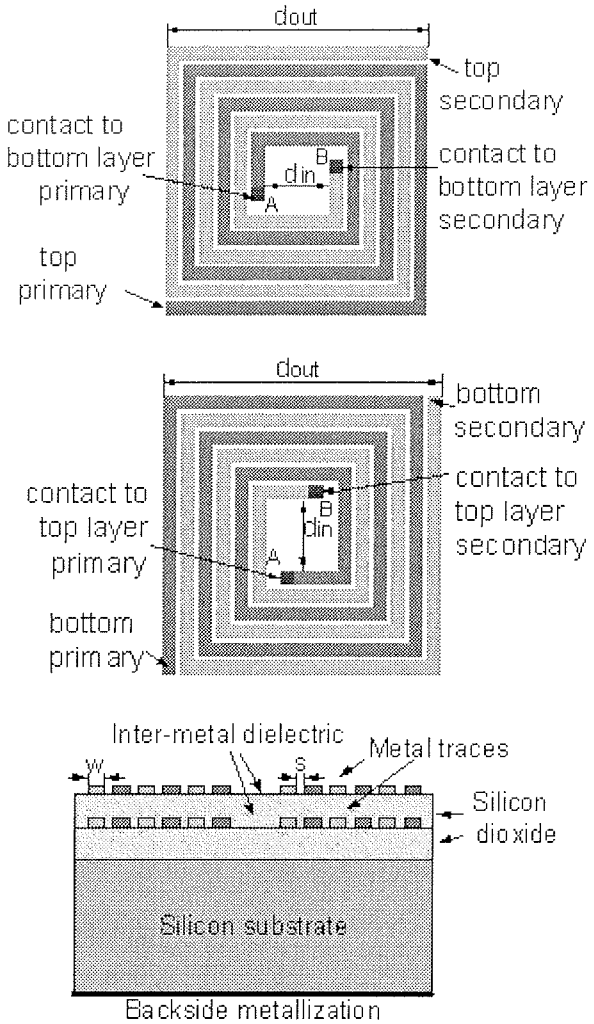

Fig. 10. Stacked interleaved transformer.

present in both metal layers achieving in this manner a full symmetry of the layout. This also implicates reduction of the parasitic capacitance between primary and secondary windings. Matching ends of windings in top and bottom layer are interconnected by vias (A and B in Fig. 10). Stacked interleaved transformer has higher value of the self-inductance of the windings, but lower mutual inductance than the stacked configuration. However, the values of total inductance for these two configurations are approximately the same. This transformer is used in narrowband applications that require symmetry.

F. Central-taped Transformer

Transformer shown in Fig. 11 represents also a mixture of interleaved (Fig. 6) and stacked (Fig. 8) configuration. Depicted transformer has a square structure, consisting of two groups of interleaved coils that are divided along a horizontal symmetry line, forming turns ratio of 4:5. One of the advantages of such construction is alleviation in connecting transformer to other circuitry, due to placing both terminals to the outside edge of the transformer. This construction shows good mutual couplings, which is favored by interwounding of the inductors. Center-taped transformer is utilized in power dividers/combiners and baluns.

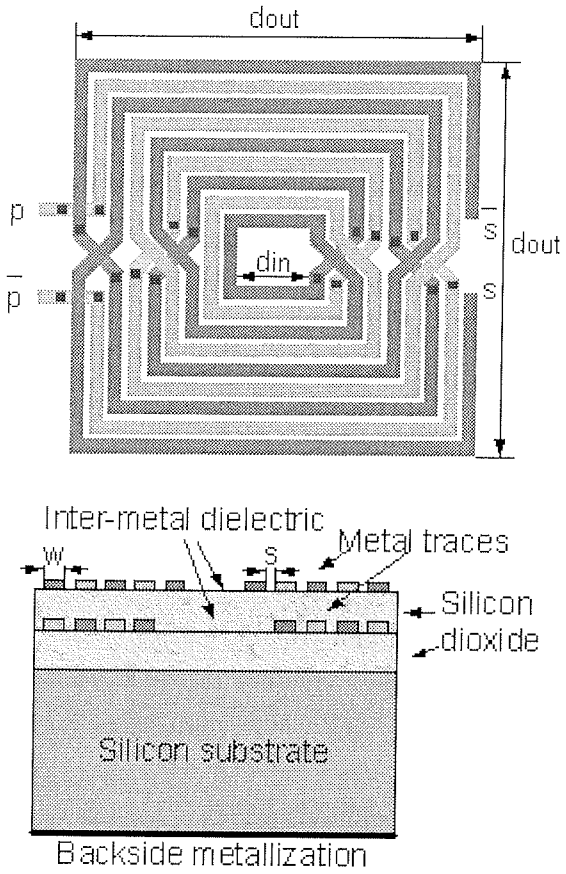

Fig. 11. Central-taped transformer.

Similar transformer configuration is depicted in Fig. 12 /26/. The primary and the secondary winding are laid on the same upper metal layer. Windings don't form whole square segments, yet their parts are connected by vias through one of the lower metal layers at points on vertical symmetry axis. In this configuration, as in center-tapped, primary and the secondary terminals are on opposite outside edges of the transformer and as result connection of the transformer to other electrical components is easy.

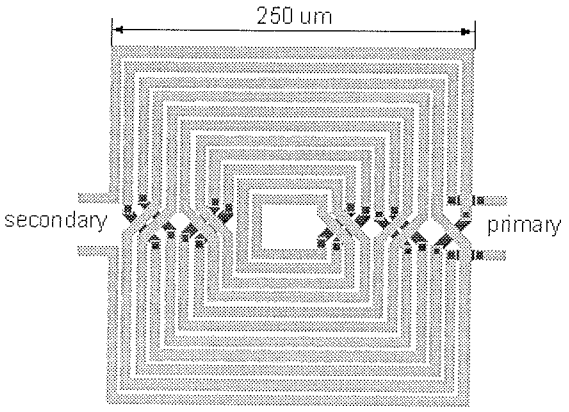

Fig. 12. Integrated transformer with L_p=5.5nH, L_s=7nH, k=0.83 and Q_p= Q_s =10 at 1.7GHz /26/.

The primary and the secondary winding can have other shapes not only square, like octagonal or circular. A special planar winding scheme for circular monolithic transformers which results in a very high coupling coeficient *k* is depicted in Fig. 13 /27, 28/. For realization other values than 1:1 of the turn ratio, different numbers of primary and secondary turns must be used. This implements that some adjacent conductors belong to the same winding which results in a lower *k*-factor. A solution for this problem is to use an interlaced winding-scheme /28/. The monolithic transformer shown in Fig. 13 consists of six primary turns P1-P6 and two secondary turns. The center taps PCT and SCT are available. Fig. 13 shows a three-dimensional top view of the transformer. The outer diameter is about 200 μm and the inner diameter is about 50 μm.

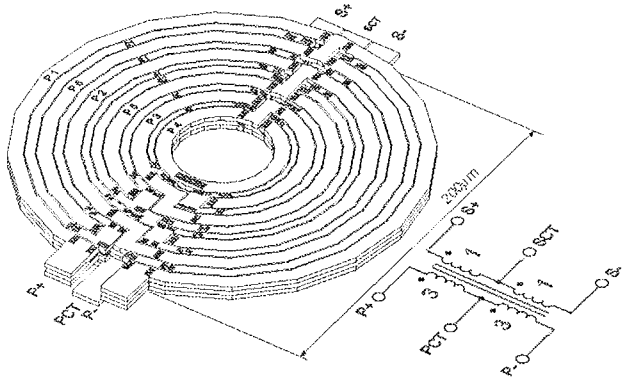

Fig. 13. 3-D-view of the planar high coupling performance transformer /28/.

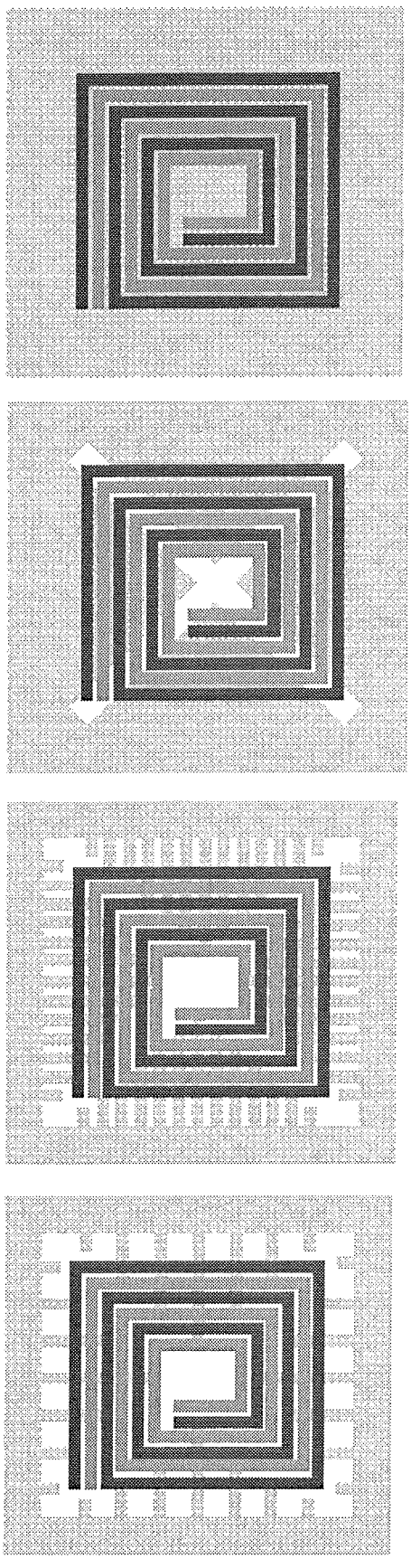

Fig. 14. The various patterned ground shields constructions a) solid ground b) coarse ground c) patterned ground d) bar ground /29/.

IV. Some Techniques for Improvement of Transformer Characteristics

One of additional techniques for improvement of transformer characteristics is implementing patterned ground shields - PGS /29/. PGS is placed between the silicon substrate and the transformer windings, onto the silicon or slightly above it. It is commonly made of aluminum or polysilicon. The main reason for introducing PGS is to limit flow of magnetically induced eddy currents in the silicon substrate. Some designs of PGS are depicted in Fig. 14.

Solid PGS (Fig. 14a) gives good results in preventing losses invoked by the electrical field. But losses caused by the magnetic field and induced eddy currents in PGS are substantial. Therefore the shield must be patterned. In Fig. 14c, 14d are depicted two ways of patterning the shield. In Fig. 14c PGS has metal strips with a 40μm width and 10μm spacing, while in Fig. 14d width of the strips is the same but the spacing between them is 60μm. As shown in /29/ transformer using PGS with larger spacing has lower values of inductance and *Q*-factor, but has higher resonant frequency and larger bandwidth than the other configuration. Introduction of these PGS leads to lower values of inductance and *Q*-factor and voltage gain on lower frequencies, but give better *k*- and *Q*-factor on frequencies higher than 4GHz compared to transformers without PGS. On frequencies higher than 14GHz shields lose their purpose leaving the transformer with the same characteristics as without PGS.

In order to decrease substrate losses it is advisable to use surrounding metal tracks for ground pads in the vicinity of on-chip components, Fig. 15. This ground ring enables dissipation of the magnetic flux in the conductive silicon substrate. According to the previous experience with inductors position of the ground ring implicates variations of the self-resonance frequency of the transformer and usage of substrate area is increased. As the ground pads are moved farther from the transformer resonance frequency increases, till it doesn't reach a saturation value.

Bulk and surface micromachining are techniques compatible with standard IC industry of inductors and transformers. By means of these techniques, electrical coupling losses can be reduced. They employ substrate removal underneath planar components (inductor, transformer...). In this way substrate losses and electrical coupling are eliminated from the component, resulting in substantial increase of self-resonant frequency and quality factor /30/-/33/. However, when the silicon substrate is removed, magnetically induced losses (eddy currents) become much more relevant. They are directly dependent on the time varying magnetic flux through the coils. They represent frequency dependant losses and they increase while the coil width increases, so they must be taken into account /31/.

The recently new solutions have been developed based on layout optimization and finding the optimum value between the magnetically induced and ohmic losses in metal

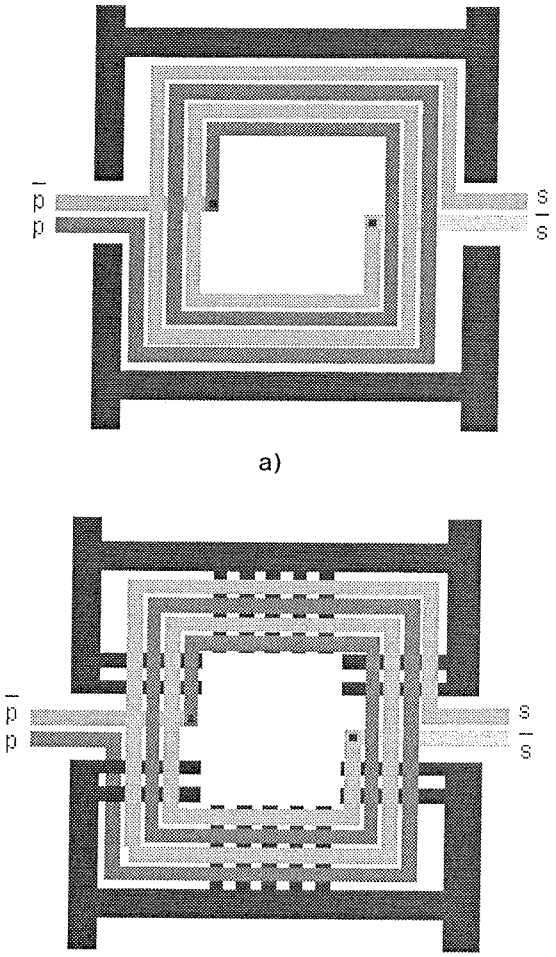

Fig. 15. Interleaved transformer with
a) the ground ring, and
b) the ground ring and the PGS.

coils. The first step of this optimization is analyzing the series resistance of the transformer's coils. It is widely known that ohmic losses of this resistance decrease while the

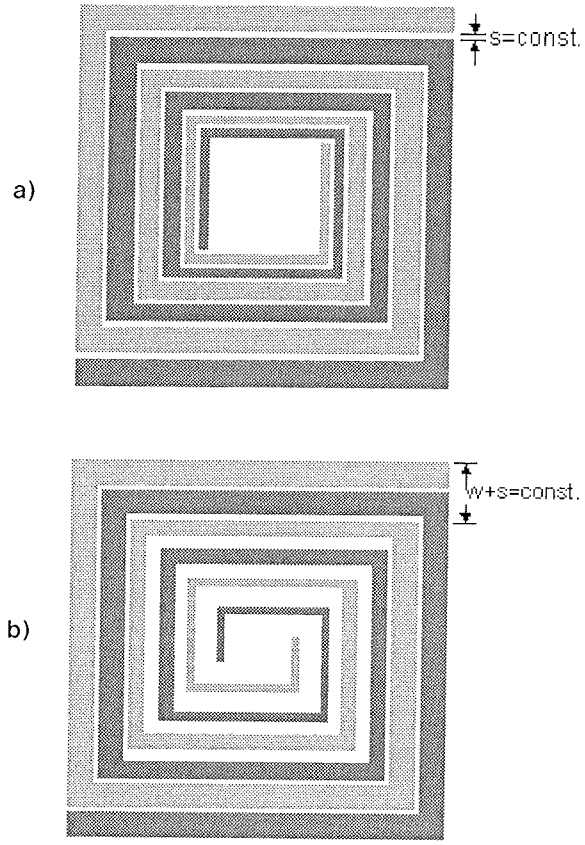

Fig. 16. Planar transformer with variable width of conductor segments.

width of the metal strips increases, but the magnetically induced losses enhance. So, there must be an optimum strip width, which minimize series resistance and maximize *Q*-factor. Layout optimization techniques can be used not to find the optimum width of the coil, but to embrace the width and/or the pitch (the thickness) of every turn as the variable part of the design. For inner turns narrow strips are used to optimize magnetic field losses, which are at the highest value in the center of the primary or secondary

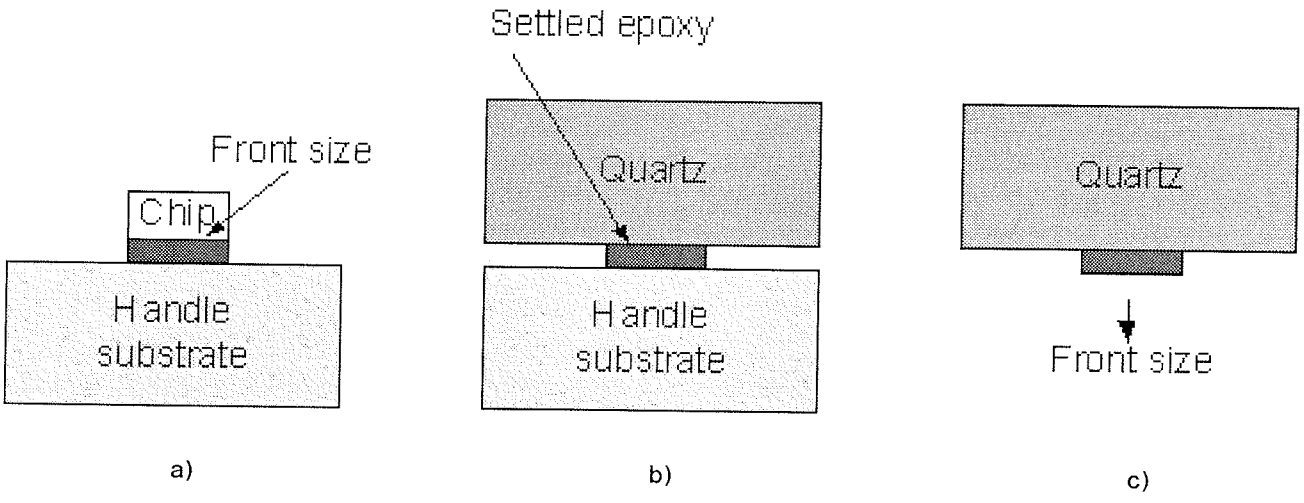

Fig. 17. Substrate transfer technique /29/.

coil of integrated transformers. The wide strips optimize the outer turns, where ohmic losses are predominant. In this manner much better results can be obtained (higher *Q*-factor and resonant frequency) /30/.

Planar transformers with variable conductor width of the primary and the secondary winding can be realized in two configurations as it can be seen from Fig. 16. The form shown in Fig. 16a is more used, where the spacing between adjacent turns is constant (*s*=const.). The configuration depicted in Fig. 16b has property that the total distance between neighboring segments is constant (*w*+*s*=const.)

Another advanced technique can be used to improve characteristics of the monolithic transformer at high frequencies /29/. By employing a substrate transfer technique lossy silicon substrate is replaced with lossless quartz substrate. First step in this process is to mount the transformer die onto a peace of insulating quartz by dissolvable epoxy glue (Fig. 17a). Then silicon substrate is removed by mechanical polishing with diamond sand paper until 30μm of silicon is left. This remain of silicon is removed by reactive plasma etching at room temperature. Following step is to use epoxy to attach another piece of quartz onto the etched surface of the die (Fig. 17b). By dissolving the epoxy glue in acetone substrate transfer technique is finished (Fig. 17c). Transformer on the quartz substrate has improved *Q*-factor and voltage gain at higher resonant frequency. However, the influence of the substrate on the *k*-factor and inductance is negligible. The usage of this technique is not yet so popular due to more complicated fabrication.

V. Conclusion

Integrated monolithic transformer performances greatly depend on geometrical and process parameters. Opposite demands are often expected and therefore a good balance should be found among self-inductance value, mutual coupling, parasitic capacitances, resonant frequency and naturally the cost of fabricated component. In this paper we have presented various transformer configurations and gave their fundamental characteristics. As we have said, planar structures occupy plenty space on chip, but they have high resonant frequency and therefore can be used in band-wide applications. Tapped transformer has also a low *k*-factor and fairly low self-inductance. Interleaved and bifilar configurations have pretty high values for coupling coefficient, but low self-inductance. On the other hand, stacked structures engage less chip area and are used in narrow-band circuits as a terminal device due to their low self-resonant frequency. Hence, this work compares the advantages and disadvantages of various monolithic integrated transformer realizations and, also, gives some possibility for improvement of integrated transformer performances.

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