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DESIGN & TEST OF SYSTEM-IN-PACKAGE

P. Cauvet[1], S. Bernard[2] and M. Renovell[2]

[1]NXP Semiconductors, Caen Cedex 9, France
[2]LIRMM, University of Montpellier, Montpellier, France

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Abstract: System-in-Package (SiP) is now becoming a significant technology in the semiconductor industry. In this talk, the basic SiP concepts are first discussed, showing difference between SiP and SoC, illustrated by some examples, drawn from real-life cases. The specific challenges are considered from the testing point of view, focussing on the assembled yield and defect level for the packaged SiP.

Načrtovanje in testiranje sistemov v enem ohišju

Kjučne besede: sistem v ohišju, testiranje SiP, izkoristek SiP

Izvleček: Izdelava sistemov v ohišju (SiP) dandanes predstavlja eno od pomembnih tehnologij polprevodniške industrije. V prispevku najprej opišemo osnovne koncepte SiP, kjer predstavimo razliko med SiP in SoC na nekaj primerih iz prakse. Še posebej predstavimo posebne izzive s stališča testiranja in se osredotočimo na izkoristek in gostoto defektov montaže SiP.

1 Introduction

Around the year 2000, the mobile phone applications have induced a paradigm shift in multi-chip packaging: the SIP has now become the fastest growing area in the packaging domain due to its associated system integration benefits. In the mobile phone applications, the system integrators have to face short product life cycles and they came to the first evidence that integrating existing and available ICs when a SiP can be used, is easier than to reinvent new ICs from scratch.

The International Technology Roadmap for Semiconductors published by the Semiconductor Industry Association defines a system-in-package (SiP) as any combination of semiconductors, passives, and interconnects integrated into a single package /1/. As a matter of fact, the definition can be even larger: A SiP can combine different die technologies and applications with active and passive components to form a complete system or sub-system, where the embedded components are interconnected by wirebond, flip-chip, stacked-die technology, or any combination of the above.

A SoC is created from a single piece of substrate, i.e., a single die; the single die is fabricated in a single process technology with a single level of interconnections from the die to the package pads or to the interposer, whereas a SiP is created from several different dies, i.e., multiple parts; these dies can come from a broad mix of multiple process technologies, such as CMOS, GaAs, or BiCMOS, with multiple levels of interconnections from die/component to die/component, or from die/component to the package pads or to the interposer. One could say that everything is 'single' for a System-On-Chip while everything is 'multiple' for a System-In-Package.

Figure 1 shows an example SiP in a global system for mobile communications (GSM) application where multiple dies, components, and leadframe connections are embedded in a single package. The multiple dies as well as the multiple levels of interconnections are clearly visible on this example.

In recent years, many types of SiP have been developed, differing by their type of carrier or interposer to be used for holding the bare die (or component) and the type of interconnections to be used for connecting components. The carrier or interposer can be a leadframe, an organic laminate, or siliconbased as illustrated in Figure 2. Another possibility is to stack components on top of each other, called stacked dies. Stacked dies are represented in Figure 3.

SiP offers a unique advantage over SoC in its ability of integrating not only any type of semiconductor technology and passive components into a single package, but also micro-electromechanical system (MEMS) with circuitry to provide a fully functional system.

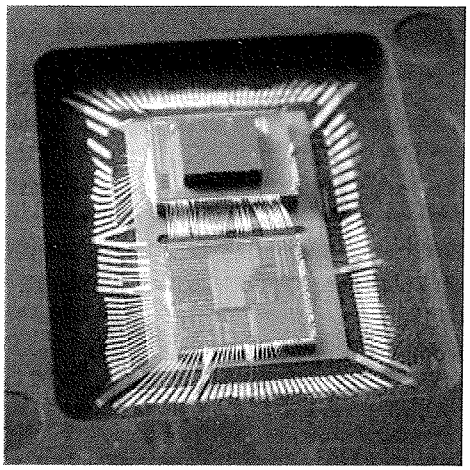
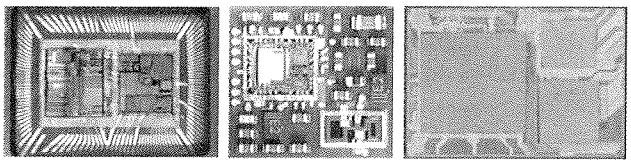


Fig. 1: Multiple dies, components and interconnections in one package



a) Leadframe b) Laminate c) Silicon-based

Fig. 2: Examples of carrier style

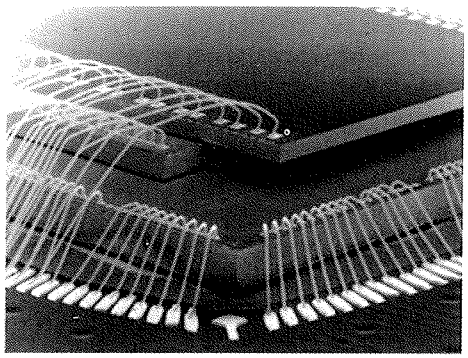


Fig. 3: Example of stacked components /2/

2 SiP Challenges

The fabrication and test flow of a standard SiP is more complex than the SoC flow. A SiP is basically the assembly of N dies (die #1 to die #n), and possibly some passive components, using a carrier or interposer. The resulting SiP can be a very sophisticated and expensive product. In addition to these costs, it is important to note that typically a defective SiP cannot be repaired. All these arguments lead to the following statement:

'The SiP process is economically viable only if the associated yield Y_{SiP} of the packaged SiP is enough high'

The 'production' yield of the packaged SiP can be defined by the number of correct SiPs (Ac) divided by the total number of assembled SiPs (A):

$$\mathbf{Y_{SiP}} = Ac / A$$

In order to optimize the yield $\mathbf{Y_{SiP}}$ of the packaged SiP, it is obviously necessary to minimize the number of defective parts. The origins for these defective SiP are numerous and diverse, among them, a defective substrate, an incorrect placement or mounting of the dies and components, a defective soldering or wirebonding of the dies and components, a stress on dies during assembly, defective dies, etc. Consequently, for an n-die SiP, the yield can be expressed as follows:

$$Y_{SiP} = 100\times [P_1 \times P_2 \times \ldots \times P_n] \times P_S \times P_A$$

where Pi is the probability that die #i is defect-free, P_S is the probability of substrate being defect-free, and P_A is the probability of assembly process being defectfree.

The above equation demonstrates the cumulative effect of the different defect levels. The substrate used as a carrier is generally made of a mature technology with a high level of quality, whereas, the assembly process and the quality of the mounted dies are particularly critical.

Indeed, SiP are only viable if the quality of the assembly process is sufficiently high. In the IC fabrication context, yields (Yic) of around 75% are quite common. But the SiP assembly context is totally different, because the yield associated to the assembly process Y_A must be very high. For example, a viable assembly yield for SiP is typically around 99%.

Moreover, an acceptable assembly yield requires that every die in the SiP exhibits a very low defect level. In other words, only high quality components are used in the SiP assembly process. Consequently, the bare dies used in the SiP assembly process must exhibit the same, or better, quality level than a packaged IC. This is known as the Known Good Die (KGD) concept, which can be stated as follows:

'KGD: A bare die with the same, or better, quality after wafer test than its packaged and 'final tested' equivalent

The majority of the challenges to achieve the KGD quality lie in the testing of the mixed signal and RF blocks.

Under the assumption that only high quality components (KGD) are used in the assembly process, the test process of the packaged SiP must focus on the faults that originate from the assembly process itself. Therefore, testing a SiP with KGD is a combination of functional test at the system level with structural test and more precisely 'defect oriented test' at the die and interconnect level..

3 Bare-die testing

Two major factors have to be considered by the manufacturers in bare die testing: test escapes of the die and infant mortality in the final package, at system level. Meeting the KGD target for high-volume markets represents a big challenge for the industry, because high pin count, high speed

and high frequencies can be handled more easily with a packaged stand-alone device than at wafer level /3/. In this section we present several solutions to help achieve this target, successively based on advanced probing techniques, alternative test methods, and reliability screening.

3.1 Advanced probing techniques

The so-called 'cantilever' probe card technology has been used for a long time and still represents the biggest market share in this segment /3/.

However, the development of very complex devices, combined with the expansion of multi-site (parallel) testing, pushes the fabrication of probe cards towards the limits of the technology, while the size and the pitch of the pads regularly decreases, pulling the probe cards towards novel, but expensive, technologies /4/. On top of those requirements, the growth of chip-scale and wafer-level packages puts further demands on probes, which contact solder bumps instead of planar pads.

Some solutions are now available able to push the mechanical limits forward. Among them, MEMS-based implementations of probe cards are now starting to replace the traditional macroscopic technologies /5/. An example of a MEMS-based probe card is shown in Figure 4.

Another solution for KGD wafer testing is also emerging, which consists of replacing the traditional probe card by a non-contact interface /7/ to avoid any scrubbing of the bond pads.

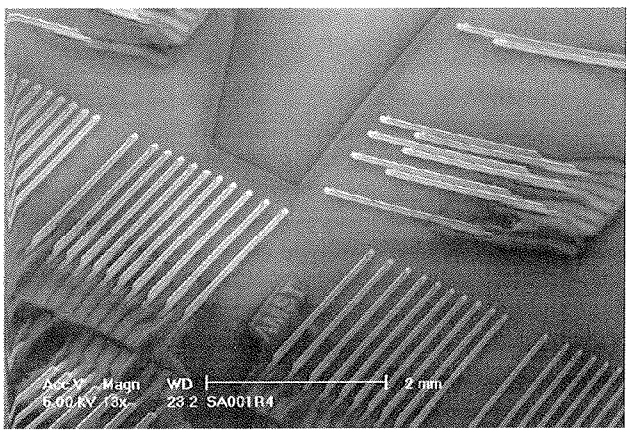


Fig. 4: View of probe tips in MEMS technology /6/

From an electrical perspective, KGD cannot be achieved for most of RF and high-speed mixed-signal ICs. So far, analog ICs are mainly tested against their specified parameters. This strategy has proved to be effective, but places a lot of requirements on the test environment including ATE, test board, and probe card. Indeed, testing RF and high-speed mixed-signal ICs represents a big challenge, because the propagation of the signal along the path may be disturbed by parasitic elements. The integrity of the RF signals can be guaranteed only with short, impedance-matched connections between the source and the load.

Compared to the traditional cantilever probe card, the "membrane" technology can solve many problems, by reducing the distance between the pads and the tuning components. Micro-strip transmission lines are designed on a flexible dielectric material in order to connect the test electronics from the ATE to the DUT /8/, /9/, /10/. This technology already offers a number of significant advantages for high-performance wafer test, from both electrical and mechanical perspectives.

Another approach to KGD for RF/analog products relies on alternative test methods. A representative example is given by a technique that consists of ramping the power supply and observing the corresponding quiescent current signatures /11/.

Other approaches propose to re-use some low-speed or digital internal resources of the DUT, and to add some DfT features in order to get rid of RF signals outside of the DUT /12/ /13/. The combination of such methods in conjunction with some structural testing techniques will help reach very high defect coverage for analog, mixed-signal and RF chips.

3.2 Reliability screening

Burn-in testing is the traditional method for eliminating infantile defects. It is done by applying abnormally high voltage and elevated temperatures to the device, usually above the limits specified in the data sheet for normal operation. Burn-in test is an effective method, but too costly for high volume ICs for low cost consumer and mobile markets. Novel reliability screens need to be developed, that can be applied at the wafer level and that may fulfill the targets without burn-in testing. In recent years, diverse alternate methods were developed and published to reduce the infantile mortality of the dies, such as IDDq /14/, high-voltage stress /15/, /16/, or statistical-based methods /17/ . Screening methods are not unique and the trend is to couple them in order to achieve a reliability level that fulfills the requirements for KGD.

4 System test

System test at the SiP level can be considered in two ways: functional system test, and access methods.

4.1 Functional system test

In a traditional system test, the application specifications of the system are tested and the overall functionality is checked. The biggest advantage of this test method is the good correlation at system level between the measurement results of the SiP supplier and those of the SiP customer (end-integrator). Also, the required quality level can be reached in very short time. However, this approach suffers from many drawbacks, such as a complex and expensive test setup, long test times, and lack of diagnosis capabilities.

Enhanced solutions have been proposed in recent years, mainly driven by wireless communications applications. Basically, we consider a system made of a transmitter and a receiver, as shown in Figure 5. In this example, we consider a SiP made of three dies: digital plus mixed-signal circuitry, an RF transceiver including a low-noise amplifier (LNA), and finally a power amplifier (PA). Other elements, such as switches, or filters, can also be placed on the substrate.

In this typical architecture, two paths are considered: the transmitter (Tx) path, and the receiver (Rx) path. To measure the system performance, the test is split in two paths, the receiver path (BER, bit error rate) and the transmitter path (EVM, error vector magnitude), respectively. In practice, a receiver is tested using sources able to generate digitally-modulated RF signals, and a transmitter is tested using a demodulator and a digitizer.

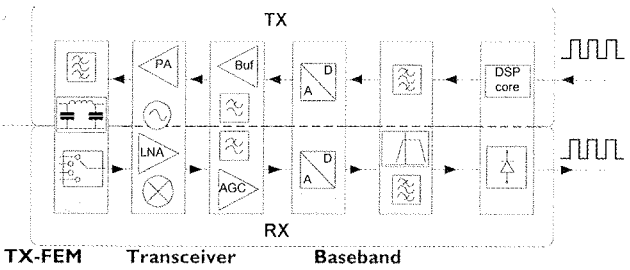


Fig. 5: A typical transceiver system

An original method is proposed in /18/, where the signals propagated through the analog paths are used to test the digital circuitry. Loop-back techniques are also increasingly proposed in literature. Most of these techniques are combined with alternate test methods, in order to reduce the test time and to be more predictable. Several solutions were recently published /19/, /20/, /21/.

As previously discussed, testing bare dies after assembly is a critical phase to achieve an economically viable SiP and to give some diagnostic capabilities. The test consists of two complementary steps, structural testing of interconnections between dies, and structural or/and functional testing of dies themselves.

The main challenge is to access these dies from the primary I/O of the SiP. The total number of effective pins of the embedded dies is generally much higher than the number of I/O for the package. Moreover, in contrast to SoC where it is possible to add some DfT between IP to improve controllability and observability, the only available active circuitry for test in the SiP are the connected active dies. Consequently, improving testability places requirements on the bare dies used for the SiP and the definition of a specific SiP Test Access Port (TAP).

4.2 SiP Test Access Port

The SiP context imposes some specific constraints on the TAP. This SiP-TAP must afford several features, mainly,

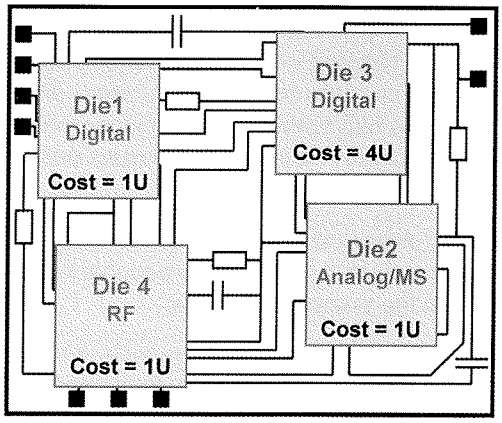


Fig. 6: Conceptual view of an example of SiP

among them, the access for die and interconnection tests, SiP test enabling at system level as it would be for a SoC, and additional recursive test procedures during the assembly phase.

Taking all the requirements into consideration, the SiP TAP controller must have two configurations: one during the recursive test and the other for the end-user test. Following the ordered assembly strategy, the first die will integrate the SiP TAP controller and, as a result, the ID code of the SiP will be the ID code of this first die. Figure 7 shows the conceptual view of the multimode SiP TAP with switches and multiplexers to implement the star or the ring configuration. The 'star' configuration allows a direct access to each die to facilitate recursive testing during the assembly. The 'ring' configuration is designed such that the end-user cannot detect the presence of several dies, either for identification (there is only one ID code), or for boundary scan test.

Thus far, no SiP TAP standard exists, but architectures have been proposed based on the IEEE 1149.1 standard /22/ or the IEEE 1500 standard /23/.

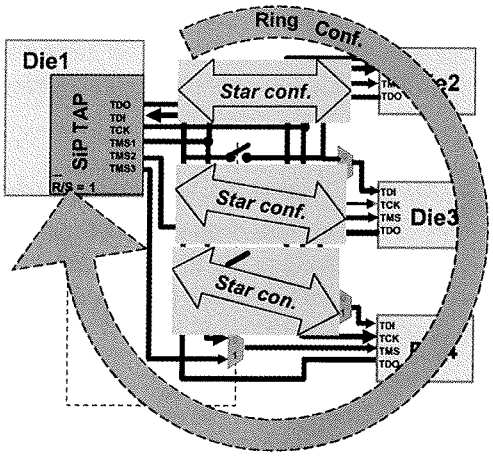


Fig. 7: Multi-configuration TAP

4.3 Interconnections

There are two types of interconnections: interconnection between dies and interconnection between die and SiP bond pads. The test method for interconnections is equivalent in both cases but the access issues are obviously different.

Concerning digital interconnections, the test of interconnection is performed through the boundary scan (IEEE 1149.1) with the external test mode.

Similarly to SoC with internal IP, we face the problem of accessing the inputs and the outputs of internal dies. In fact, SiP with four times less external pads than internal pins of embedded dies is very common. Consequently, we rely on boundary scan facilities for testing the internal dies. By activating the bypass function in dies, it is possible to reduce the length of the scan chain. However, "at speed testing" requires using techniques such as compression, DfT, and BIST. Unfortunately, in the SiP context, no additional active silicon is available and so no additional circuitry can be implemented. Consequently, either BIST or DfT should already exist in the die itself. Obviously, there is very little chance to have this DfT facility available on the hardware of one of the other dies because the design of each die is completely independent. A solution consists of using the software or programmable capabilities available on the other digital dies to implement a fully configurable DfT. Another method uses a transparent mode of the other dies to directly control and observe from the primary I/O of the package.

Unfortunately, we might find a SiP configuration where none of these techniques can be applied. In this case, the only solution to access the specific internal pin is to add direct physical connection SiP I/O pins while attempting to meet all the associated requirements in terms of signal integrity. In the specific case of a memory die, the access problem is critical since these embedded memories are generally already packaged. These Package-on-Package (PoP) or Package-in-Package (PiP) configurations have no BIST capabilities and thus the BIST has to be implemented in another digital core for application to the embedded memory.

4.4 Analog , RF and MEMS components

For the test of analog, mixed-signal, or RF dies, the two most significant challenges are the cost reduction of the required test equipment, and the test of embedded dies because of difficulty to access to these dies after SiP assembly.

From the point of view of the test engineer, the possibility of assembling heterogeneous components might be a testing nightmare since the test equipment has to be able to address the whole set of testing requirements in all domains: digital, RF, analog, etc, resulting in unacceptable test costs (ATE options, test time, etc.). The functional tests are required to achieve a satisfactory test quality and to give some diagnostic capabilities at the die level. Even if all the tests previously performed at the wafer level for each die are not necessarily required after assembly, the price of the test equipment and the very long test sequences usually make the test cost prohibitive. As a result, specific approaches must be considered to reduce the testing time and the test equipment cost.

A common approach is to move some or all the tester functions onto the chip itself. Based on this idea, several BIST techniques have been proposed where signals are internally generated and/or analyzed /24//25//26//27//28/. However, the generation of pure analog stimuli and/or accurate analog signal processing to evaluate the system response remains the main roadblock.

Another proposed approach is based on indirect test techniques. The fundamental idea is to replace the difficult direct measurements by easier indirect measurements, provided that a correlation exists between what is measured and what is expected from the direct measurements. This approach looks promising for testing RF systems, for example the techniques using artificial neural networks /35/.

Other techniques consist of transforming the signal to be measured into a signal that is easier to be measured by ATE. For example, timing measurement is easier for ATE than a precise analog level evaluation and so, a solution is to on-chip convert an analog signal to a proportional timing delay. Another possible solution consists of using DfT techniques to internally transform the analog signals to digital signals that are made controllable and observable from the chip I/Os /29//25/. As a result, only digital signals are externally handled by less-expensive "digital" test equipment (a Low Cost Tester for example). These techniques are limited by the accuracy of the conversion of the analog signal. A similar approach attempts to avoid the problem of conversion accuracy by assuming several digital-to-analog converters (DACs) and analog-to-digital converters (ADCs) are already available to obtain a fully digital test /30/. All the SiP including RF, low-frequency analog, and/or mixed-signal devices can benefit from these above techniques;

Micro-Electric-Mechanical-Systems (MEMS) represent the extreme cases of heterogeneous systems. Indeed, in a typical MEMS, we can find accelerometer, pressure sensor, temperature or humidity sensors, micro-fluidic system, bio-mems, etc.

The first problem for MEMS testing begins with the required test equipment. MEMS are generally dedicated to generate or actuate non-electrical signals. Consequently, test equipment should allow generation and measurement using sound, light, pressure, motion, or even fluidics. Because of their price, the difficulty to implement them, and the very long associated testing time, the use this type of equipment for production test (especially at wafer level) is rarely an option /31/. In production test environment, only fully electrical signals are actually viable.

In this context, two approaches are likely: perform an indirect structural or functional test on an electrical signal that would be an image of the physical signal associated with the MEMS under test, or implement some DfT circuitry allowing one to convert the physical signal associated with the MEMS to an electrical signal /32/, /33/.

Another major challenge in MEMS testing is due to the significant package influence. Indeed, MEMS characteristics depend on the properties and the quality of the package used. As a result, the cost of MEMS testing can be prohibitive /34/.

For MEMS integration into a SiP, the classical problems of MEMS testing are exacerbated. From the package standpoint, the SiP concept poses new challenges. For monolithic MEMS in CMOS technology, direct integration of the bare MEMS onto the passive substrate is conceivable. For more complex MEMS, the bare die can be flipped onto the passive substrate. Achieving a perfect etching and sealing of the cavity, and guaranteeing the cavity quality during the life of the system represent the new challenges. In this context, one solution consists in adding an additional and simple MEMS into the cavity to monitor the cavity characteristics as illustrated in figure 8.

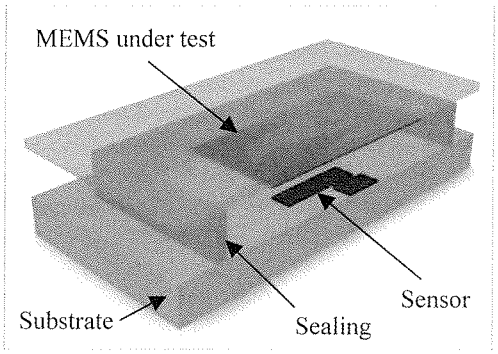


Fig. 8: Cavity monitoring thanks to additional sensor (MEMS).

Considering access to MEMS in the SiP, for both smart MEMS composed of significant digital processing and for simple analog sensor, the problem is equivalent to digital and mixed-signal die. As a result, the solutions are thus similar to those described earlier according to the nature of the electric signal to be accessed.

5 Conclusion

A system-in-package (SiP) is a packaged device comprised of two or more embedded bare dies and, in most cases, passive components. This technology has found many applications in recent years, providing system or sub-system solutions in a single package, using various types of carriers and interconnect technologies.

In this paper, we describe several emerging solutions to achieve the KGD target, based on advanced probing, alternate methods, and enhanced screening techniques. The test at system level is also addressed, from two different - but complementary - viewpoints, functional test and test access.

Currently, SiP is moving towards ever more sophisticated packaging technologies, which will require new test solutions. The trend towards more functionality combined with more communication features for emergent applications, such as healthcare, smart lighting, or ambient computing, drives the integration of a large variety of sensors and actuators. Consequently, very heterogeneous SiP implementations will be developed, posing new test challenges.

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P. Cauvet,
NXP Semiconductors, 2 Esplanade Anton Philips,
BP20000, 14906 Caen Cedex 9, France
philippe.cauvet@nxp.com, bernard@lirmm.fr

S. Bernard2 and M. Renovell
LIRMM, University of Montpellier / CNRS - 161 rue
Ada, 34392 Montpellier, France
renovell@lirmm.fr

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