FAST MOS TRANSISTOR MISMATCH OPTIMIZATION – A COMPARISON BETWEEN DIFFERENT APPROACHES

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Key words: MOS transistor mismatch, optimization, mismatch simulation, integrated circuits

Abstract: In this paper two different approaches for calculating the standard deviation of circuit performance measures caused by MOS transistor mismatch are presented. The short CPU time needed for mismatch evaluation makes it possible to include the proposed approaches in a circuit optimization loop as a criterion subject to optimization. Both mismatch evaluation methods were tested on four different circuits. The optimized circuits were compared to the circuits obtained from an optimization run where the list of criteria did not include mismatch. The results show that a significant reduction of standard deviations is obtained when mismatch evaluation is included in the optimization loop.

Hitra optimizacija neujemanja MOS tranzistorjev – primerjava različnih pristopov

Kjučne besede: neujemanje MOS tranzistorjev, optimizacija, simulacija neujemanja, integrirana vezja

Izvleček: V članku sta predstavljena dva različna pristopa za izračun standardnih deviacij lastnosti vezja, ki jih povzroča neujemanje identično načrtovanih MOS tranzistorjev. Glavna prednost opisanih pristopov je hiter izračun standardnih deviacij lastnosti vezja, ki so posledica neujemanja. To je ključnega pomena, če želimo posledice neujemanja vključiti v kriterijsko funkcijo optimizacijskega postopka. Oba pristopa sta bila preizkušena z optimizacijo štirih različnih vezij. Lastnosti tako dobljenih vezij smo primerjali z lastnostmi vezja dobljenega z optimizacijskim postopkom, ki ni vključeval učinkov neujemanja. Primerjava je pokazala, da je tovrstna vključitev neujemanja v optimizacijsko zanko smiselna, saj se standardna devicija lastnosti vezja občutno zmanjša.

1 Introduction

Mismatch is an effect that arises in IC fabrication and is a limiting factor of the accuracy and reliability of many analog integrated circuits. The main reason for mismatch is the stochastic nature of the fabrication process. Due to mismatch two equally designed transistors exhibit different electrical behaviour. Consequently the operating point and other circuit characteristics differ from their desired values. Mismatch can be divided into a systematic and a stochastic component. The systematic component is not considered in this paper because it can be reduced to great extend with proper layout /1/, /2/. The stochastic component is caused by random microscopic device architecture fluctuations. It can be reduced with better process control and larger transistor areas /3/, /4/. Most often the Gaussian distribution is used for modelling the stochastic variations of model parameters. The amount of mismatch can be expressed with standard deviation (σ) of transistor model parameters.

Mismatch can be modelled in many different ways /3/-/6/. Because of the limited availability of mismatch model parameters only some of them can be used for general purpose. One of the simplest models is the Pelgrom model (1) /3/.

$$\sigma(\Delta P) = \frac{A_P}{\sqrt{WL}} \tag{1}$$

In this model the standard deviation (σ) of the parameter difference (ΔP) between two identically drawn transistors depends on parameter A_P (which in turn is technology-dependent) and effective channel dimensions W and L. In the optimization runs presented in this paper we used (1) because it is simple and the technology-dependent parameters are available in the literature /7/. In /8/ it is shown that the model (1) is suitable for the 0,18µm technology. Due to the limited availability of mismatch parameters, this model is still frequently used for mismatch evaluation. In this paper two different methods of mismatch simulation are presented and tested on four different circuits.

Most commonly used transistor parameters in mismatch modelling (mismatch parameters) are threshold voltage (V_T) and current factor (β). The standard deviation of V_T and β can be expressed as

$$\sigma(\Delta V_T) = \frac{A_{V_T}}{\sqrt{WL}} \tag{2}$$

$$\sigma\left(\frac{\Delta\beta}{\beta}\right) = \frac{A_\beta}{\sqrt{WL}} \tag{3}$$

The technology dependant parameters A_{Vt} and A_β for different types of technologies are available in /7/.

2 Mismatch optimization

A robust circuit exhibits adequate performance in all corners. A corner defines a group of different process variations. The performance of the circuit is expressed with the cost function which is a sum of penalties /9/. Each measure has a goal and if the measured value deviates from this

goal, a penalty which is proportional to the violation, is added to the cost function. The goal is to minimize the cost function taking into account all corners. For this purpose the Constrained simplex /9/ optimization method has been used, which performs remarkably well on circuit optimization problems /10/.

To include mismatch in the optimization as yet another criterion, it has to be simulated first. The goal of mismatch simulation is to obtain a standard deviation of circuit properties caused by the stochastic nature of transistor model parameters. This standard deviation can be included in the cost function. In this paper two different approaches for mismatch simulation are presented. The first one is the sensitivity-based approach and the second one is the min-max approach. In both approaches a design of an operational amplifier will be used for better understanding. Consider an operational amplifier where a designer is interested in the standard deviation of the output voltage caused by the stochastic nature of the transistor model parameters. Beside the offset voltage performance measures like swing at gain, bandwidth, phase margin, etc. are also important in the design process. All these performance measures are circuit properties but only offset voltage is relevant for mismatch analysis.

2.1 Sensitivity-based approach

The sensitivity-based approach assumes that mismatch parameters are not correlated and that the changes caused by the stochastic nature of model parameters are within the bounds where the circuit behaves linearly. The evaluation of the standard deviations of the circuit properties can be divided in three major steps:

Step 1: Calculate the standard deviation of every relevant transistor parameter (mismatch parameter).

Step 2: Calculate the sensitivity of circuit properties to all mismatch parameters.

Step 3: Calculate the approximated standard deviation of the circuit property.

In a circuit composed of k MOS transistors only $n \leq k$ MOS transistors are relevant to the mismatch analysis. $m=2 \cdot n$ standard deviations must be calculated (n standard deviations for the threshold voltages and n standard deviation for the current factors). The remains k-n MOS transistors belong usually to the start up circuit or power down control.

In step 2 the sensitivity (α) of a circuit property P_X (in our example this is the output offset voltage) to every mismatch parameter is calculated. The sensitivity indicates how much the variation of a mismatch parameter affects circuit property P_X. The sensitivity is calculated using the perturbation approach (4)

$$\alpha_i = \frac{P_X(\delta_i) - P_X(0)}{\delta_i} \qquad i = 1,\ldots,m \qquad (4)$$

Where $P_X(0)$ is the value of the circuit property when all mismatch parameters are set to their nominal values while the $P_X(\delta_i)$ is the value of the circuit property when one mismatch parameter is perturbed. The perturbed value (for example V_T) is the sum of the nominal value and one standard deviation ($\delta_i = V_T + \sigma(\Delta V_T)$) of the respective mismatch parameter.

Assuming that mismatch parameters are uncorrelated the standard deviation of a circuit property can be expressed as:

$$\sigma^2(P_X) = \sum_{i=1}^{m} \alpha_i^2 \cdot \sigma_i^2 \qquad (5)$$

The sensitivity-based approach requires $m+1$ circuit simulations to calculate the sensitivities. One simulation is needed for the nominal mismatch parameter values and m simulations are needed for the perturbed circuits.

2.2 Min-Max approach

With this approach we estimate the extreme value of a circuit property P. We assume P has an extreme when all mismatch parameters are at their extreme values. This is true if P is a monotonic function of the mismatch parameters. Which extreme value ($+\sigma$ or $-\sigma$) a mismatch parameter should take in order for P to take its extreme value depend on the sensitivity. Just like with the sensitivity-based approach we assume that mismatch parameters are not correlated. Once the upper (max) and lower (min) extreme of P are obtained, the upper bound on the standard deviation of the circuit property can be calculated. The min-max approach can be divided in 4 steps.

Step 1: Calculate the standard deviation of every mismatch parameter.

Step 2: Obtain the signs of the sensitivities to all mismatch parameters.

Step 3: Measure the extreme (min and max) values.

Step 4: Calculate the upper bound on the standard deviation.

Step 1 and step 2 are very similar to the corresponding steps in the sensitivity-based approach. To obtain the signs of the sensitivities $m+1$ simulations are necessary (m is the number of mismatch parameters). In step 3 the extreme values of the circuit properties are calculated. This is done using two simulations per circuit property (one for the upper and one for the lower extreme). To measure the upper extreme (P_{max}) we increase (or decrease) the value of every mismatch parameter by one standard deviation if the sensitivity is positive (if the sensitivity is negative). The same is done for the lower extreme (P_{min}), except that the reasoning is opposite. For positive sensitivity the value of the mismatch parameter is decreased and for negative sensitivity it is increased. In step 4 the upper bound on the standard deviation can now be calculated (6).

$$\sigma(P_X) \leq M_\sigma(P_X) = \left| \frac{P_{\max} - P_{\min}}{2} \right| \qquad (6)$$

3 Examples

The proposed approaches for mismatch evaluation were included in the optimization loop and the obtained results were compared with the results of the optimization run without mismatch evaluation. The comparison was done on four different circuits:

- Bandgap reference circuit (BGR)
- Operational amplifier (OPA)
- Beta multiplier reference circuit (BMR)
- Comparator (COMP)

The first optimization run (A) considers only performance measures, while the second and the third run (B, C) include mismatch. In the second run (B) the sensitivity-based approach is used for evaluating the mismatch and in the third run (C) the min-max approach is used. All circuits in this paper have been simulated using the SPICE OPUS simulator and the BSIM3 model of a 0,18 µm process technology. To obtain robust circuits every circuit has been simulated in three different corners. Every corner was described with the corresponding temperature, supply voltage, MOS transconductance, etc.

3.1 Bandgap reference (BGR)

A stable voltage reference is very important in many circuits. A bandgap voltage reference (BGR) is capable of providing a voltage almost independent of temperature and supply voltage fluctuations. In this paper we optimized a 1-V low power CMOS bandgap reference based on resistive subdivision (Figure 1) which is in detail described in /11/.

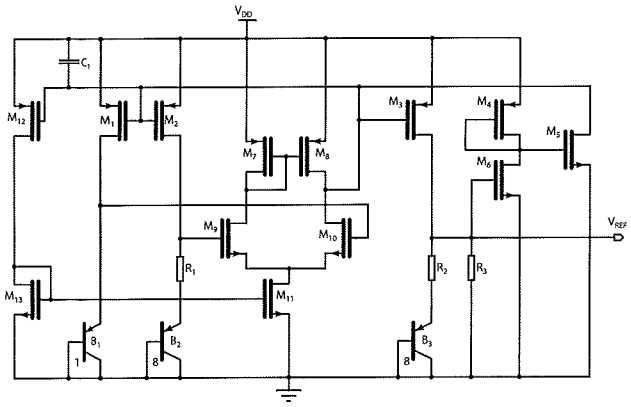

Fig 1: Bandgap voltage reference (BGR)

It is known that sample to sample variations (mismatch) are larger than the variations caused by the temperature or supply voltage fluctuation. Therefore mismatch is a dominating factor determining the absolute accuracy of the bandgap reference circuit /11/.

The optimization parameters were the three resistances (R_1-R_3) and the channel dimensions (width and length) of all MOS transistor except transistors M_4-M_6 which constitute the start up circuit. The list of performance measures and parameters was the same for all of the three optimization runs. The cost function was composed of the following performance measures:

- output voltage change when the temperature varies from -20°C to 50°C,
- output voltage change when the supply voltage varies from 1V to 1,6V,
- circuit area,
- standard deviation of the output voltage caused by mismatch.

Table 1 lists the results of the optimization. The first and the second column contains the names and the desired values of the performance measures while the others list the results of optimization runs A, B and C. The standard deviation σ (V_{REF}) is calculated from 1000 Monte Carlo simulations.

Table 1: Comparison of three different optimization runs (BGR-circuit)

		Desired value	Optimization processes		
			BGR-A	BGR-B	BGR-C
Perf. Meas.	Max (dV_{REF}/dV_{DD}) [mV/V]	< 4	1,80	3,04	3,39
	Max (dV_{REF}/dT) [mV/°]	< 0,15	0,15	0,15	0,14
	Area [µm²]	< 6000	3521	5996	5985
	σ (V_{REF}) [mV]	< 7	**16,2**	**7,05**	**6,67**

It can clearly be seen that including mismatch effects in the cost function results in the enlargement of the transistors area and the reduction of the reference voltage variation caused by mismatch. The maximal reference voltage slope with respect to the supply voltage increases, while the maximal slope with respects to the temperature remains almost unchanged. Despite the large reduction of the standard deviation (more than 2 times) all the results are still within the specified bounds. Figure 2 shows 30 Monte Carlo simulations of the circuit obtained from run A where mismatch was neglected. If we compare this figure to figure 3 where the results of run B are plotted the reduction of the standard deviation is clearly visible.

3.2 Operational amplifier (OPA)

The operational amplifier is one of the fundamental building blocks of analog integrated circuits. Due to mismatch an operational amplifier exhibits a random offset voltage. In this paper the operational amplifier from figure 4 was optimized.

The optimization parameters were the capacitance of the capacitor and the channel dimensions (width and length) of all transistors except M_{N1S} and M_{P1S}, which are used for shutting down the amplifier. All performance measures and their goals (desired value) are listed in table 2. The standard deviation $\sigma(V_{OUT})$ is calculated from 1000 Monte-Carlo simulations.

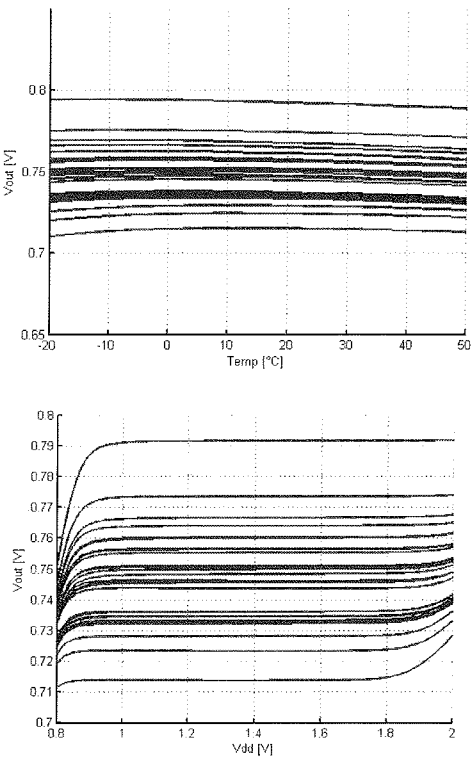

Fig 2: Variation of the BGR output voltage with respect to the temperature and the supply voltage when mismatch is not included in the optimization loop (30 samples).

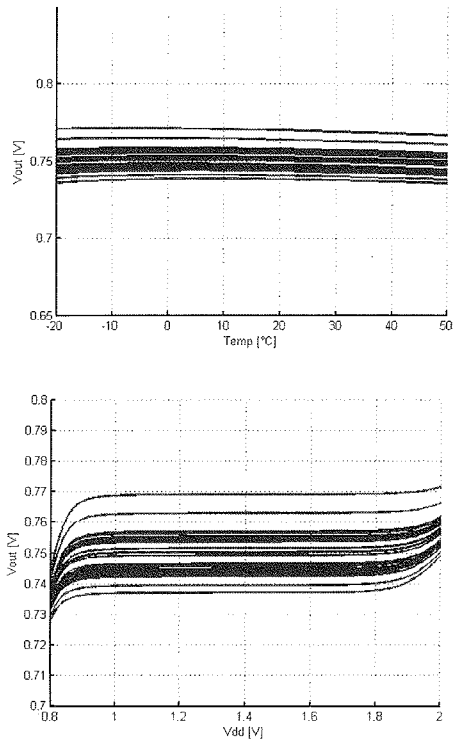

Fig 3: Variation of the BGR output voltage with respect to the temperature and the supply voltage when mismatch is included in the optimization loop (30 samples).

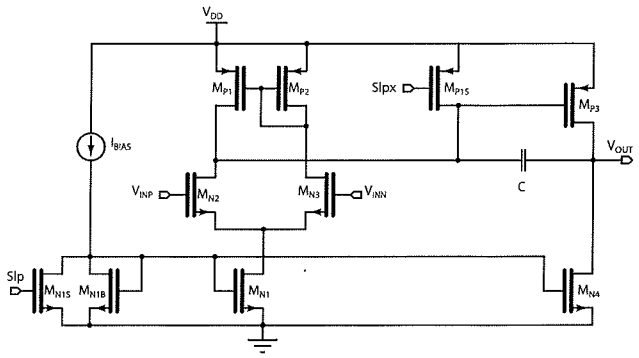

Fig 4: Operational amplifer (OPA)

Table 2: Comparison of three different optimization runs (OPA-circuit)

		Desired value	Optimization processes		
			OPA-A	OPA-B	OPA-C
Perf. measures	Swing at gain [V]	> 2	2,58	2,24	2,18
	Phase margin [°]	> 45	61,8	65,7	67,2
	Unity gain b.w. [MHz]	>18	32,7	20,3	43,1
	Gain [dB]	> 70	72,1	83,5	85,3
	Area [μm²]	< 250	233,8	249,7	249,8
	σ (V_{OUT}) [mV]	< 1,8	**4,44**	**1,87**	**1,70**

The results of the three optimization runs are listed in table 2. We can see that for the circuit obtained from the first run (without mismatch) the output voltage has a standard deviation of 4,44 mV (offset). Both optimization runs that included mismatch produced better results. In runs B and C the standard deviation of the output voltage was reduced by a factor of 2,3 or more. Most of the remaining performance measures stayed within the desired range.

3.3 Beta-multiplier reference (BMR)

The Beta-multiplier circuit is used for providing a stable and temperature independent current reference for a whole range of circuits like operational amplifiers, comparators, etc. It can also be used as a voltage reference circuit.

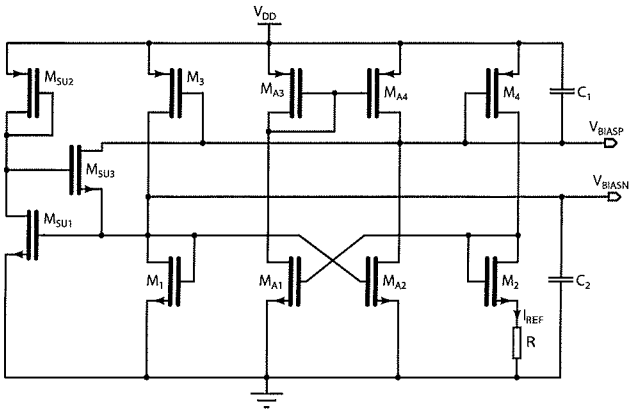

Fig 5: Beta multiplier reference (BMR)

The circuit in figure 5 can provide a stable current (I_{REF}) that flows through resistance R. This current is fairly stable with respect to temperature and supply voltage variations.

One can mirror the reference current using gate voltages V_{BIASP} and V_{BIASN}. The optimization goals were to minimize the variation of the current caused by the change of temperature and supply voltage. The optimization parameters were the resistance R and channel dimensions of all transistors except transistors that constitute the start up circuit (M_{SU1}, M_{SU2}, M_{SU3}). The results of the three optimization runs are listed in table 3. The standard deviation $\sigma(I_{REF})$ is calculated from 1000 Monte Carlo simulations.

Table 3: Comparison of three different optimization runs (BMR-circuit)

		Desired value	Optimization processes		
			BMR-A	BMR-B	BMR-C
Perf Meas	Max (dI_{REG}/dV_{DD}) [µA /V]	< 0,4	0,31	0,30	0,49
	Max (dI_{REG}/dT) [µA /°]	< 0,06	0,047	0,053	0,060
	I_{REG} [µA]	= 20	19,9	20,0	20,0
	Area [µm^2]	< 500	490	497	513
	σ (I_{REG}) [µA]	< 1	**3,45**	**0,99**	**0,53**

The first two performance measures (dI_{REG}/dV_{DD} and dI_{REG}/dT) provide the information on the output current maximum variation with respect to the supply voltage and temperature variations. The third measure is the value of the reference current while the last two are the circuit area and the standard deviation of the reference current caused by mismatch. From table 3 it can clearly be seen that the standard deviation ($\sigma(I_{REG})$) from runs B and C (where mismatch was included in the cost function) is more than 3 times smaller than the one obtained in run A. All the design requirements are fulfilled except the area in run C where a small goal violation occurs. The standard deviation obtained in run C is nearly two times smaller then the goal. The reason is that min-max approach calculates the maximum value of the standard deviation, which is in this example 2 to 3 times bigger than the real standard deviation (see table 5). Due to this the weight of this performance measure is effectively bigger than the weight of the circuit area.

3.4 Comparator (COMP)

The comparator from Figure 6 is a decision-making circuit. The output voltage (V_{out}) switches from 0V to V_{dd} when V_{INP} is greater than V_{INN}. The output switches back to 0V when V_{INP} becomes smaller than V_{INN}. The output does not switch instantly when the difference V_{INP}-V_{INN} changes sign meaning that there is some hysteresis present in the circuit. Mismatch causes that the width of the hysteresis to vary randomly. The optimization run which includes mismatch attempts to remove the variation of hysteresis.

The optimization parameters were the channel dimensions of all transistors. The results of the optimization runs are listed in table 4.

The first performance measure (Delay time LH) measures the time form the moment when V_{INP} crosses V_{INN} and the moment when V_{OUT} reaches 90% of the difference between the initial and the final value. The second measure (Delay time HL) is the same as previous with the difference that

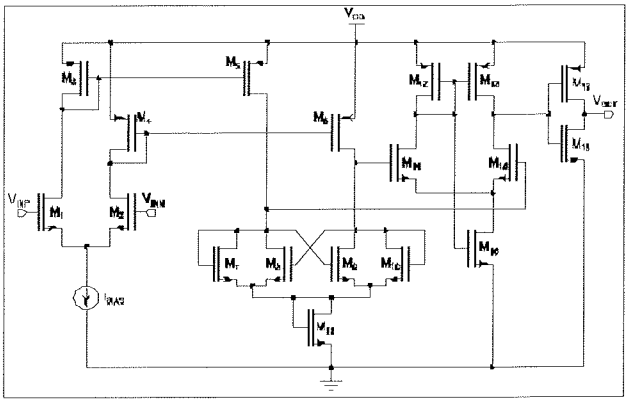

Fig 6: Comparator (COMP)

Table 4: Comparison of three different optimization runs (COMP-circuit)

		Desired value	Optimization processes		
			COMP-A	COMP-B	COMP-C
Perf. measures	Delay time LH [ns]	< 5	3,68	4,94	5,80
	Delay time HL [ns]	< 5	3,87	3,38	4,66
	Rise time [ns]	< 0,3	0,17	0,13	0,11
	Fall time [ns]	< 0,3	0,18	0,18	0,26
	Hysteresis [mV]	< 1	0,83	0,56	1,95
	Positive slope [mV]	< 1	0,93	0,46	0,40
	Negative slope [mV]	< 1	0,51	0,46	0,40
	Overshoot [mV]	< 50	13,7	6,18	8,26
	Undershoot [mV]	< 50	6,63	8,52	4,18
	Area [µm]	< 90	85,4	89,5	88,1
	σ (V_{HIST}) [mV]	< 5	**10,2**	**5,29**	**4,50**

the falling edge of V_{OUT} is measured (when V_{OUT} reaches 10% of the difference between the initial and final value). The rise time is the time needed for the output to rise from 10% to 90% of the difference and the fall time is measured between the points where the output crosses the 90% and 10% level of the difference. The fifth measure is the width of the hysteresis, while the last two measures provide the slope of the hysteresis. From the results it can be seen that almost all the design requirements are fulfilled and that the standard deviation of the hysteresis is reduced to half if mismatch is considered in the optimization run.

3.5 Comparison of the approaches for mismatch evaluation

In table 5 the standard deviations of the circuit properties affected by mismatch are listed for all four circuits. For every circuit the computational effort of the mismatch evaluation has been calculated for all three methods: Monte-Carlo, sensitivity-based approach and min-max approach.

Table 5 shows that the mismatch effect calculated with the sensitivity-based approach is close to the value obtained from 1000 Monte Carlo simulations. The min-max approach overestimates the mismatch. This can also be seen from table 5. Typically the min-max approach results in 2 to 4 times larger values than Monte-Carlo analysis. The main difference between the two presented approaches and Monte-Carlo approach is the number of simulations need-

Table 5: Comparison between of different approaches for mismatch evaluation

	Monte Carlo Approach	Sensitivity-Based Approach	Min-Max Approach
BGR-A [mV]	16,2	16,3	43,6
BGR-B [mV]	7,05	7,04	19,3
BGR-C [mV]	6,67	6,71	17,5
OPA-A [mV]	4,45	4,40	9,59
OPA-B [mV]	1,87	1,87	4,49
OPA-C [mV]	1,70	1,71	4,03
BMR-A [µA]	3,45	3,39	7,53
BMR-B [µA]	0,99	0,99	2,71
BMR-C [µA]	0,53	0,52	1,64
COMP-A [mV]	10,2	9,59	34,8
COMP-B [mV]	5,29	4,99	19,9
COMP-C [mV]	4,50	5,57	12,5

ed to evaluate the standard deviation of a circuit property. To obtain the actual value of the standard deviation of a circuit property 1000 or more Monte-Carlo simulations are needed. The sensitivity-based approach is significantly faster since it needs only $m+1$ simulations (where m is the number of mismatch parameters) to obtain similar values as Monte-Carlo approach. The min-max approach also gives satisfying results with only $m+3$ simulations.

4 Conclusion

With the reduction of transistor dimensions the mismatch is becoming the dominating factor of the accuracy of many analog circuits. In the examples it was shown how mismatch can be included in circuit optimization. Two different ways of mismatch evaluation were presented. The sensitivity-based approach returns more realistic values while on the other hand the min-max approach results in the upper (lower) bound of a circuit performance measures. Optimization runs using these two methods have been conducted on four different circuits and the results were compared to the results of an optimization run where mismatch was neglected. The comparison shows that significant improvements of circuit performance can be achieved. Both optimization runs where mismatch was included resulted in circuits that exhibited similar performance.

5 Acknowledgment

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