SINGLE ELECTRON FAULT MODELING IN QCA DEVICES

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Abstract: Quantum Cellular Automata (QCA) represents an emerging technology at the nanotechnology level. There are various faults which may occur in QCA cells. One of these faults is the Single Electron Fault (SEF) that can happen during manufacturing or operation of QCA circuits. The behavior of single electron fault in QCA devices is not similar to either previously investigated faults or conventional CMOS logic. A detailed simulation based logic level modeling of Single Electron Fault for QCA basic logic devices is represented in this paper.

Modeliranje napake SEF pri delovanju component QCA

Kjučne besede: QCA, napaka SEF

Izvleček: QCA (Quantum Cellular Automata) predstavlja prihajajočo tehnologijo na nanotehnološkem nivoju. Obstaja veliko različnih napak, ki se lahko pojavijo v QCA celicah. Ena izmed teh je napaka enega elektrona (Single Electron Fault-SEF), ki se lahko pripeti med izdelavo ali delovanjem QCA vezij. Obnašanje SEF v QCA vezjih ni enako nobeni preje obravnavani napaki v konvencionalni CMOS logiki. V prispevku obravnavamo natančno logično simulacijo pojava SEF v QCA vezjih.

1. Introduction

The microelectronics industry has improved the integration, the power consumption, and the speed of integrated circuits during past several decades by means of reducing the feature size of transistors. But it seems that even by decreasing the transistor sizes, some problems such as power consumption can't be ignored. Utilizing the QCA technology for implementing logic circuits is one of the approaches which in addition to decreasing the size of logic circuits and increasing the clock frequency of these circuits, reduces the power consumption of these circuits. QCA, which was first introduced by Lent et al. /1/, represents an emerging technology at the nanotechnology level. QCA cells have quantum dots, in which the position of electrons will determine the binary levels of 0 and 1.

Various types of cell misplacement faults may occur during fabrication and manufacturing of QCA devices and circuits. Some of them which have been characterized are *cell displacement*, *cell misalignment*, *cell omission* and *cell rotation* /2-7/.

- A *cell displacement* is a defect in which the defective cell is misplaced from its original direction.
- A *cell misalignment* is a defect in which the direction of the defective cell is not properly aligned.
- A *cell omission* is a defect in which a particular cell is missing compared to the original.
- A *cell rotation* is a defect in which the defective cell is rotated in its location.

There are some other faults, such as missing or extra dots or/and electrons which may occur in QCA devices and circuits /2, 3/. Single event effects (SEE) are an example of such phenomena which can affect QCA devices and circuits. These types of effects can cause electrons to tunnel outside or inside QCA cells, and therefore some remaining QCA cells may contain zero, one, two, three, four or more electrons. This is the main defect caused by SEEs which may occur for QCA devices and circuits. Considering the QCA structure with two electrons in each cell, we can conclude that defected cells may lead to circuit malfunctioning /8/.

The main goal of this paper is to model and characterize the single electron fault in QCA devices. We will investigate the effects of faulty cell in binary wire, inverter chain, inverter gate, and majority gate.

The remainder of this paper is as follows. In Section II, a brief review of QCA is presented. In Section III, the effects of single electron fault on QCA devices are investigated. Finally, Section IV will conclude this paper.

2. QCA Review

In Quantum Cellular Automata (QCA), a cell contains four quantum dots, as schematically shown in Fig. 1. The quantum dots are shown as the open circles which represent the confining electronic potential. Each cell is occupied by two electrons which are schematically shown as the solid dots.

In a cell, the electrons are allowed to jump between the individual quantum dots by the mechanism of quantum mechanical tunneling but they are not allowed to tunnel between cells. The barriers between cells are assumed sufficient to completely suppress intercellular tunneling.

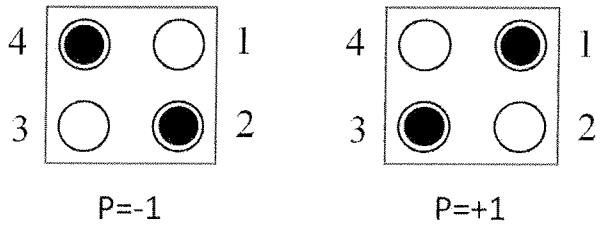

Fig. 1. QCA cell and its ground states

If they are left alone, they will meet the configuration corresponding to the physical ground state of the cell. It is in an obvious manner that the two electrons will tend to occupy different dots because of the Coulombic force associated with bringing them together in close proximity on the same dot.

By these concepts, it's concluded that the ground state of the system will be an equal superposition of the two basic configurations with electrons at opposite corners, as shown in Fig. 1. The positions of the electrons are also shown in this figure.

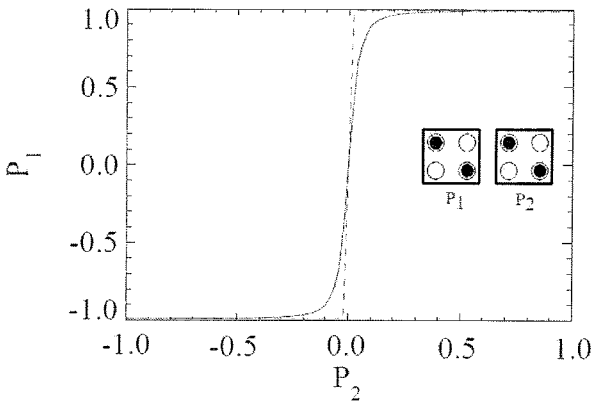

Fig. 2. Coupling of QCA cells

Coupling between the two cells is provided by the Coulomb interaction between electrons in different cells. Fig. 2 shows how one cell is affected by the state of its neighbor /10/. This figure shows the two cells where the polarization of cell 1 (P1) is determined by the polarization of its neighbor (P2). P2 is assumed to be fixed at a given value, corresponding to a specific arrangement of charges in cell 2 and this charge distribution exerts its influence on cell 1, thus determining its polarization. The result which can be drawn here is the strongly non-linear nature of the cell-cell coupling. Cell 1 is almost completely polarized even though cell 2 might only be partially and not completely polarized /9, 10/.

The physical interactions between cells may be used to realize elementary Boolean logic functions. The basic logic gates in QCA are the Majority logic function and the Inverter which are illustrated in Fig. 4(a) and Fig. 3, respectively. The Majority logic function can be realized by only 5 QCA cells /11/.

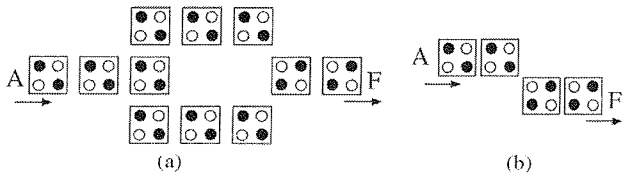

Fig. 3. (a) Redundant inverter gate, (b) Inverter gate

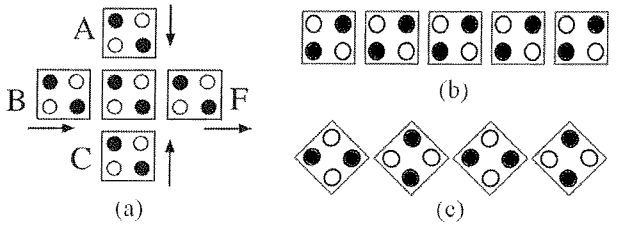

Fig. 4. (a) Majority logic gate, (b) Binary wire, (c) Inverter chain

The logic AND function can be implemented by a Majority logic function by setting one of its inputs permanently to 0 and the logic OR function can be implemented by a Majority logic function by setting one of its inputs permanently to 1.

QCA clocking provides a mechanism for synchronizing information flow through the circuit. It should be considered that the clock also controls the direction of information flow in a QCA circuit. The QCA clock also provides the power required for circuit operation. More precisely, the QCA clock is used to control the tunneling barrier height in cells. When the clock is low, the electrons are trapped in their associated positions and can't tunnel to other dots, therefore latching the cell (Hold phase). This is caused by the intracellular barriers which are held at their maximum height. When the clock signal is high, the cell goes to the null polarization state (Relax phase). This is caused by the intracellular barriers which are held at their minimum height. Between these two cases, the cells are either releasing or switching.

Fig. 5 shows the barrier height in four phases of clock. Each cell in a particular clocking zone is connected to one of the four available phases of the QCA clock shown in Fig. 6. Each cell in the zone is latched and unlatched in synchronization with the changing clock signal and therefore the information is propagated through cells /12-15/.

3. Single Electron Fault Modeling

In this Section, fault modeling will be accomplished for QCA wires, inverter, and majority gates. All cells are assumed to have a length and width of 18 nm and quantum dots are 5 nm in diameter. The center to center distance of two neighbor cells is 20 nm. Thus, the cell size can be defined as 20 nm. As an assumption, a 20 nm cell size was used in /16/ and a 25 nm cell size was used in /5/. Thus, the 20

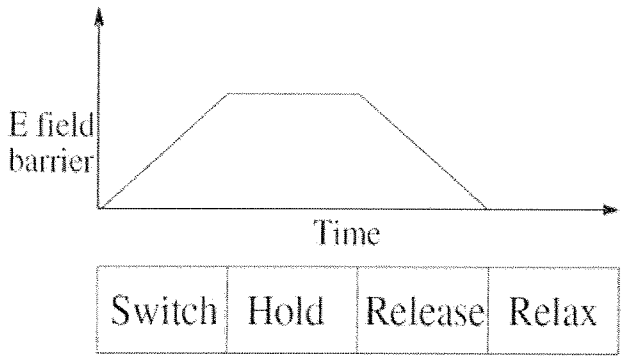

Fig. 5. Barrier height in four phases of clock

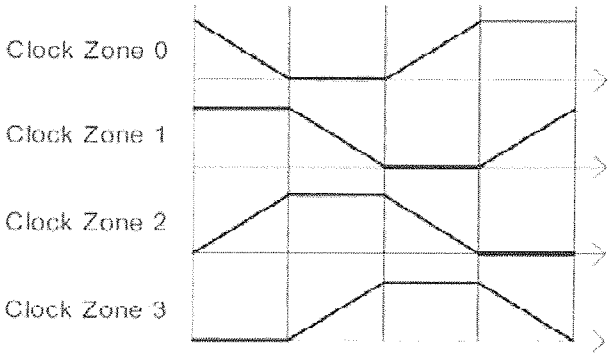

Fig. 6. QCA clock zones

nm assumption is valid for QCA cells. The center to center distance of two neighbor quantum dot in a QCA cell is 9 nm (For example, dot1 and dot2 in Fig. 1). According to previous definitions, other geometric distances are calculated. As an example, considering two neighbor cells, the distance between dot4 in the left cell and dot1 in the right cell is 29 nm and so on. Also it is assumed that each cell is assigned to an individual clock zone and there are no neighbor cells with the same clock zone. Positions of electrons and polarization of cells are obtained from the fact of the least Kink energy. It means that all possible configurations are considered and the Kink energy is calculated for each configuration. Configuration with the least Kink energy is the most stable configuration. The Kink energy can be computed by the following equation.

$$E_{i,j} = \frac{q_i q_j}{4\pi\varepsilon_0\varepsilon_r\left|r_i - r_j\right|} \quad (1)$$

All following simulations i.e. calculating the Kink energy (electron-volt) are accomplished by MATLAB software /17/.

3.1. Fault Modeling for QCA Wires

There are two types of wires in QCA technology, binary wire and inverter chain (Fig. 4(b, c)). We have investigated the single electron fault for these two types of wire and modeled the fault for them. Binary wire will be discussed in this subsection and inverter chain will be discussed in the next.

Two major questions should be answered for a binary wire which contains a faulty cell:

- Considering the faulty cell, where should its single electron go if the previous cell has the polarization of zero or one?
- Considering the faulty cell, which polarization shall be dictated to its next cell?

For the first case, simulation results show that if a cell is faulty and its previous cell has the polarization of zero, the single electron will go to position number 1 and if its previous cell has the polarization of one, the single electron will go to position number 2. The Kink energy is computed for each position and the position with the least Kink energy is considered to be the target position. The kink energy of each position is illustrated in Table 1.

Table 1 Kink energy for positions of electron in a faulty cell in binary wire according to its previous cell polarization

Prev. Cell Pol.	Position 1	Position 2	Position 3	Position 4
Zero	**0.0089309**	0.0092492	0.015224	0.013423
One	0.0092492	**0.0089309**	0.013423	0.015224

For the second case, simulation results show that if a cell is faulty and its electron is in positions of 1, 2, 3 or 4, the next cell will obtain the polarization of one, zero, zero and one correspondingly. The Kink energy is computed for each polarization and the polarization with the least Kink energy is considered to be the target polarization. The kink energy of each polarization is illustrated in Table II. It can be concluded from Table I that positions of 3 and 4 cannot be occupied by single electron in a faulty cell. But in order to have a complete simulation result, they are considered as occupied positions in Table 2.

Table 2 Kink energy for polarization of next cell in binary wire according to the position of electron in faulty cell

Faulty Cell Position	Next Cell Polarization Zero	Next Cell Polarization One
Position 1	0.015224	**0.013423**
Position 2	**0.013423**	0.015224
Position 3	**0.0089309**	0.0092492
Position 4	0.0092492	**0.0089309**

Fig. 7 illustrates the faulty cell effect on a binary wire. As illustrated in Fig. 7(a), if the left side cell has the logic value of zero, the faulty cell will have its electron in position 1 and the right side cell will obtain the logic value of one and as illustrated in the Fig. 7(b), if the left side cell has the logic value of one, the faulty cell will have its electron in position 2 and the right side cell will obtain the logic value of zero. According to simulation results, if a single electron fault occurs in a binary wire, the logic value of that wire will be inverted.

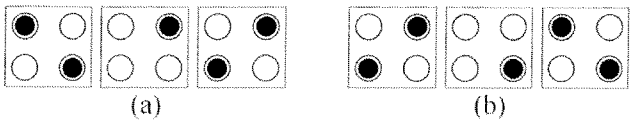

Fig. 7. Faulty cell effect on binary wire

3.2. Fault Modeling for QCA Inverter Gate

In this section we will discuss the inverter gate or inverter chain and also redundant inverter gate of Fig. 3(a) which has two inverters in parallel.

Two previous questions for an inverter chain containing a faulty cell should be addressed.

For the first case, simulation results show that if a cell is faulty and its previous cell has the polarization of zero, the single electron will go to position number 2 and if its previous cell has the polarization of one, again the single electron will go to position number 2. The Kink energy is computed for each position and the position with the least Kink energy is figured out to be the target position. The kink energy of each position is illustrated in Table 3.

Table 3 Kink energy for positions of electron in a faulty cell in inverter chain according to its previous cell polarization

Prev. Cell Pol.	Position 1	Position 2	Position 3	Position 4
Zero	0.0080519	**0.0066624**	0.0080519	0.011112
One	0.0075388	**0.0063317**	0.0075388	0.0097721

For the second case, simulation results show that if a cell is faulty and its electron is in positions of 1, 2, 3 or 4, the next cell will obtain the polarization of one. It means that the output is stuck at one. The Kink energy is computed for each polarization and the polarization with the least Kink energy is figured out to be the target polarization. The kink energy of each polarization is illustrated in Table 4.

Table 4 Kink energy for polarization of next cell in inverter chain according to the position of electron in faulty cell

Faulty Cell Position	Next Cell Polarization Zero	Next Cell Polarization One
Position 1	0.0080519	**0.0075388**
Position 2	0.011112	**0.0097721**
Position 3	0.0080519	**0.0075388**
Position 4	0.0066624	**0.0063317**

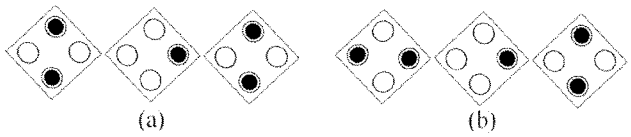

Fig. 8. Faulty cell effect on inverter chain

Fig. 8 illustrates the faulty cell effect on inverter chain. As illustrated in Fig. 8 (a), if the left side cell has the logic value of one, the faulty cell will have its electron in position 2 and the right side cell will obtain the logic value of one and as illustrated in Fig. 8 (b), if the left side cell has the logic value of zero, the faulty cell will have its electron in position 2 and the right side cell will obtain the logic value of one. According to simulation results, if a single electron fault occurs in an inverter chain, the logic value of that wire will be stuck at one.

Considering the redundant inverter gate, the fault may occur on 3 cells which are two right most cells on up and down input wires and a cell which is at the diagonal neighborhood of these two cells. Occurrence of the fault on other cells of redundant inverter gate may be treated as binary wire fault. Also two previously mentioned questions for the redundant inverter gate should be answered.

Table 5 Kink energy for positions of electron in a faulty cell in redundant inverter gate according to its previous cells polarization

Prev. Cell Pol.	Position 1	Position 2	Position 3	Position 4
Zero	0.014384	**0.014201**	0.017824	0.018651
One	**0.014201**	0.014384	0.018651	0.017824

First, the single diagonal neighbor cell will be investigated. For the first case, simulation results show that if this cell is faulty and its previous up and down cells have the polarization of zero, the single electron will go to position number 2 and if its previous cells have the polarization of one, the single electron will go to position number 1. The Kink energy is computed for each position and the position with the least Kink energy is figured out to be the target position. The kink energy of each position is illustrated in Table 5. Second case of fault modeling for this cell is similar to binary wire.

Fig. 9 illustrates the output faulty cell effect on redundant inverter gate. Simulation results show that the redundant inverter gate will act as a wire in presence of single electron fault in the output cell, i.e. the single diagonal neighbor cell.

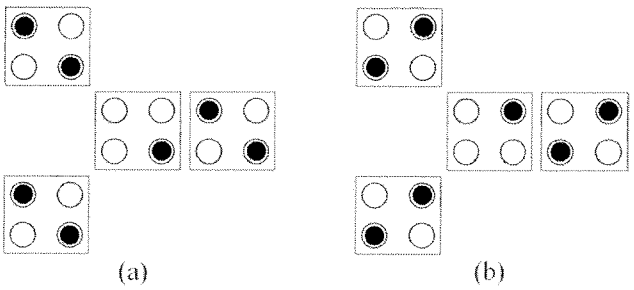

Fig. 9. Output faulty cell effect on redundant inverter gate

There are also two cases for two right most cells on up and down wires. The first case is like binary wire but for the sec-

ond case, simulation results show that if the cell in the up position is faulty, the next cell, i.e. the diagonal neighbor cell, will be stuck at zero and if the cell in the down position is faulty, the next cell, i.e. the diagonal neighbor cell, will be stuck at one. The Kink energy is computed for each polarization and the polarization with the least Kink energy is figured out to be the target polarization. The kink energy of each polarization is illustrated in Table 6. Fig. 10 illustrates the up input faulty cell effect on redundant inverter gate.

Table 6 Kink energy for polarization of next cell in redundant inverter gate according to the faulty cell in up or down input position

Input Polarization and Faulty Input	**Next Cell Polarization Zero**	**Next Cell Polarization One**
Zero and Up	**0.02313**	0.023643
One and Up	**0.027216**	0.027547
Zero and Down	0.027547	**0.027216**
One and Down	0.023643	**0.02313**

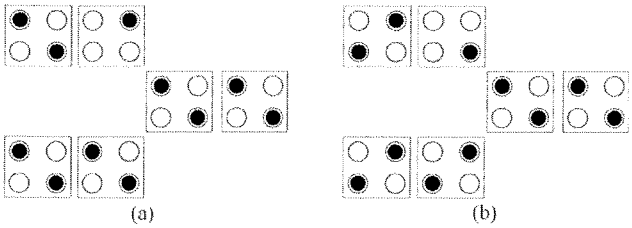

Fig. 10. Up input faulty cell effect on redundant inverter gate

3.3. Fault Modeling for QCA Majority Gate

To model the single electron fault in majority gate, we have exhaustively simulated this gate and the fault effect of each of its four cells, i.e. input A, input B, input C, and central cell was investigated for every input vector. If the fault occurs on output cell, it can be treated as a wire between central cell and output cell.

As an example of simulation, the computed Kink energy and the position of electron in faulty central cell of majority gate are listed in Table 7. Again the least Kink energy will introduce the target position. All faulty states in presence of the faulty central cell are illustrated in Fig. 11.

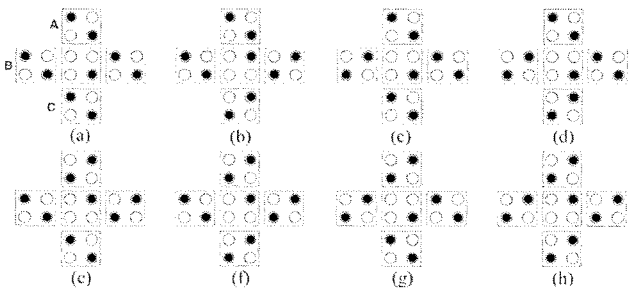

Fig. 11. Faulty states of majority gate in presence of the faulty central cell

Table 7 Kink energy for positions of electron in faulty central cell of majority gate

Input ABC	Position 1	Position 2	Position 3	Position 4
000	0.033086	**0.031922**	0.039379	0.036096
001	**0.033404**	0.033722	0.037578	0.035777
010	0.033404	**0.031603**	0.037578	0.037896
011	0.033722	**0.033404**	0.035777	0.037578
100	**0.031285**	0.031603	0.039697	0.037896
101	**0.031603**	0.033404	0.037896	0.037578
110	0.031603	**0.031285**	0.037896	0.039697
111	**0.031922**	0.033086	0.036096	0.039379

Output Simulation results are shown in Table 8. Like other gates, here we computed the Kink energy for finding the output of the majority gate.

Table 8 Desired output of the majority gate and computed output in presence of single electron fault

Input ABC	Output for Faulty A	Output for Faulty B	Output for Faulty C	Output for Faulty Cent.	Desired Output
000	0	0	0	0	0
001	1	1	0	1	0
010	1	0	1	0	0
011	1	0	0	0	1
100	0	1	1	1	0
101	0	1	0	1	1
110	0	0	1	0	1
111	1	1	1	1	1

Looking more precisely at the simulation results, we can conclude that if a fault occurs on an input, the output will change its functionality to majority of other inputs and inverse of faulty input. Occurrence of the fault on central input is equivalent to occurrence of the fault on B input.

4. Conclusion

A detailed modeling and characterization of single electron fault for QCA basic logic devices has been represented in this paper. As stated before, the behavior of single electron fault in QCA devices is not similar to either previously investigated faults or conventional CMOS logic. For example, stuck at zero or stuck at one fault model in redundant inverter gate is based on the input on which the fault occurs.

Our results show that if a single electron fault occurs in a binary wire, the logic value of that wire will be inverted. If the mentioned fault occurs in an inverter chain or a Not gate, the output will be stuck at one. If this fault occurs on the output of redundant inverter gate, the function of this gate will be inverted and it acts as a wire. Occurrence of the single electron fault on the right most cells of up and down wires of redundant inverter gate will lead to the output getting stuck at zero and one respectively. Single electron fault on the central cell of majority gate will change the

majority output to majority of vertical inputs and inversed horizontal input. Occurrence of this fault on each input of majority gate will change the output to be the majority of other inputs and the inverse of this faulty input.

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