A FLASH INTERPOLATOR ASIC WITH BUILD-IN AMPLITUDE MEASUREMENT CIRCUIT

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Key words: Interpolation, amplitude measurement, orthogonal signals, flash interpolator, automatic gain control, encoder.

Abstract: A flash interpolation circuit converts a pair of periodic and orthogonal sine-signals into a stream of periodic - phase shifted sinusoidal signals, the amplitudes of which can be combined to produce useful information about the peak amplitude of the input sine-signals, independently of the signal's frequency. An interpolation factor of 4 is shown to be sufficient for measuring amplitudes with an accuracy of 5.8 %.

The interpolator architecture, combined with an amplitude measuring system, has been designed, integrated as a part of the interpolator ASIC, evaluated and analyzed. The ASIC is designed and processed in 0.35 ěm CMOS technology.

Bliskovni interpolator z vgrajenim merilnikom amplitude

Kjučne besede: interpolator, merjenje amplitude, pravokotni signali, bliskovni interpolator, avtomatična kontrola ojačanja, kodirnik.

Izvleček: V članku je opisano bliskovno interpolacijsko vezje za pretvorbo analognih sinusnih in ortogonlnih signalov v množico prav tako sinusnih - fazno zamaklnjenih signalov, ki predstavljajo osnovno informacijo za nov algoritem merjenja amplitude. Merjenje je neodvino od frekvence signalov, interpolacijsko število 4 pa zadošča za preciznost merjenja 5.8%. Algoritem je podan in preizkušen v interpolacijskem vezju, ki je bilo procesirano v 0,35um tehnologiji CMOS.

1. Introduction

A typical application in the motion control field is in magnetic or optical linear and rotary encoders, the major part of which comprises integrated electronics. In general, the electronics comprise an opto-sensing area or hall sensors structure, analog front-end and signal conditioning, and a fast interpolator and digital signal processing unit. The front-end performs sensors supply, sensors excitation and signal magnification functions. The operation speed of the encoders, based on magnetic sensors, is usually much slower than one based on light modulation. This holds true mainly for magnetic rotary encoders, the speed of the magnetic linear encoders being faster, but usually never exceeding the speed of optical encoders /1/, /4/, /16/, /21/, /24/, /31/ and /35/.

An analog signal generated from a sensors array is amplified and digitized to provide incremental orthogonal digital signals named track A and track B. Before digitizing the analog signals they can be further interpolated to achieve better measurement resolution /2-3/, /6-7/, /11/, /13/, /18/, /22/, /25/, /28/, /29/ and /35/.The same is true for an absolute type encoder which can perform absolute position detection /9/, /14/, /20/, /32/.

In the case where more than 7-bit resolution is required, analog signals conditioning need to be implemented. This includes equalization of the sine and cosine signal amplitudes, their offset equalization and phase difference adjustment to 90 degrees. The most common practice is adjusting analogue front-end parameters via a serial interface or reprogramming them with access to internal EEPROM /12/. Automatic offset measurement and cancellation are relatively simple /17/, the phase measurement and correction and the amplitude regulation and measurement being more complicated /5-6/, /11/, /25/, /28/, /38/ and /42/. A magnitude and phase estimation algorithm has been published /5/ for a signal with time-varying frequency. The method is slow and requires modest computations.

Squaring algorithm using analog multipliers is a well known method for obtaining/extracting DC information from sine-cosine signals /36/. The main disadvantages are the limited linear input voltage range and its temperature behavior. Also the flash interpolator circuits that comprise the signal generating circuit, of which the out-of-phase signals are generated by gain stages having different magnifications, are much slower /37/. The appropriate comparators circuit /37/ compares signals at different common mode levels, which may additionally cause different delays and offsets. The Cordic-based Loeffler discrete cosine transform (DCT) architecture is presented in /41/. It requires high level of digital complexity and is very suitable for low-power and high-quality codecs.

Anything that can affect the accuracy of the final application is related to the overall decoder system's components /9/, /19-20/, /40/, /43/, /44/ and to the applied algorithms /27/, /28/. Therefore, the question of calibration is system related.

The aim of this work is to present a less precise, but cost-effective and robust amplitude measurement algorithm, based on a flash interpolating circuit, suitable for VLSI integration on "system on chip SoC". Amplitude measurement is a basic pre-processing step for automatic signal-amplitude correction and for the AGC function. The major advantage of the proposed method is that there is no need for an extra system clock. Due to the lower silicon area consumption, low power consumption and signal frequency independent measurement method, the present solution is suitable for use in all integrated automatic signal conditioning systems.

This paper is organized as follows. The typical application - encoder - that uses AMM, and the design considerations are described in Section 2. A detailed description of the proposed flash interpolation method using sine wave input signals with an interpolator-inherent principle of amplitude measurement are described in the third and in fourth Section. The results of measurements are presented in Section 5.

2. Encoders - Basic Principles

An optical encoder translates an angular or linear position into an electrical signal. It is typically composed of a light source (LED), a main scale with a built-in optical grating with measuring period MP, and an optical scanner that is composed of an opto-sensor array and a reading scale with a built-in optical grating with a reading period, RP. The scanning head is usually composed of reverse polarized photodiodes that produce the quadrature signals, together with an additional photodiode (DF) that generates the index signal that is used for absolute position encoding.

In short, as the scanner moves along the main scale the amount of light from the light source is modulated. The electrical signal that is produced by the opto-sensor in the optical array is also modulated.

As we have seen, the encoder produces two ninety-degree shifted (quadrature) signals A+, A- and B+, B- (Figure 1b). The signals in Figure 1b are periodic; this periodicity corresponds to the movement of the scanner head with constant velocity along the main scale One period of the signal corresponds to a movement of the scanner head equal to the grating period (MP, RP). In general, the signals are not periodic in time, but are periodic in relation to the displacement along the main scale. The signals A+, A-, and B+, B- in Figure 1b are also not pure sine-cosine, but, in reality, are distorted and contain harmonic components. The incoming signals are also imbalanced in phase, offset and amplitude. The encoder system therefore requires signal conditioning prior to interpolation.

The two pairs of signals from optical array are usually transformed into voltages with a fully-differential voltage amplifier to remove the large DC component and suppress even harmonics to produce the signals to be further interpolated. The voltage amplifier should have a low output impedance to drive the resistive interpolation network. The two quadrature signals enable the position of the scanner head to be detected at all times, just by measuring the values of these two signals. To achieve high interpolation accuracy, the amplitude of the incoming sine signals should be regulated to the acceptable maximum level.

The signals can be digitized directly by an analog comparator. The two resulting digital signals (signal F4 and F8 in Figure 1b) will still be in quadrature and all information be in the low-high and high-low transitions of the signals. There are four such transitions per grating period (MP, RP). Therefore the intrinsic resolution of the encoder is one fourth of the grating period. Alternatively, interpolation can be used to increase the resolution.

An incremental type encoder outputs a pair of digital square waves Ao and Bo (Figure 1b) that are 90 degrees apart and convey, for instance, the change in the shaft's position, and direction of rotation. An absolute type encoder, on the other hand, detects an absolute position. Optical or magnetic encoders are widely used transducers that have applications in robotics, manufacturing, motors, and the hi-tech industry /1/, /14/, /23/, /24/ and /26/. All these may have incremental or absolute encoders.

3. Flash Interpolator - Theory and Fundamentals

The basic architecture of the proposed flash interpolation converter consists of four matched resistive chains, connected in a symmetric bridge (Figure 1a). The resistivity of each chain is R_v The differential channel signals CH-A and CH-B, ordinary and inverted (A+, A-, B+, B-), are connected to opposite sites of the bridge, the voltages of which are of equal amplitude, but phase shifted by 0 and 180 degrees (CH-A) and by 90 and -90 degrees (CH-B) as shown in Figure 1b. An interpolation factor of *IP=4* is chosen as an example. Thus interpolator circuit in Figure 1a consists of four resistive chains, each having *IP* resistors (r1 to r4 with total resistivity of $R_v = \sum_1^4 r_i$). It also consists of twice as many voltage comparators, C1 to C8, connected to the taps of the bridge. Each comparator always compares tap voltages on the same common mode (CM) level, as shown from simulations in Figure 2 (s1, s2, to s16). Each comparator compares two voltages, shifted in phase by exactly 180 degrees. Although all comparators operate at the same CM level, they differ in performance, which causes INL and DNL errors of the output code (variations of the separation time). Interpolator linearity is also limited by the resistors' matching requirements. Resistance values in the chain are calculated according to the shape of the incoming orthogonal and differential signals connected to the bridge corners (A+, A-, B+, and B-). Angle resolution *K* is defined by interpolation resolution set by *IP* within a single chain interval of 90 angle degrees. *K* is a constant:

$$K = \frac{90}{IP}, \text{ where } IP \text{ is defined in (6).} \quad (1)$$

From the present example of orthogonal sine signals, calculation of the resistivity of the chain resistors in a resistor bridge is:

- signal-angle calculation on individual resistor tap:

$$\alpha_I = I \cdot K; \quad I = 1, 2, \ldots, IP, \quad (2)$$

where maximal angle is α_{max} = 90 deg, and resistors are:

$$R_I(\alpha_I) = R_V \cdot \frac{\cos(\alpha_I)}{\sin(\alpha_I)+\cos(\alpha_I)}; \quad 45\text{deg} \le \alpha_I \le 90\text{deg} \quad (3)$$

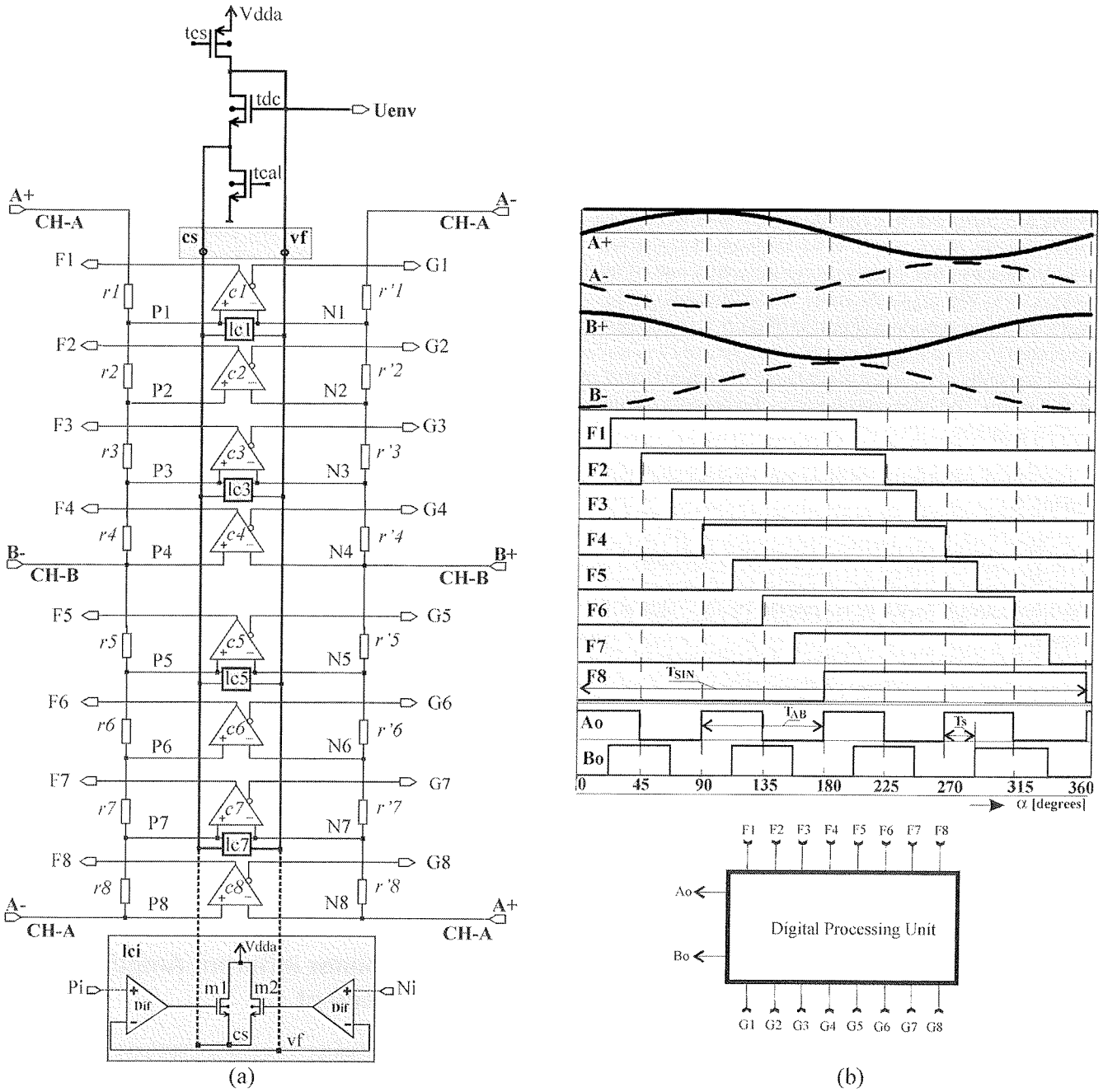

Fig.1. The linear optical encoder system – principle of operation. The interpolation factor of four is taken as an example, the realization of which is shown in (a). Signals A+, A- and B+, B- are the interpolator's input signals. The interpolator's output signals Fi and Gi are differential-digital signals, generated by the flash A/D converter/ interpolator. An XOR in the Digital Processing Unit (b) operates on them to produce a quadrature output signal Ao and Bo. Signals generated at the chain taps P1, P2, P3, P5, P6, P7 and N1, N2, N3, N5, N6, N7 are phase shifted. The all-followers common circuit (at the top (a) consists of the single load device tcal, *the level-shift circuit, constructed from diode device* tdc *and the biasing device* tcs. *Topology at the bottom (a) shows a distributed amplitude measurement structure within* ***lc1***, ***lc3***, ***lc5*** *and* ***lc7***. Vdda *is positive supply voltage,* vf *is feedback connection and* cs *a common source terminal for all distributed follower pairs, each consisting of two differential amplifiers* Dif *and a follower device* m1 *and* m2.

T_{SIN} is the sine-wave period and corresponds to the grating period RP; T_{AB} is the processor tracks output period and T_S the separation time between the two neighboring edges of tracks Ao and Bo (b).

$$R_I(\alpha_I) = R_V \cdot \frac{\sin(\alpha_I)}{\sin(\alpha_I)+\cos(\alpha_I)};\ 0\,\mathrm{deg} < \alpha_I < 45\,\mathrm{deg} \qquad (4)$$

$R_I(\alpha_I)$ is the sum of the resistivity of the resistors from *i=1* to *i=I*. Resistivity of a single resistor in a chain $R(r_i)$ is calculated by subtracting all resistors $(R(r_1)$ to $R(r_i\text{-}1))$ from the previously calculated sum.

Resistors are symmetrically positioned from the center of each resistive chain; thus the resistor values are mirrored within a range from 45 degrees to 90 degrees, and all four chains are matched. It is therefore sufficient to calculate resistors in the range from 0 to 45 degrees. It is also sufficient to process the incoming signals within half of their periods (0 to 180 angle degrees), since the same comparators act in the second half-period (Figure 1). As shown in the present example for *IP=4*, the resistivity of *r1* is equal to the resistivity of *r4,* the resistivity of *r2* is equal to that of *r3* and so on. The angle resolution in the present example is 22.5 degrees.

In the case of saw-shape incoming quadrature signals, the relation is:

$$R_I = \frac{R_V}{IP} \text{ and all resistors are of the same resistivity.} \qquad (5)$$

The interpolation factor *IP* is defined by the ratio of two periods:

$$IP = \frac{T_{SIN}}{T_{A,B}} \qquad (6)$$

T_{SIN} is the period of the incoming sine signals, $T_{A,B}$ is the period of the outgoing digital-orthogonal signals **Ao** and **Bo**, as shown in Figure 1b, where the track signals **Ao** and **Bo** are generated from the comparators' output signals **Fi** and **Gi** (Figure 1a).

Lagging or leading of the track signals depends on the current positions of the sine wave signals or, in other words, on the direction of movement of the measuring-head. Processor input signals contribute equal delay to the generated tracks, so it is important to achieve constant separation time between digital output edges over the whole input sine wave period. This is very important at high moving speed.

3.1 Identifying the Non-ideality Sources

Although all comparators operate at the same CM level, they differ in performance, which causes INL and DNL errors of the output code (variations of the separation time). It is important to note that the comparator's input signals from the resistor taps have different slopes. The offset of the comparators would influences the switching point by the ratio between peak sine signal amplitude and the comparator offset voltage. This influence can be expressed as an angle difference of $d\alpha=\sin^{-1}(Voff)$ (we assume that the peak sine amplitude is 1V). The most critical non-ideality is the comparator offset difference (mismatch). Interpolator linearity is also limited by the resistors' matching requirements. The resistor mismatch directly affects the comparator switching. Furthermore, the influence of different non-idealities on the system performance becomes important when a higher order interpolator is an issue (resistors mismatch directly influences tracks separation time). It is therefore important to follow the matching parameters' information supported by an IC manufacturer and design resistors wide accordingly. Mismatch of the resistors' contacts and taps' resistance are in some cases more important. Therefore, the realization of the current contacts differs from that used only as a voltage tap. Moreover, all the resistors' related layout rules, like dummy material, should also be considered.

The influence of the comparator's delay on the interpolator performance depends on the scanner moving speed. The delay degrades the separation time (and the real head position) only minimally at lower speed, while the effect increases with increasing moving speed. The comparator's delay limits the upper measuring speed. Just take an example from section 4: the realized interpolation factor of 100 gives 400 transitions per sine signal period (IP=100). Using a grating period of 20 µm, a sine signal frequency of 100 kHz is achieved by the scanner moving speed of 2m/second. The rate of the track signals Ao and Bo are 100 times faster and is 10 MHz. The nominal separation time between the two neighboring edges of Ao and Bo is therefore 25 ns. At such a high speed, the comparator's delay should not exceed 6 ns (to maintain a minimal separation time of 50% from the nominal one). It is also important to note that the comparator's delay could be much larger; the difference between neighboring comparators delay should not exceed 6 ns. The position error will be accumulated in this case.

Temperature dependence and reliability of the product are the most serious issues in high accuracy motion control.

4. Interpolator Inherent Amplitude Mesurement

The proposed circuit for measuring amplitude is combined into an interpolator architecture shown in Figure 1a. This results in a compact, area efficient topology that contributes to better dynamics and finally to better speed performance. The interpolator is therefore a basic structure, upgraded by an envelope detector, the output of which tracks the maxima of relevant signals generated along the resistor bridge. The AMM upgrade consists of distributed voltage followers Ic1, Ic3, Ic5 and Ic7, combined to odd comparators *c1*, *c3*, *c5* and *c7* (Figure 1a). As described later, only odd comparators handle phase shifted signals having maxima at:

$$P_i, N_i \equiv i \cdot K, \quad i=1, 3, 5, \ldots 2(IP-1) \tag{7}$$

Each follower consists of a differential stage (Dif) followed by a source follower device m1 or m2, the sources of which are connected to a single - active load device *tcal* at the common node *cs* (at the top in Figure 1a). The active load structure is common to all followers in the AMM circuit. The drain voltage of the *tcal* device follows voltages on the inputs of the follower devices m1 and m2 from all comparators/followers. Follower feedback voltage, vf, is shifted up by the diode voltage of the *tdc* device, which forces the source voltages of m1 and m2 to be below the gate voltages of m1 and m2 for a diode voltage of the *tdc* device. This action is required for differential amplifiers *Dif* to compare input signals to the common feedback signal *cs*, where all input signals have the correct common-mode level. The common source potential, therefore, follows that input voltage on the follower devices m1 and m2, which have the maximum amplitude. Consequently, a higher source potential on node *cs* forces the devices m1 and m2 with lower input amplitudes to the off state. The current source *tcs* provides proper biasing for the diode device *tdc*. Output signal Uenv tracks the input signal on resistor taps that is currently of the highest amplitude. The potential on node *vf* is therefore the envelope (maxima) of all compared signals and carries useful information about the peak amplitude of incoming signals from channels CH-A and CH-B.

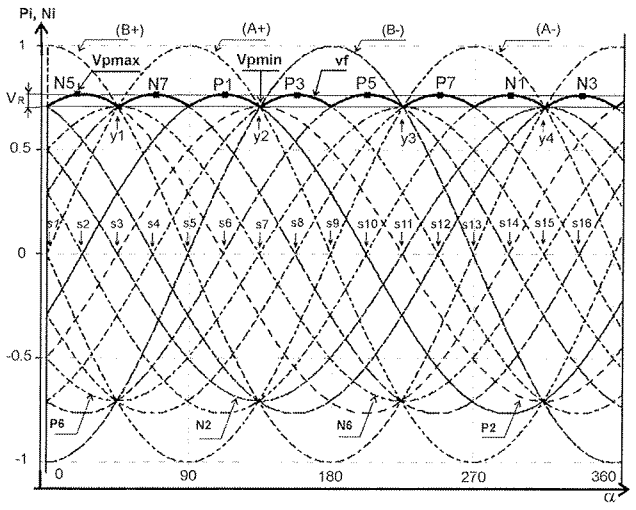

Fig. 2. Simulated waveforms of the phase shifted signals Pi and Ni on the symmetrical resistive bridge of an interpolator from Figure 1a. The shadow area V_R is an envelope range (envelope ripple), showing also local minima and maxima. Signals P2, N2, P6, and N6, as well as input signals from CH-A (A+, A-) and from CH-B (B+, B-), do not contribute to minimization of the envelope ripple. All signals have the same period and offset as input signals, but differ in amplitude and phase shift.

The tracking accuracy depends on differential amplifier gain and offset voltage. All signals within one segment of the bridge cross at the same points (y1, y2, y3 and y4) which are multiples of 45 degrees. The ripple extremes exist at multiples of α=45/2 degree:

$$\alpha = K = \frac{360}{4 \cdot IP} = 22.5 \deg. \tag{8}$$

from which it follows that *IP=4* is sufficient to realize amplitude measuring (AMM) and automatic-gain control (AGC) functions. The extremes of the Uenv envelope are:

- global minima that are at even multiples of α, where α is 22.5 angle degrees, and are defined as:

$$Vp\min = Vp \cdot \left\{ \left[\sin(\alpha) + \frac{\cos(\alpha) - \sin(\alpha)}{\cos(\alpha) + \sin(\alpha)} \cdot \cos(\alpha) \right] \cdot \sin(90 - \alpha) \right\} = Vp \cdot 0.707106 \tag{9}$$

Vp is the peak amplitude of the input sine signal.

- maxima that are at odd multiples of α and are defined as:

$$Vp\max = Vp \cdot \left[\sin(\alpha) + \frac{\cos(\alpha) - \sin(\alpha)}{\cos(\alpha) + \sin(\alpha)} \cdot \cos(\alpha) \right] = Vp \cdot 0.76536 \tag{10}$$

As the interpolation factor *IP* increases, the signal amplitudes on the resistor bridge taps closer to input signals increase, while the ripple extremes remain at multiple of the 22,5 degrees (Figure 2). An interpolation factor IP of 4 is therefore optimum for the proposed algorithm. Because the minima are global, a ripple of 5,825% of the peak input amplitude *Vp* is a minimum and is defined as:

$$ripple[\%] = Vrip[\%] = \frac{Vp\max - Vp\min}{Vp} \cdot 100 \tag{11}$$

The *ripple* function $V_{rip}(a)$ can also be described using a general *modulo* function, valid over the whole signal period:

$$Vrip(\alpha) = Vp \cdot \left[\begin{array}{l} \sin\left(\alpha\left(\bmod\frac{\pi}{4}\right)\right) \cdot \left(1 - \sin\frac{\pi}{4}\right) + \\ + \cos\left(\alpha\left(\bmod\frac{\pi}{4}\right)\right) \cdot \sin\frac{\pi}{4} \end{array} \right], \tag{12}$$

and the extreme functions are:

$$Vrip\_\max(n) = Vrip\left((2n+1) \cdot \frac{\pi}{8}\right) \cdot \text{ and is: } 0.76536 \,.\, V_p, \tag{13}$$

where maxima are positioned at all odd multiples of $\pi/8$;

$$Vrip\_\min(n) = Vrip\left(2n \cdot \frac{\pi}{8}\right) \text{ - and is: } 0.707106 \,.\, V_p, \tag{14}$$

minima are positioned at all even multiples of $\pi/8$, where *n* ranges from ....,-2, -1, 0, 1, 2...., and where $\pi/8$ radians is equal to 22.5 angle degrees. Any other search for maxima in terms of "searching for minima above global minima" is much more complex and requires much higher

speed Ic$_i$ circuits, the tracks of which have to be controlled by extra - fast comparators.

4.1 Identifying the Non-ideality Sources

Resistor *r1* mismatch of 1% and 2% (Figure 1a) is taken as an example for analysis shown in Figure 3. The larger *r1* resistivity then required slightly reduces the maximum at the corresponding angle position, as is shown in detail on top of the picture (curves *r1_1%_mis* and *r1_2%_mis*). It is evident that the comparator offset cannot affect the sine signals on resistors' taps. On the other hand, the offset voltage of the differential stages Dif drastically affects the envelope extremes. As the Dif is in a source follower configuration, its offset contributes directly with a unity gain to the envelope change as is shown, as an example, for 10mV offset (curve *Dif_10mV_offset*) and for -10mV offset (curve *Dif_-10mV_offset*). It is also clear that each Dif stage contributes only at an appropriate angle position area (we put offset voltage to Dif stage in the Ic1 block only - Figure 1a).

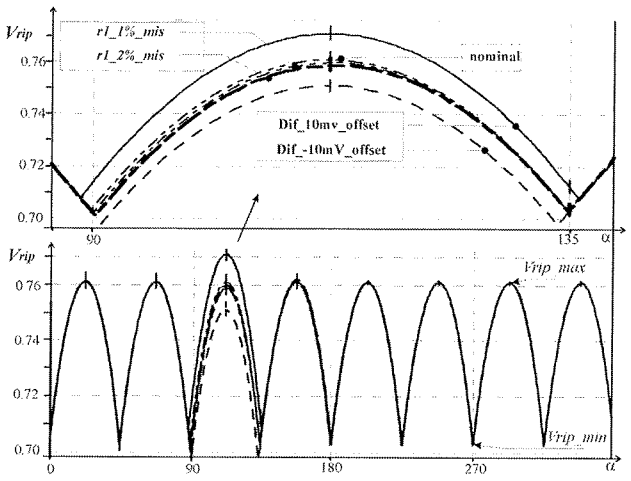

Fig. 3. Simulated envelope voltage, Vrip, *on Uenv output node (curve P1 is shown in detail).*

5. Results and Discussion

The proposed technique was realized in an encoder ASIC to verify the accuracy of the AMM technique. The realization is an integrated incremental ASIC (Figure 4) which operates at an input sine wave signal frequency from DC to 100kHz in a temperature range from -40°C to 125°C and at a supply voltage of 4.5V±0.5V. The processed ASIC is fully operational up to 200 kHz under typical conditions. The opto-sensor array is a separate integrated circuit comprising the reverse biased Si photodiodes and the signal is in the form of an electrical current. The light intensity of the LED device is controlled by part of the generated error signal in the AGC block. The measured performances of the AMM itself are shown in Table I. Measured ripple is filtered out at higher frequencies (pad-probe: 300Ω/8pF-1MΩ/90pF) and therefore cannot be reported without filtering action (Table I). The measurement at the fastest operation is shown in Figure 5.

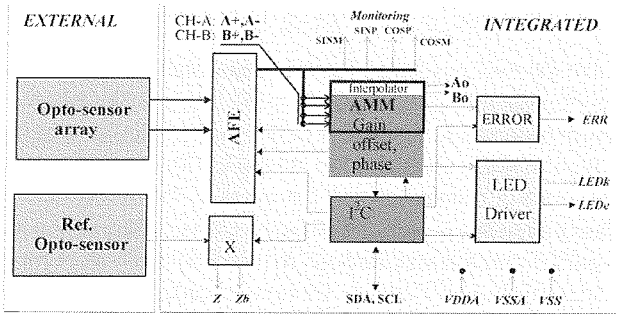

*Fig. 4. Interpolator ASIC combines a signal conditioning feature, where externally generated input sine signals are applied to the analog-front-end, AFE, and where the AMM module (**am**plitude **m**easurement as part of the interpolator) automatically controls the amplitudes of the incoming orthogonal sine signals to the interpolator circuit.*

Table I: Measured AMM output signals.

Sine/Cosine Frequency [kHz]	Sin/Cosine peak [mV]	Measured Uenv additionally loaded by the probe – 1M/90PF	
		V_{min} [mV]	V_{max} [mV]
0.1	500	352	383
1	100	74	80
1	500	352	383
20	1000	709	755
100	1000	740	740

It is clear that, in practice, the signal conditioning is not running when the scanner is moving fast, simply because the measurement, and therefore the interpolation, should not be disturbed by the automatic AMM and AGC. The amplitude measurement and regulation are running within a certain frequency window and that range has to be monitored simultaneously. Result 5,8% represents an optimum and the minimum for the flash interpolator we proposed. Measurement accuracy of 5,8% for the AGC function is sufficient for most industrial applications.

6. Conclusion

The aim of this work was to find a cost-effective and area-effective method of generating peak amplitude information from sine wave signals. The major part of the amplitude measurement and envelope extraction is already inherent in the presented flash interpolator and only minor additional electronics has been added. The target of this work was to improve the quality of the quadrature signals to enable higher interpolation factors and higher encoder resolution.

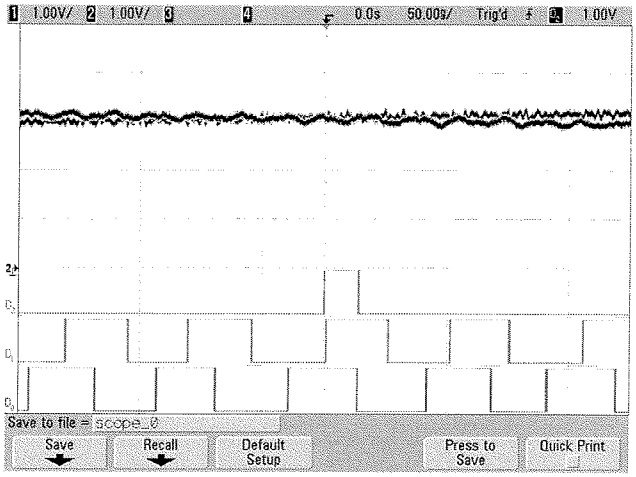

Fig. 5. Measurement of the interpolator at IP=100 and at input sine signals frequency of 100 kHz. Index is shown in D2, track Ao in D1 and the track Bo in D0.

The amplitude information, when evaluated, shows the following: if the AC part of the information is larger than the expected 5.8 % ripple (seen at lower head moving speed only), it results from the sine-signal-pair to cosine-signal-pair amplitude mismatch. To implement precise amplitude correction, matching of the quadrature sine signals prior to AGC is necessary. Moreover, appropriate comparator circuits that weight the measured signal amplitudes to predefined values need to be designed, having the hysteresis ratiometric to generated signal amplitude to overcome undesired ripple at lower signal frequencies. It is also important to regulate sensors supply and light intensity parameters prior to AGC (based on AMM measurement) to maintain the design requirements for the dynamic range.

The proposed solution for AMM is much more robust than that using a square circuit to generate DC voltage out of sine and cosine signals. The amplitude measurement described in this paper is an inherently linear process that generates envelope by using the same signal processing path as the interpolator itself. Interpolator monotonicity is guaranteed by the proposed architecture.

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