A NOVEL CMOS DEFUZZIFICATION CIRCUIT EMPLOYING CURRENT DIFFERENCING BUFFERED AMPLIFIER BASED CURRENT-MODE MULTIPLIERS

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Key words: Current Differencing Buffered Amplifier (CDBA), Defuzzification circuit, current-mode multiplier

Abstract: In this paper, design and analysis of a novel current-mode defuzzification circuit is presented. The proposed defuzzification circuit is based on current-mode four-quadrant multipliers that have been constructed with simple current squarer and current differencing buffered amplifier (CDBA). This circuit has capable of high linearity, simple structure, and wide input current range. The defuzzification circuit has been simulated and verified by PSPICE with MIETEC 1.2 μm parameters. The circuit is suitable for using Centre Of Gravity (COG) method in current-mode fuzzy logic controllers. The purpose of this paper is to present an alternative approach for current-mode defuzzification circuit design.

Novo FLC CMOS vezje

Kjučne besede: CDBA vezje, mehčalno vezje, ojačevalniki toka

Izvleček: V prispevku predstavimo načrtovanje in analizo inovativnega vezja FLC (Fuzzy Logic Circuit). Mehčalno vezje (defuzzification circuit) je linearno in ima enostavno strukturo in vhodni tok v širokem intervalu. Vezje smo simulirali s programom PSPICE s parametri MIETEC 1,2um. Namen prispevka je prikazati drugačen pristop k načrtovanju vezij FLC.

1. Introduction

The defuzzification circuit or defuzzifier is one of the most important units in the fuzzy logic controllers (FLC). There are two ways to implement a defuzzifier: the analogue approach and the digital approach. The analogue approach presents several advantages in front of digital ones, especially regarding speed of processing, power dissipation and functional density. Moreover, the analogue circuit based fuzzy blocks perform continuous-time processing and they have the particularly to be well compatible with sensors, actuators and all other analogue signals /1-3/. On the other hand, digital circuits are superior to analogue counterpart in accuracy, extendibility, and easy of design automation /4-5/.

The centre of gravity (COG) is the most popular defuzzification method in FLC. Various defuzzification circuits using COG method are described in literature /6-9/. A high-speed digital defuzzification circuit based on BiCMOS technology has been proposed in /7/ but the fabrication cost is high. The other defuzzification circuit design with current-mode analogue circuits was proposed in /8/. However, both frequency range and speed of these circuits are low. Another defuzzification circuit using resonant tunnelling diodes is proposed by Tang and Lin /9/. Their design reduces circuit complexity compared with conventional digital and analogue signal processing circuits.

Recently, a new five-terminal active current-mode element, called a current differencing buffered amplifier (CDBA), has received much attention in the electronics community /10-12/. It can be operated in both current-mode and voltage-mode in a wide frequency range and can also be implemented with CMOS technology. Differential nature of this element at the input makes it especially suitable for various analogue signal-processing applications demanding high speed, high bandwidth and simple implementation.

In this paper, a new defuzzification circuit employing CDBA based current-mode multipliers is presented. The proposed circuit is built using current-mode four-quadrant multiplier includes simple current squarer and CDBA, and current-mode reverse function circuit as divider unit.

The outline of this paper is as follows. Section II briefly defines a block diagram of proposed defuzzification circuit, then the current squarer and Current Differencing Buffered Amplifier (CDBA) that composed of current-mode four-quadrant multiplier are theoretically described in detailed. Also, the current-mode reverse function circuit is described as the division unit of defuzzification circuit. Section III evaluates a proposed four-quadrant multiplier, reverse function circuit and defuzzification circuit with PSPICE simulation experiments. In Section IV, the overall conclusions are given.

2. Circuit Description

The COG method in current-mode is expressed as

$$I_{out(COG)} = \frac{\sum_{i=1}^{n} I_{\mu i}.I_{ci}}{\sum_{i=1}^{n} I_{\mu i}} \quad (1)$$

where n represents the number of fuzzy sets on the universe of discourse, $I\mu_i$ and Ic_i represent the *membership function output* and *support* value of the *i* th fuzzy set, respectively. Eq. (1) can be arranged with current values of input/output variables as follows.

$$I_{out} = \frac{I_{\mu 1}.I_{c1}}{I_{\Sigma}} + \frac{I_{\mu 2}.I_{c2}}{I_{\Sigma}} + ... + \frac{I_{\mu n}.I_{cn}}{I_{\Sigma}} \quad (2)$$

where I_{Σ} is equal to $\sum_{i=1}^{n} I_{\mu i}$

The input and the output characteristics of each term in equation (2) can be defined by using current-mode four-quadrant multiplier blocks. Each block in Eq. (2) is computed as follows:

$$I_{out} = \frac{I_x I_y}{I_w} \quad (3)$$

where I_x, I_y, I_w, and I_{out} variables are corresponded with $I\mu_i$, Ic_i, I , and I_{oi} , respectively. The block diagram of defuzzification circuit processing unit in Eq. (3) is implemented with two multipliers and one current-mode reverse function block as shown in Fig.1.

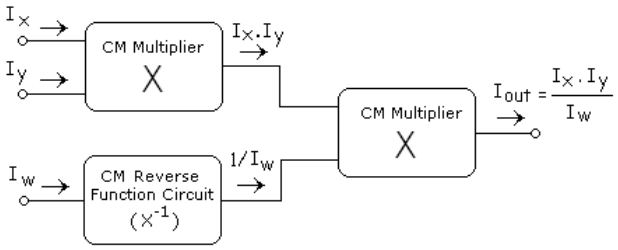


Fig. 1: The block diagram of defuzzification circuit processing unit

The building blocks of current-mode multiplier circuit are shown in Fig. 2. This multiplier circuit is consists of two cascode current mirrors, one modified current differencing amplifier (CDBA), and three current squarer units.

The modified circuit structure of the CDBA in /10/ and circuit symbol is shown in Fig. 3 (a) and (b), respectively. The characteristic equation of this element can be given as

$$V_p = V_n = 0, \quad I_z = I_p - I_n, \quad V_w = V_z \quad (4)$$

Here, current through z-terminal follows the difference of the current through p-terminal and n-terminal. Input terminals, p and n, are internally grounded. A possible CMOS realization of CDBA consisting of a differential current

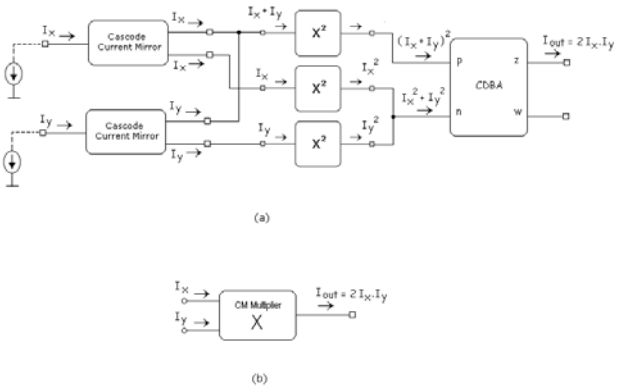


Fig. 2: (a) The building blocks of current-mode multiplier circuit (b) its symbol

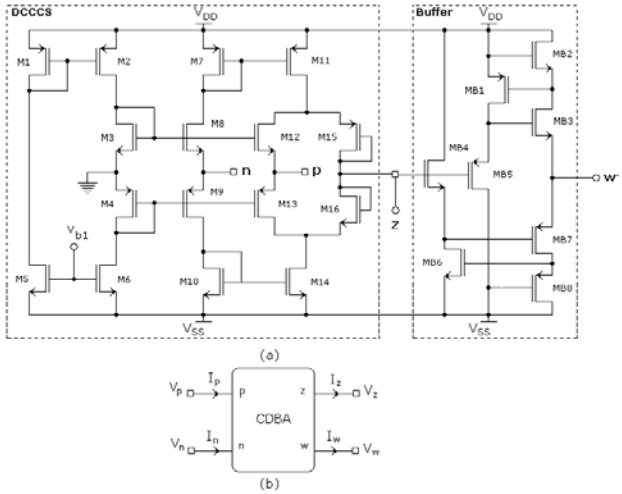


Fig. 3: (a) Simplified CMOS implementation of modified CDBA and (b) its symbol (V_{DD}= -V_{SS}= 2.5 V and V_{b1}= -1.45 V)

controlled current source (DCCCS) followed by a voltage buffer is shown in Fig. 3 (a).

2.1. Current Squarer

The current squarer circuit into four-quadrant multiplier is shown in Fig. 4.The MOSFETs, M1, M2, and M3, are the identical transistors, working in saturation region. In condition that $V_{GS}>V_T$ and $V_{DS}>V_{GS}-V_T$, the expression of drain current for the simple MOS transistor operating in saturation region is

$$I_{ds} = \mu C_{ox} (\frac{W}{L})(V_{GS} - V_T)^2 \quad (5)$$

$$I_{ds} = K(V_{GS} - V_T)^2 \quad (6)$$

Where **K** is trans-conductance parameter, and μ, $C_{ox,}$ W, and L stand for carrier effective mobility, gate oxide capacitance per unit area, width, and length of the channel, respectively /13/.

In Fig. 4, V_B and I_{in} are the dc bias voltage and input current, respectively. If all MOS transistors operate in saturation

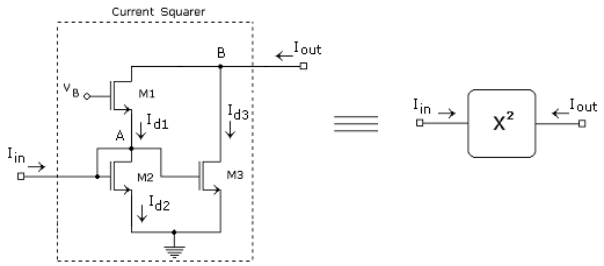


Fig. 4: The current squarer circuit and its symbol

region and trans-conductance parameters of all transistors are identical, i.e., $K_1=K_2=K_3=K$, then bias voltage V_B is given by

$$V_B = V_{gs1} + V_{gs2} \tag{7}$$

If KCL is applied to A and B nodes, output current I_{out} can be obtained as follows:

$$I_{d2} = I_{d3} = I_{in} + I_{d1} \tag{8}$$

$$I_{out} = I_{d1} + I_{d3} \tag{9}$$

Using equations (4)- (5), I_{out} can be derived as follows

$$I_{out} = 2I_{d1} + I_{in} \tag{10}$$

The voltage of node A, V_A, is equal to V_{gs2} and the drain current of M_1 transistor can be obtained by using equation (1) and (2).

$$V_A = V_{gs2} = \sqrt{\frac{(I_{in} + I_{d1})}{K}} + V_t \tag{11}$$

$$I_{d1} = K\left[(V_B - V_{gs2}) - V_t\right]^2 \tag{12}$$

Using equation (7) into (8), the drain current of M_1 transistor, I_{d1}, can be obtained as follows:

$$I_{d1} = \frac{I_{in}^{\,2}}{4K(V_B - 2V_t)^2} + \frac{K}{4}(V_B - 2V_t)^2 - \frac{I_{in}}{2} \tag{13}$$

If equation (9) is placed into equation (6), the output current I_{out} is given by

$$I_{out} = \frac{I_{in}^{\,2}}{2K(V_B - 2V_t)^2} + \frac{K}{2}(V_B - 2V_t)^2 \tag{14}$$

Where K transconductance parameter, bias voltage, V_B, and threshold voltage, V_t, are constant values and are chosen by designers.

Here, $\frac{K}{2}(V_B - 2V_t)^2$ expression in equation (10) is similar to drain-to-source current of MOSFET transistor in saturation region. Therefore, this current can be supplied from a current mirror structure. If this expression is equal to constant bias current as I_B via current mirror, then output current, I_{out}, can be obtained as follows:

$$I_{out} = \frac{1}{4I_B} I_{in}^{\,2} + I_B \tag{15}$$

From (11), the circuit operates as squarer circuit with the dc output offset current of I_B. The offset current is cancelled by adding the current source to the output terminal.

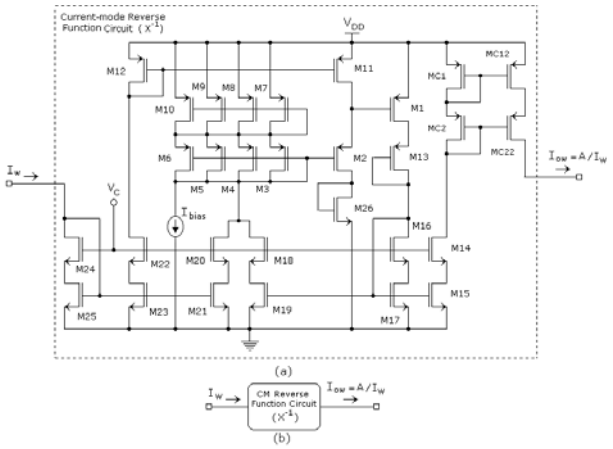


Fig. 5: (a) Current-mode reverse function circuit and (b) its block representation

Figure 5 shows current-mode reverse function (1/x or x^{-1}) circuit as divider operator in proposed defuzzification unit. This circuit is basically current squarer/divider circuit. The reverse function circuit output current I_{out} is obviously given by

$$I_{out} = \frac{I_{bias}^{\,2}}{4I_w} \tag{16}$$

$$I_{out} = \frac{A}{I_w} \quad \text{for} \quad A = \frac{I_{bias}^{\,2}}{4} \tag{17}$$

Here, I_{bias} is corresponded to squaring current and it has been fixed value as dividing coefficient, i.e. $A = I_{bias}^{\,2}/4$. Thus, the circuit can be converted to divider operator by fixing squaring current I_{bias}. In this circuit, the voltage-translinear loops are formed by transistors M1–M10; note that the bulk terminals of these transistors are connected to their sources, thus avoiding the body effect. M13 and M26 are diode-connected transistors included for decreasing the channel-length modulation effect in M1 and M2, respectively. Transistors M11–M12 form a current mirror and M14–M25 constitute high-swing cascode current copiers employed for injecting the required combinations of currents into the voltage-translinear loop. The circuit is designed for VDD = 2.5 V and V_C = 1.3 V /14/.

3. Simulation Results

The behaviour of the implemented CDBA and simple current squarer based defuzzification circuit was confirmed with 1.2 µm MIETEC CMOS process parameters by PSPICE simulations. The all device dimensions of the squarer circuit in Fig. 4 are identical and W/L= 120 µm/2 µm. The transient analysis results of current-mode reverse function circuit are shown in Fig. 6. Here, I_{bias} current is corresponded to

I_z current in current squarer/divider circuit is presented by /14/. This current is fixed value (50 µA) in our proposed defuzzification circuit for using as divider operator.

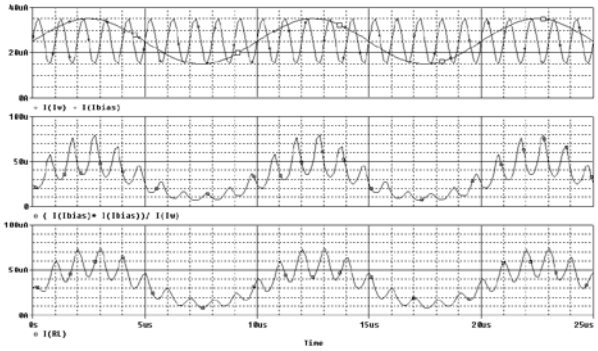
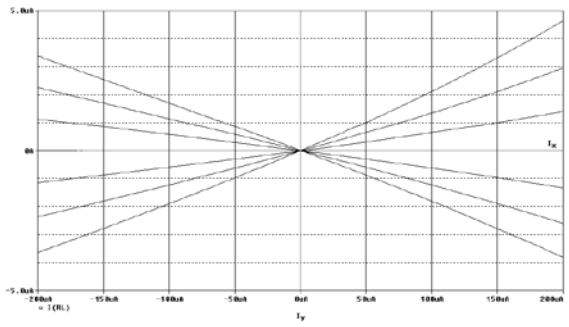


Fig. 6: The transient analysis result of current-mode reverse function circuit. Input signals (top), the calculated result of current-mode reverse function (middle), the circuit output (bottom) /14/.

The PSPICE-DC and transient analysis results of multiplier circuit (Fig.2 (a)) are shown in Fig. 7 (a) and (b), where I_y(i.e. I_{ci} support value) is [-200 µA; +200 µA] in amplitude, I_x (i.e. $I_{\mu i}$ membership value) is varied DC signal forms between [-15 µA; +15 µA] in 5 µA steps. In Fig. 7 (b), the frequencies of input currents, I_x and I_y, are selected 3 and 5 MHz, respectively. The error change of between calculation result and circuit output is about %1. So, this result is shown both wide

a)



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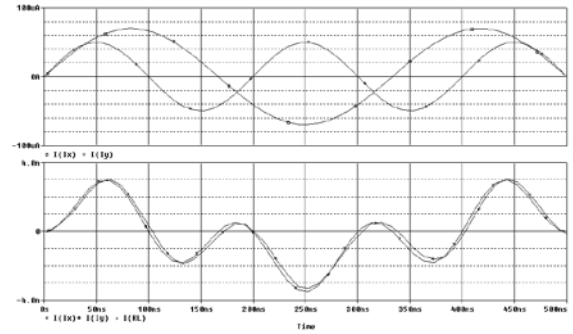

Fig. 7: (a) DC waveform of CDBA and current squarer based current-mode four-quadrant multiplier (b) Transient response of four-quadrant multiplier. Input current signal (top) and together calculated graph and circuit output (bottom) (frequencies of I_x and I_y are 3 and 5 MHz, respectively.)

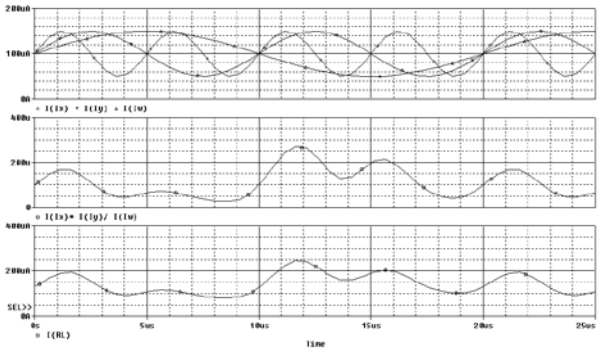

Fig. 8: The simulation results of current squarer and CDBA based defuzzification circuit. Input current signals (top), the calculation result of defuzzification process (middle), and the output waveform of proposed defuzzification circuit (bottom).

input current range and high frequency features of proposed circuit because of using CDBA structure in current-mode four-quadrant multipliers. In the simulations of proposed defuzzification circuit, the circuit parameter values are determined as follows: V_{DD}= -V_{SS}= 2.5 V, -200 µA ≤ I_y (I_{in}) ≤ +200 µA, -15 µA ≤ I_x ($I_{\mu i}$) ≤ 15 µA, V_{b1}= -1.45 V, R_L=1 KΩ.

The mathematical and simulation results of defuzzification processing unit are shown with together in Fig. 8. Three input sinusoidal signals (I_x, I_y, and I_w) are applied defuzzification processing unit. The simulation result of defuzzification circuit is verified to calculation result as shown in Fig. 8.

4. Conclusions

A novel current-mode defuzzification circuit using Centre of Gravity (COG) method has been designed and analyzed. Its behaviour was confirmed by PSPICE simulation experiments with MIETEC 1.2 µm CMOS process. The implemented defuzzification circuit is based on current-mode four-quadrant multipliers and modified current squarer/divider circuits as divider operator in defuzzification processing unit. The proposed current-mode defuzzification circuit has capable of high linearity, simple structure, and wide input current range. The features are verified with PSPICE simulation experiments. The defuzzification circuit is suitable for CMOS fuzzy logic controllers with Centre Of Gravity (COG) method.

References

/1/ S. Bouras, M. Kotronakis, K. Suyama, Y. Tsividis, 'Mixed Analog-Digital Fuzzy Logic Controller with Continuous-Amplitude Fuzzy Inferences and Defuzzification', *IEEE Trans. On Fuzzy Systems*, May 1998, 6, (2), pp. 205-215.

/2/ A. Rodriguez-Vazques, R. Navas, M. Delgado-Restituto, F. Vidal-Verdu, 'A Modular Programmable CMOS Analog Fuzzy Controller Chip', *IEEE Trans. on Circuits and Systems-II*, March 1999, 46, (3), pp. 251-265.

/3/ J.L. Huertas, S. Sánchez-Solano, I. Baturone, A. Barriga, 'Integrated circuit implementation of fuzzy controllers', *IEEE J. Solid-State Circuits*, vol. 31, No.7, pp. 1051-1058, 1996.

/4/ M.J. Patyra, J.L. Grantner, and K. Koster, "Digital Fuzzy Controller: Design and Implementation", *IEEE Trans. On Fuzzy Systems*, vol.4, no.4, pp. 439-459, 1996.

/5/ S. Sánchez-Solano, Á. Barriga, C.J. Jimenez, J.L. Huertas, "Design and application of digital fuzzy controllers", *IEEE Proc. the Sixth International Conference on Fuzzy Systems*, vol.2, pp. 869 -874, 1997.

/6/ B.D. Liu, C.Y. Huang, H.Y. Wu, 'Modular current-mode defuzzification circuit for fuzzy logic controllers', *Electron. Lett.*, 1994, 30, (16), pp.1287-1288.

/7/ J.B. Kuo, H.J. Huang, S.S. Chen, C.S. Chiang, 'BiCMOS dynamic defuzzifying circuit for fuzzy logic controllers', *Electron. Lett.*, 1993, 29, (1), pp.67-68.

/8/ M. Tartagni, P. Perona, 'Computing centroids in Current-mode Technique', *Electronics Letters*, 1993, Vol. 29, Iss. 1, pp. 1811-1813.

/9/ H. Tang, H.C. Lin, 'Defuzzifier circuits using resonant tunneling diodes', Proc. *IEEE Int. Symposium on Circuit and Systems*, Seattle, April 1995, pp. 981-984.

/10/ C. Acar, and S. Özoğuz, " A Versatile Building Block: Current Differencing Buffered Amplifier Suitable for Analog Signal Processing Filters," *Microelectronics Journals*, vol.30, pp.157-160, 1999.

/11/ A. Toker, S. Özcan, O. Çiçekoğlu, and C. Acar, "Current-mode allpass filters using CDBA and a new high Q bandpass filter configuration", *IEEE Trans. on Circuits and Systems-II: Analog and Digital Signal Processing*, vol.47, no.9, pp.949-954, 2000.

/12/ W. Tangsrirat, W. Surakampontorn, and N. Fujii, "Realisation of leaprog filters using current differencing buffered amplifiers," *IEICE Trans. Fundemantals*, vol. E86-A, no.2, pp.318-326, 2003.

/13/ C. Toumazou, F.J. Lidgey, and D.G. Haigh, *Analogue IC Design: The Current-Mode Approach*, London, U.K.:IEE Press, 1990.

/14/ A. J. López-Martín, A. Carlosena, "Current-Mode Multiplier/Divider Circuits Based on the MOS Translinear Principle", *Analog Integrated Circuits and Signal Processing*, vol.28, pp.265-278, 2001.

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