BV_{CEO} ENGINEERING IN SOI LBT STRUCTURE WITH TOP CONTACTED BASE

Marko Koričić, Tomislav Suligoj

Department of Electronics, Microelectronics, Computing and Intelligent Systems, Faculty of Electrical Engineering and Computing, University of Zagreb, Zagreb, Croatia

Key words: SOI, lateral bipolar transistor, extrinsic base, charge sharing effect, common-emitter breakdown voltage, cutoff frequency

Abstract: Properties of SOI LBT structure with the base contact on top are analyzed by device simulations. The effect of the extrinsic base width on the common-emitter breakdown voltage (BV_{CEO}) is studied in detail. Charge sharing between extrinsic and intrinsic base acceptors can be controlled to achieve fully depleted collector. Shielding of the electric field across intrinsic junction by the extrinsic base electric field can be used to limit the peak value of the electric field along the current path in the collector-base depletion region and to increase the value of BV_{CEO}. Two peaks of electric field appear in the base-collector depletion region – the first one at the intrinsic junction and the second in the drift region toward extrinsic collector. The area in which breakdown occurs depends on the value of the electric field in two peaks, which can be controlled by the extrinsic base width (w_{bext}).

Inženiring parametra BV_{CEO} v SOI LBT tranzistorski strukturi z baznim kontaktom na vrhu

Kjučne besede: SOI, bipolarni tranzistor, ekstrinzična baza, deljenje naboja, prebojna napetost s skupnim emiterjem, mejna frekvenca

Izvleček: Simulirali smo lastnosti SOI LBT tranzistorske strukture z baznim kontaktom na vrhu. Podrobno smo proučili vpliv širine ekstrinzične baze na prebojno napetost tranzistorja, $BV_{CEO.}$ Kontroliramo lahko porazdelitev naboja akceptorjev intrinzične in ekstrinzične baze, da dosežemo popolnoma osiromašen kolektor. Senčenje električnega polja ekstrinzične baze čez intrinzičen spoj lahko uporabimo za omejitev najvišje vrednosti električnega polja vzdolž tokovne poti v osiromašenem področju spoja kolektor-baza, kakor tudi za povečanje prebojne napetosti $BV_{CEO.}$ Pojavita se dva vrhova električnega polja v osiromašenem področju spoja baza-kolektor. Področje, kjer pride do preboja, je odvisno od vrednosti električnega polja teh dveh vrhov, ki ju lahko kontroliramo s širino baze, w_{bext}.

1. Introduction

Recently, the extremely-thin silicon-on-insulator (SOI) has been marked as a potential CMOS technology for 22 nm node and below, /1/. Small parasitic capacitances inherent for SOI technology, good electrostatic behavior and low variability due to undoped channel promise a good solution for short channel effects (SCE) and scaling properties of such CMOS. This trend in IC industry will force SOI wafer manufacturers to improve wafer production in terms of lower defect density and reduced cost. It can be expected that wafer cost of not only ultra-thin-film SOI, but also thicker film SOI, will be reduced in the near future. In the past years, thin-film SOI technology has been proposed as a potential technology for radio-frequency (RF) system-on-chip (SoC) integration /2/, /3/. Excellent characteristics regarding the device isolation and small parasitic capacitances, as well as higher quality passives compared to bulk-silicon technologies, make this technology appropriate for low-power battery supplied applications like mobile phones, GPS, WiFi, etc. In order to achieve SoC level of integration for RF applications, bipolar transistors are desired in a technology platform due to their superior analog performance such as lower noise figure and higher gain. Vertical bipolar transistors in SOI may become prohibitively expensive due to more complex process /4/, which in addition to the higher cost of SOI wafers may result in a technology that is not economically viable. On the other hand, lateral bipolar transistors (LBTs) in SOI can be fabricated in a process that is less complex with the significant cost reduction compared to the vertical bipolar transistors, either in bulk or SOI substrates. It can be expected that cost of technology will be reduced further with the advance in SOI wafer manufacturing. Due to the nature of intrinsic base fabrication, which relies on the spacer technique and lateral redistribution of impurities, cutoff frequencies (f_T) of SOI LBTs above 20 GHz were not reported. The only LBT with reported state-of-the-art electrical performance is Horizontal Current Bipolar Transistor (HCBT) but it is fabricated in bulk-silicon wafers /5/. However, reported AC performance of SOI LBTs is still suitable for applications in microwave frequency range including the most important wireless application standards. Several LBT structures have been proposed so far and can be roughly categorized with respect to the base contact position as laterally contacted /6/, /7/, /8/ and top-contacted structures /2/, /3/, /9/, /10/. One benefit of placing the base contact on the top is that transistor length can be increased in the third dimension by the mask design if higher current drive is needed in the applications. In the case of laterally contacted base, i.e. two-sided base contact, transistor

operating current cannot be increased by increasing the emitter length, because the intrinsic base resistance would be increased. The ultimate result is that AC performance of the transistor is degraded through the reduction of maximum oscillation frequency (f_{max}). To overcome this issue, transistors of unit emitter size can be connected in parallel, which gives less flexibility in the circuit design. In order to achieve a SoC level of integration, transistors with different values of breakdown voltages should be available in a certain technology. In standard vertical transistors it is accomplished by the different parameters of the selectively implanted collector, which implies the usage of additional lithographic masks and results in an increased process complexity and ultimately higher cost of technology. On the other hand, in LBT structures with top contacted base, different values of breakdown voltages can be obtained by the mask design and the control of the width of the base contact region, i.e. extrinsic base width (w_{bext}), without any increase in the process complexity. In this paper, design tradeoff between cutoff frequency (f_T) and common-emitter breakdown voltage (BV_{CEO}), specific for SOI LBT structure with top-contacted base are analyzed by the device simulations. Physical mechanisms in the extrinsic base effect on transistor's breakdown voltage are analyzed in detail.

2. Simulation structure

A typical LBT structure such as the one reported in /2/ is analyzed by device simulation in MEDICI. The highest maximum oscillation frequency (f_{max}) and common emitter current gain (β) as well as the lowest base resistance (R_B) among all LBTs are reported for this structure. Cross-section of the device with marked geometrical parameters and the doping profile of the intrinsic transistor are shown in Fig. 1 and 2, respectively. Technological parameters are summarized in Table 1. Emitter height (h_E) is determined by the thickness of the silicon on insulator film and the small link-base region (l_b), which is defined during the extrinsic

Table 1. Technological and geometrical parameters of the soi lbt simulation structure

N_{ABext}, (cm^{-3})	N_{DC}, (cm^{-3})	N_{DE}, (cm^{-3})	w_{bext}, (nm)	l_b, (nm)	h_E, (nm)	d_{poly}, (nm)	d_E (nm)	d_C (nm)	d_{OX} (nm)
$2\cdot10^{20}$	$1.5\cdot10^{17}$	$1.8\cdot10^{20}$	500	70	120	200	300	500	300

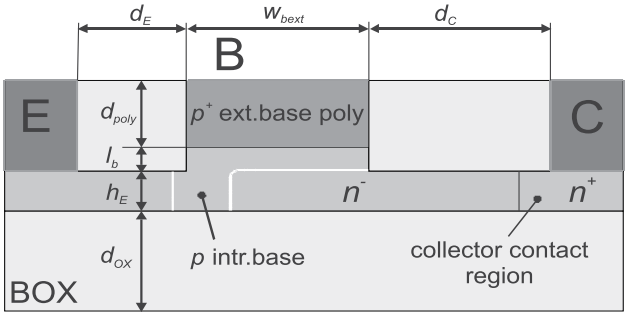

Fig. 1. Cross-section of the device simulation structure with marked geometrical parameters.

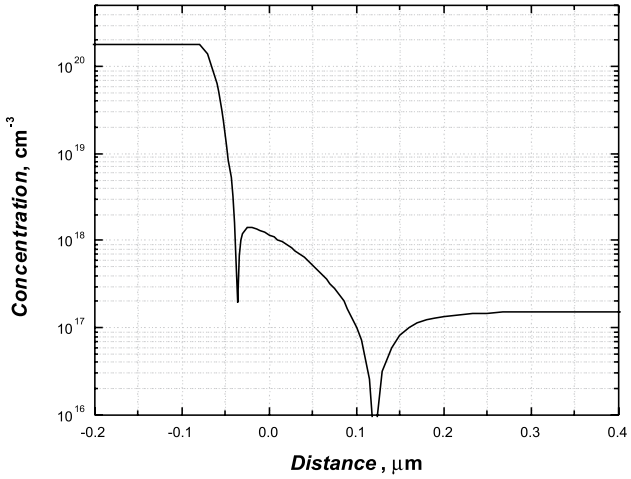

Fig. 2. Doping profile of the intrinsic transistor.

base polysilicon overetching. In this way, the extrinsic base profile, which is diffused from the extrinsic-base polysilicon, does not overlap the upper edge of the emitter, which could reduce the current gain and degrade base current ideality at lower base-emitter voltages due to the high-field effects and band to band tunneling /11/. Intrinsic transistor is formed by ion implantation of the intrinsic base and emitter, which are separated by the spacer formed on the sidewall defined during the extrinsic base polysilicon etching. Later on in the process, dopants are laterally diffused to form the final intrinsic transistor profile. This represents the fundamental limit on the control of the intrinsic base profile and basewidths cannot be scaled below 100 nm as it is routinely done in standard vertical bipolar transistors. Since the emitter region is not implemented in polysilicon, the distance between emitter contact and the base-emitter junction should be larger than the minority hole diffusion length in order to obtain smaller associated component of the base current and the larger current gain. The minimum distance between highly doped n^+ collector contact region, i.e. extrinsic collector, and the p^+ extrinsic base is limited by breakdown voltages of the transistor. Extrinsic base polysilicon should be highly doped and thick enough to suppress electron diffusion to the extrinsic base region, which could

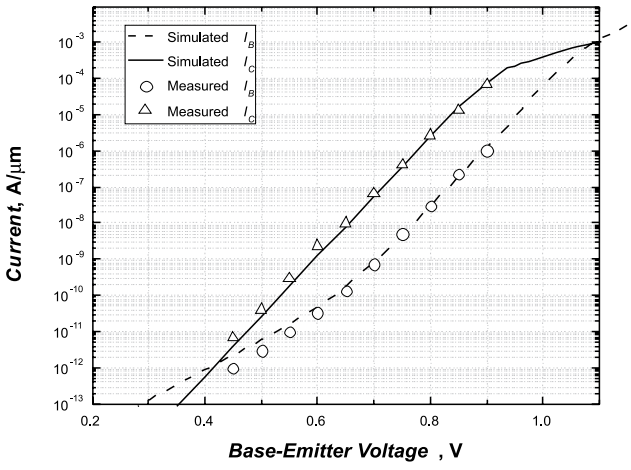

Fig. 3. Simulated Gummel characteristics. Measured data from /2/ is included for reference.

increase the base current and degrade the current gain (β). This structure has the base contact placed on the top and the base current is supplied only from one direction. Therefore, one-sided base contact is formed, which is not beneficial regarding the value of the base resistance (R_B). Nevertheless, the smallest R_B and the highest f_{max} value among SOI LBTs are reported for this structure, owing to a small thickness of SOI film and silicided base contact, which results in a small intrinsic component of the base resistance and a small contact resistance, respectively.

3. Simulation of electrical characteristics

Simulated Gummel characteristics of the transistor are presented in Fig. 3. Measured data is taken from /2/ for the reference. Doping profile in the intrinsic base is adjusted to get reasonable fit of the collector current. Summary of the simulated characteristics is given in Table 2.

Table 2. Summary of the simulated electrical characteristics

β	f_T, (GHz)	f_{max}, (GHz)	R_B, (Ω)	C_{jBC}, (fF)
83	12.7	67.1	250	1.55

3.1. Analysis of common emitter breakdown voltage and cutoff frequency

Tradeoff between speed and the breakdown voltage in bipolar transistors is well known. In order to suppress base widening at higher collector currents (i.e. Kirk effect) and to increase the cutoff frequency of the transistor (f_T), collector doping concentrations are increased, which results in a higher electric field in the base collector depletion region and lower value of breakdown voltages. Common emitter breakdown voltage (BV_{CEO}) is more important since it is typically 2 to 3 times lower than the common base breakdown voltage (BV_{CBO}) and is responsible for evaluation of transistor's safe operating area. The tradeoff is usually evaluated in terms of ($f_T BV_{CEO}$) product, bounded by the Johnson's limit /12/, which approximately equals 200 GHzV and 400 GHzV for implanted base and SiGe epi-base transistors, respectively /13/. Cutoff frequency (f_T) and common emitter breakdown voltage (BV_{CEO}) are simulated in MEDICI. f_T is calculated from AC analysis. *Y*-parameters are simulated and converted to *h*-parameters. f_T is determined as the frequency at which, h_{21} falls to unity. For evaluation of the common emitter breakdown voltage, base current reversal method in forced V_{BE} measurement is used /13/. Base-emitter voltage (V_{BE}) is set to 0.7 V and collector-emitter voltage (V_{CE}) is swept. BV_{CEO} is determined as the V_{CE} at which the base current changes the sign, i.e. turns from positive to negative. Non-local impact ionization model based on lucky electron model with hard threshold energy /14/ is used in simulations. All BV_{CEO} simulations are done with standard drift-diffusion model and the effects of self-heating are not considered. However, simulations are done for V_{BE} of 0.7 V at which collector current is small and no substantial self-heating is expected.

The unique geometry of LBTs with the base contact placed on the top results in a collector region which is surrounded by the extrinsic base from the top, the intrinsic base from one side and buried oxide from the bottom (Fig. 1). In the forward active mode of transistor operation, the base-collector junction is reversely polarized and the electric field is supported by the fixed charge in the depletion region. In the case of top contacted structure, there are two components of the electric field. Vertical component originates from the electric field lines which are terminated between collector donor charge and the extrinsic base acceptors, whereas horizontal component originates from the electric field lines which are terminated on the intrinsic base acceptors. Total amount of the collector charge is limited by the donor concentration in the collector and the thickness of the silicon on insulator film. This two-dimensional effect of collector charge sharing between extrinsic and intrinsic base acceptors, i.e. vertical and horizontal component of the electric field can be controlled in the way that collector becomes fully depleted and breakdown voltage improved for transistors with wider extrinsic base (w_{bext}).

At first, dependence of the BV_{CEO} on extrinsic base width (w_{bext}) is investigated. Simulations are done for the structures with different collector concentrations (N_{DC}). Intrinsic base profile is kept the same in the simulations, meaning that intrinsic base is narrower and current gain (β) slightly higher for transistors with higher collector concentration. Results are shown in Fig. 4. For the doping concentrations up to $2.5 \cdot 10^{17}$ cm^{-3} the effect of the BV_{CEO} improvement can be observed if the extrinsic base width (w_{bext}) is increased. BV_{CEO} value saturates for extrinsic base width larger than 0.8 μm. Therefore, engineering of the breakdown voltage by the mask design is possible for extrinsic base widths up to 0.8 μm. For collector doping concentrations larger than $2.5 \cdot 10^{17}$ cm^{-3}, breakdown voltages are sharply reduced and

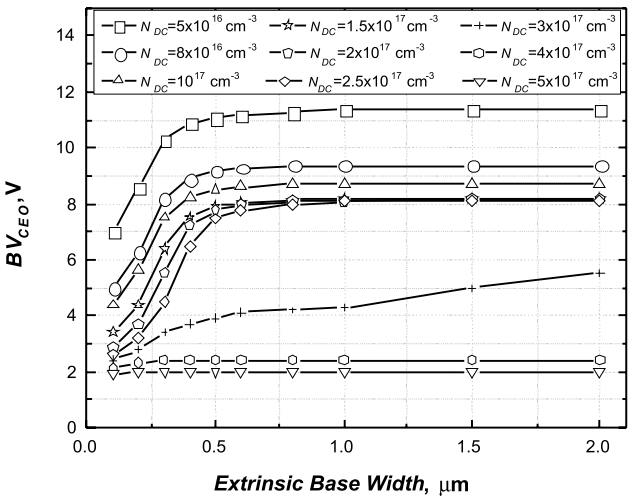

Fig. 4. Dependence of BV_{CEO} on the extrinsic base width (w_{bext}) for different collector concentrations.

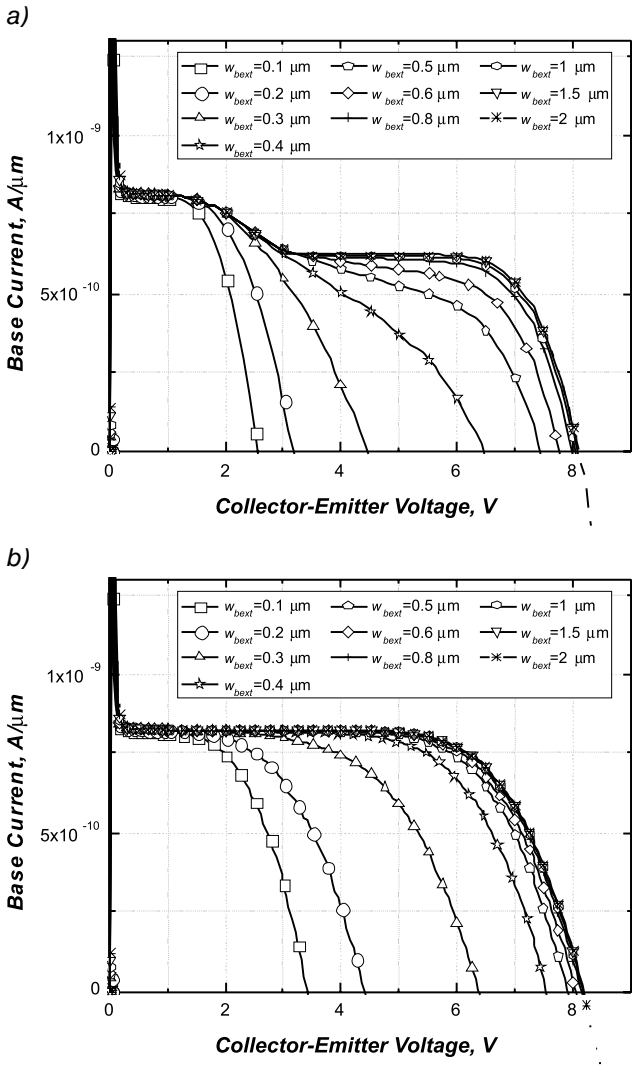

Fig. 5. Simulation of BV_{CEO} dependence on w_{bext} for: a) N_{DC}=2.5·10^{17} cm^{-3}, b) N_{DC}=1.5·10^{17} cm^{-3}.

cannot be improved by extending w_{bext}. BV_{CEO} simulations for collector concentrations of 2.5·10^{17} and 1.5·10^{17} cm^{-3} are shown in Fig. 5.a and 5.b, respectively. For collector concentration of 2.5·10^{17} cm^{-3} a plateau in the base current is observed for transistors with wider extrinsic base. These characteristics indicate that electric field has two peak values in the base-collector depletion region. The first peak appears at the intrinsic base-collector junction and approaches the value of the critical electric field at V_{CE} around 3 V. Weak avalanche starts and generated holes drift to the base side reducing the base current. However, peak electric field at the intrinsic base-collector junction is not increased for V_{CE} larger than 3 V and impact ionization is limited as indicated by the plateau in the characteristics for voltages between 3 and 7 V. This is explained by the full depletion of the collector region and the extrinsic base shielding effect. Impact ionization rate in the transistor for V_{CE} of 3 and 9 V is shown in Fig. 6.a and 6.b, respectively. For V_{CE}=3 V, just before full depletion of the collector, maximum impact ionization rate occurs at the intrinsic base-collector junction. When V_{CE} is further increased up to 9 V, another region with high impact ionization rate appears

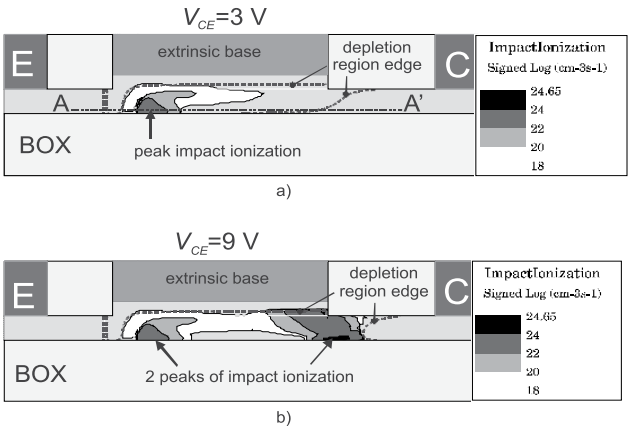

Fig. 6. Impact ionization rate for structure with N_{DC}=2.5·10^{17} cm^{-3} at V_{BE}=0.7 V and a) V_{CE}=3 V, b) V_{CE}=9 V.

in the drift region to the right side of the extrinsic base. Maximum rate occurs in the bottom part near the buried oxide interface since electrons are pushed down by the vertical component of field and current is crowded near the buried oxide interface. Since the holes generated by impact ionization drift to the base side and are injected to the emitter, a positive feedback of electrons due to transistor's current gain (β) occurs and causes BV_{CEO} to be 2 to 3 times lower than BV_{CBO}. Moreover, for BV_{CEO} to occur the critical electric field has to appear along the current path since the avalanche multiplication process is initiated by mobile electrons. Simulated distribution of electric potential, field and impact ionization rate for different V_{CE} in the plane AA' from Fig. 6. are shown in Fig. 7.a-c. From the potential distribution in Fig. 7.a it can be observed that collector is not fully depleted for V_{CE} below 3 V. Potential is constant across neutral collector region below extrinsic base and electric field is zero. Potential drop appears across depletion region and peak electric field is placed at the intrinsic base-collector junction (Fig. 7.b). For V_{CE} of 4 V and above, the collector under the extrinsic base is fully depleted. Characteristics of potential distribution bends and deviates from standard square function in the area below the extrinsic base and electric field magnitude in that area is reduced. Furthermore, the potential drop across the intrinsic-base-collector junction practically doesn't increase with V_{CE} and the peak of the electric field at intrinsic base-collector junction is constant (Fig. 7.b). Since the collector charge under the extrinsic base is completely shared, there is no available charge to support increase of potential and electric field across the intrinsic base-collector junction. The rest of the potential drop appears across the drift-region on the right side with respect to the extrinsic base-collector junction. Electric field vectors for transistors with w_{bext} of 0.5 μm and 1 μm are shown in Fig. 8.a and 8.b, respectively. Direction of the vectors indicates the direction of the electric field, whereas length of the vectors is proportional to the magnitude of the electric field, i.e. density of the electric field lines in given points of the structure. In case of w_{bext}=0.5 μm, a part of the field lines terminated on the intrinsic base acceptors are originated from donors in the

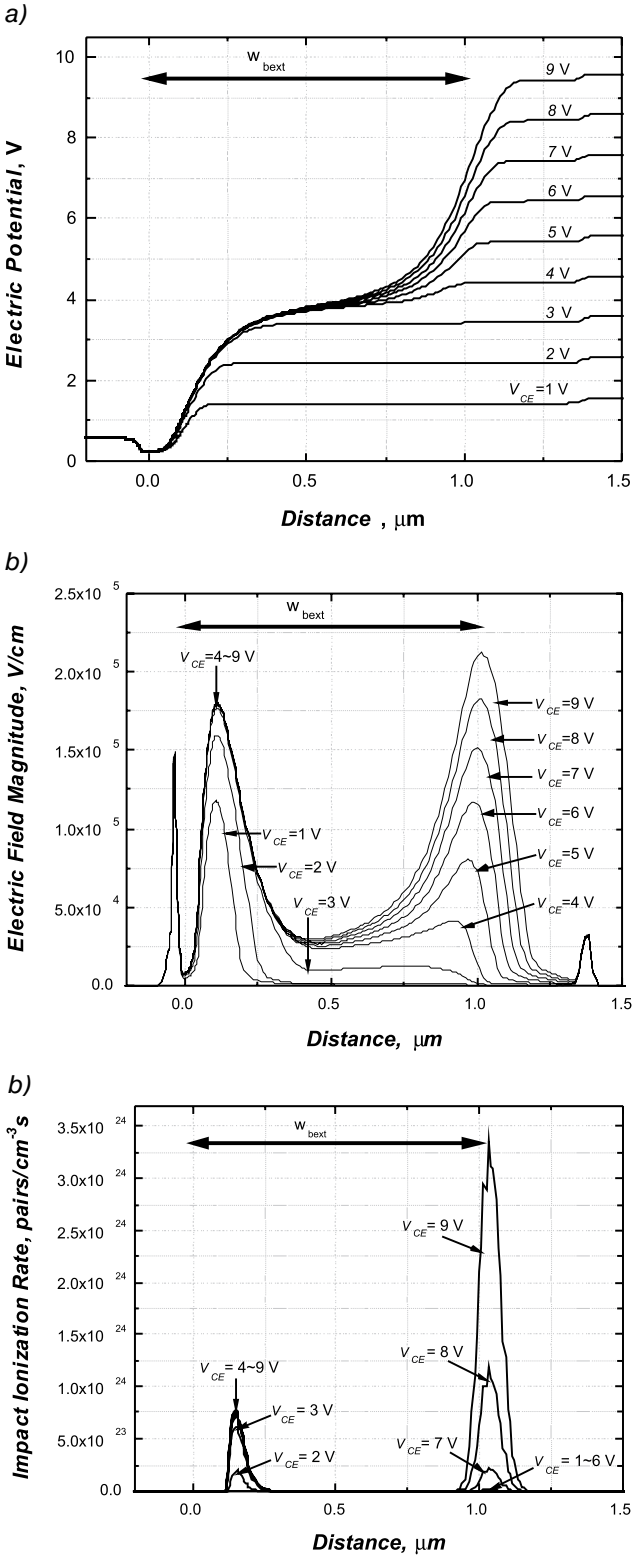

Fig. 7. Distribution of: a) electric potential, b) electric field, c) impact ionization rate dependence on V_{CE} in the bottom part of the transistor, in the plane marked AA' in Fig.6. 15 nm from the buried oxide. Extrinsic base is located between 0 and 1 μm.

drift region, which can be observed as a longer horizontal arrows in Fig. 8a. Therefore, horizontal electric field is only partially shielded by the vertical field and the peak value

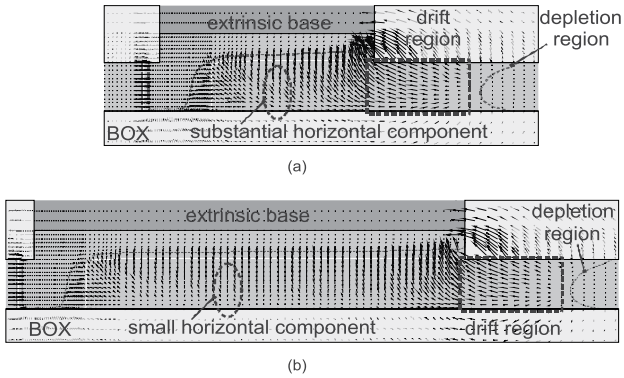

Fig. 8. Electric field lines at V_{CE}=8 V for structures with a) w_{bext}=0.5 μm and b) w_{bext}=1 μm

at the intrinsic junction can be increased with V_{CE} but at a slower rate. Shielding is more efficient for larger w_{bext} and the current generated by impact ionization is smaller, which can be observed as a smaller reduction of the base current in Fig. 5.a and the appearance of the plateau in the characteristics. For w_{bext}=1 μm, intrinsic base electric field, which has only horizontal component is completely terminated between donors below the extrinsic base and the intrinsic base acceptors, which is observed as a shorter horizontal arrows in Fig. 8b. Therefore, horizontal electric field is effectively shielded by the extrinsic base vertical field and cannot be further increased with V_{CE}. Density of electric field lines that are terminated on the extrinsic base acceptors is increased in the area next to the drift region, since there is more available donor charge in the area toward extrinsic collector. Field lines originated from donors in the drift region are spread laterally through the drift region and then bent upwards and terminated on the extrinsic base acceptors. Electric field associated with the extrinsic base-collector junction has vertical and horizontal component. The result of this effect is that the second peak of the electric field appears in the drift region as it can be observed in Fig. 7.b. For larger w_{bext}, if V_{CE} is further increased, critical field is exceeded in the drift region and transistor breakdown occurs. From the impact ionization rate shown in Fig. 7.c it can be seen that two regions of the high impact ionization rate associated with two peaks of the electric field, appear in the transistor. The first one is at the intrinsic base-collector junction, which does not increase substantially for voltages above 3 V, whereas the second is placed in the drift region and increases rapidly for V_{CE} above 7 V. These observations are in a good agreement with the characteristics shown in Fig. 5.a. In the case of the characteristics in Fig. 5.b for collector concentration of $1.5 \cdot 10^{17}$ cm^{-3} the peak of the electric field at the intrinsic base-collector junction does not approach the critical value and no substantial impact ionization occurs in this region. Critical electric field is achieved in the drift region only and no plateau in the characteristics in Fig. 5.b is observed.

Influence of the collector concentration on the cutoff frequency (f_T) is simulated as well and the results are shown in Fig. 9. As expected, f_T is increased for higher collector concentrations. This is attributed to the narrower intrinsic

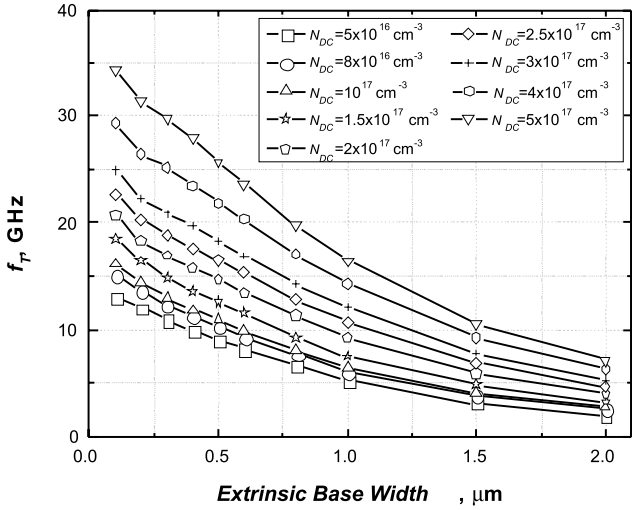

Fig. 9. Dependence of the cutoff frequency (f_T) on extrinsic base width (w_{bext}) for different collector concentrations.

base and the shorter base transit time. In addition, Kirk effect is pushed to higher current densities. It is also observed that f_T decreases for larger w_{bext}. This can be explained by the influence of the vertical electric field on the current flow under the extrinsic base. Electrons flowing through the base-collector depletion region are pushed down by the vertical electric field toward buried oxide and local current density is increased causing the Kirk effect to appear at lower values of the collector current. Furthermore, in the case of fully depleted collector, electrons have to travel through the wider depletion region, which results in a longer transit time. Both effects reduce cutoff frequency.

Influence of the distance between n^+ extrinsic collector and the p^+ extrinsic base is also investigated. BV_{CEO} dependence on w_{bext} is shown in Fig. 10. It can be seen that BV_{CEO} can be increased for larger w_{bext}. However, BV_{CEO} saturates at smaller value if the distance between collector contact and extrinsic base (d_c) is reduced. This is explained by

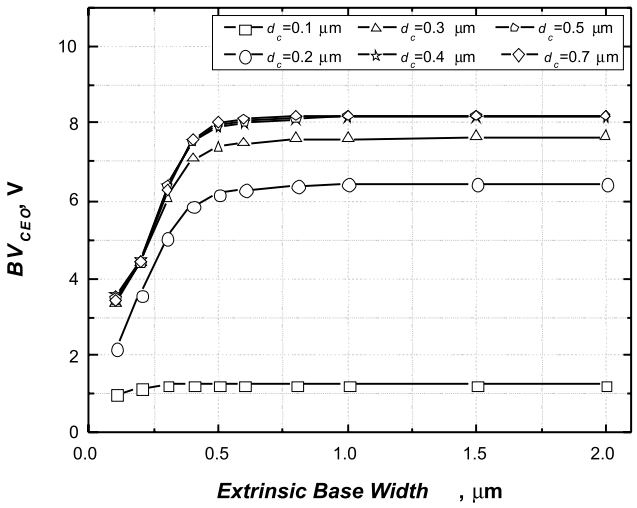

Fig. 10. Dependence of BV_{CEO} on w_{bext} for different distances between n^+ collector and p^+ extrinsic base (d_c).

the reduced depletion region width if n^+ region is brought closer to the p^+ extrinsic base. Electric field is increased in the drift region and breakdown occurs at lower collector-emitter voltages. It can also be observed that the increase of BV_{CEO} with d_c saturates at d_c=0.4 μm. Obviously, for larger values of d_c, the base-collector depletion region does not reach n^+ extrinsic collector and does not cause an increase of the electric field in the drift region. Influence of d_c on cutoff frequency is also investigated. However, less than 5% improvement in f_T can be achieved by bringing the n^+ collector contact region closer to the extrinsic base.

3.2. Emitter height dependence

Dependence of the BV_{CEO} and f_T on the emitter height (h_E) is investigated next. Link base length (l_b) of 70 nm and collector concentration of $1.5 \cdot 10^{17}$ cm^{-3} are kept constant in the simulations. Intrinsic transistor profile from Fig. 2 is used in simulations. In the real process, h_E would be determined by the thickness of the silicon on insulator film. Dependence of BV_{CEO} on h_E with w_{bext} as a parameter is shown in Fig. 11. It can be observed that BV_{CEO} is increased with h_E as long as collector is fully depleted for collector-emitter voltage that is lower than the breakdown voltage. Since the extrinsic base shielding effect is stronger for larger w_{bext}, BV_{CEO} has the tendency of rise even for larger values of h_E. For larger w_{bext}, electric field lines of the horizontal component of field are completely terminated between intrinsic base acceptors and donors below extrinsic base and there is no penetration of the horizontal field associated with intrinsic base-collector junction all the way to the drift region. Magnitude of the electric field for structures with h_E of 0.2 μm and w_{bext} of 1 μm and 0.5 μm are presented in Fig. 12.a and 12.b, respectively. It can be seen that for structure with w_{bext}=1 μm peak electric field at the intrinsic base-collector junction rises for V_{CE} voltages up to 5 V and after that it is practically constant. Horizontal field is shielded by the extrinsic base vertical field completely. If V_{CE} is increased further, the second peak of the electric field appears in the drift region and causes the transistor breakdown to occur when critical field is reached. For structure with w_{bext}=0.5 μm,

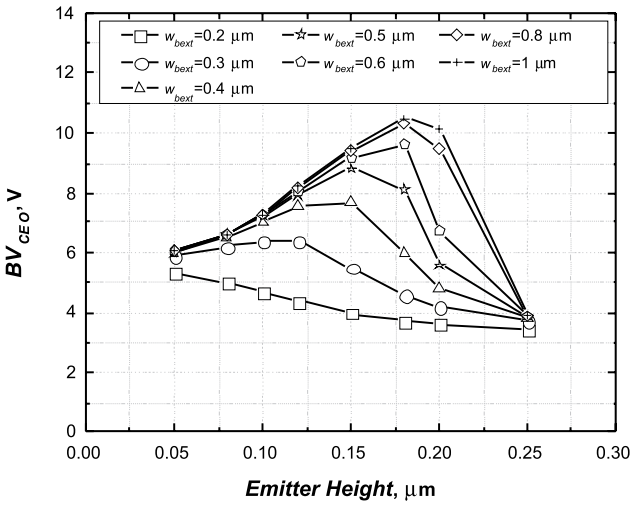

Fig. 11. Dependence of BV_{CEO} on h_E for different w_{bext}.

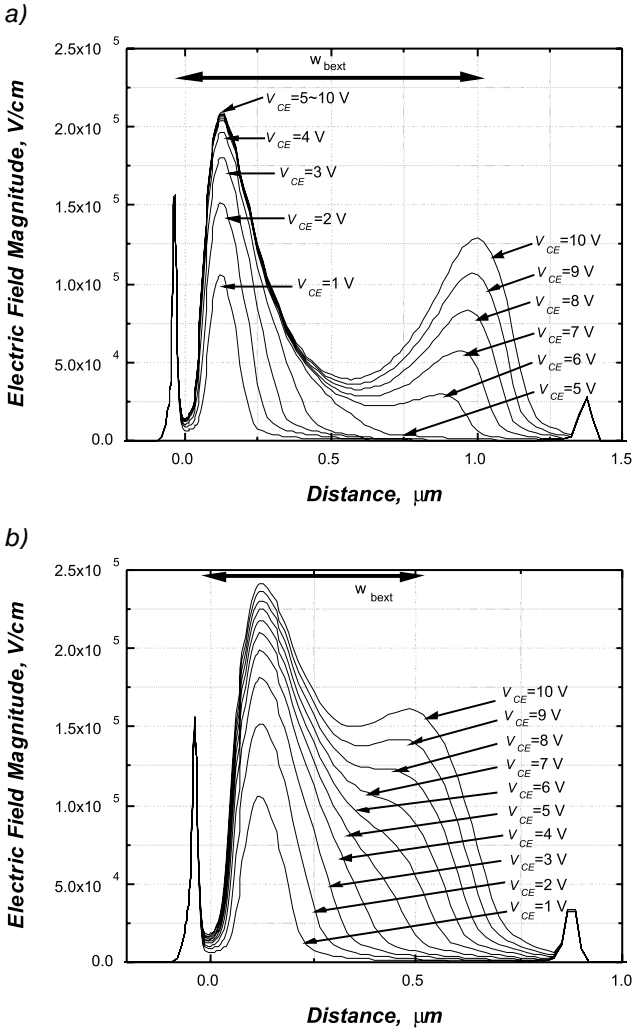

Fig. 12. Electric field in the transistor 15 nm from buried oxide for structure with $N_{DC}=1.5\cdot10^{17}$ cm^{-3}, $h_E=0.2$ μm and a) $w_{bext}=1$ μm, b) $w_{bext}=0.5$ μm.

the extrinsic base shielding is not complete. Peak electric field at the intrinsic base-collector junction increases even for voltages greater than 5 V and can reach the critical value for transistor breakdown. Since part of the electric field lines originated from donors in the drift region to the right side of the extrinsic base are terminated at extrinsic base acceptors, there are more available donor charge below extrinsic base which can support horizontal electric field over the intrinsic base-collector junction. Horizontal field penetrates toward the drift region and the peak at the intrinsic base-collector junction is increased. Avalanche multiplication and transistor breakdown occur at the intrinsic base-collector junction.

In addition, for larger w_{bext} current flows over a longer distance under the influence of vertical electric field and is pushed down to the buried oxide interface. Therefore, current flows through the part of the drift region where magnitude of the electric field is smaller compared to the upper part, closer to the p^+ extrinsic base region, resulting in a lower impact ionization rate.

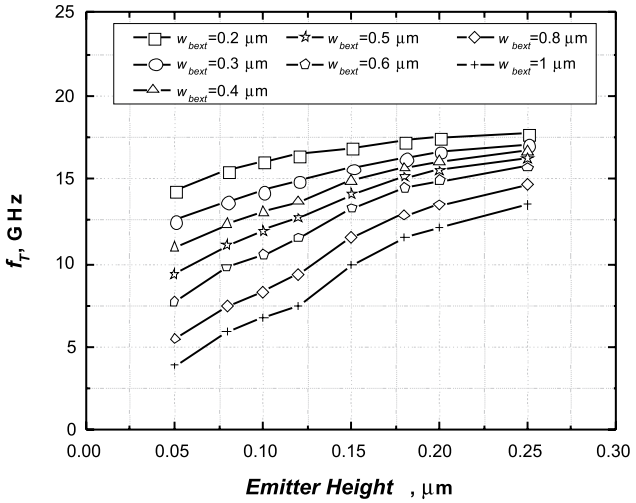

Fig. 13. Dependence of f_T on h_E for different w_{bext}.

As h_E is reduced, the amount of the available donor charge under the extrinsic base is reduced and voltage drop associated with vertical electric field is smaller. Therefore, a larger voltage drop appears laterally across the drift region and critical electric field for avalanche multiplication in the drift region is reached at lower V_{CE}, causing the decrease in BV_{CEO}. For the largest values of h_E, BV_{CEO} decreases since collector is not fully depleted any more.

Simulation results of f_T dependence on h_E for different w_{bext} is presented in Fig. 13. For larger h_E, f_T is increased. As h_E is increased, cross-section of the neutral collector is increased and current crowding due to vertical field influence is less pronounced. Kirk effect is pushed to higher collector currents as local current density is reduced and f_T is increased. The current crowding effects are more pronounced for structures with larger w_{bext} which can be observed as a smaller value of f_T in Fig. 13. In addition, electrons are traveling through the wider depletion region increasing the associated transit time. For w_{bext} larger than 0.5 μm the transit time through the depletion region becomes comparable to the base transit time. Furthermore, time constant associated with the collector-base capacitance and the collector resistance i.e. R_CC_{BC} is increased for larger w_{bext}, which further reduces f_T.

3.3. Link-base length dependence

Influence of the link-base length (l_b) on BV_{CEO} and f_T is also investigated. Emitter height (h_E) is kept constant at 120 nm and collector concentration is set to $1.5\cdot10^{17}$ cm^{-3}. By increasing l_b, thickness of the *n*-collector under the extrinsic base is increased and a higher collector-emitter voltage is needed to reach full depletion of the collector region. Simulation results for BV_{CEO} dependence on l_b with w_{bext} as a parameter are shown in Fig. 14. For larger w_{bext}, shielding by the extrinsic base field is more efficient and higher BV_{CEO} values are observed. This dependence is similar to the dependence on h_E, since in both cases the amount of collector charge is changed by the variation in the thickness of the *n*-collector below the extrinsic base. Results of

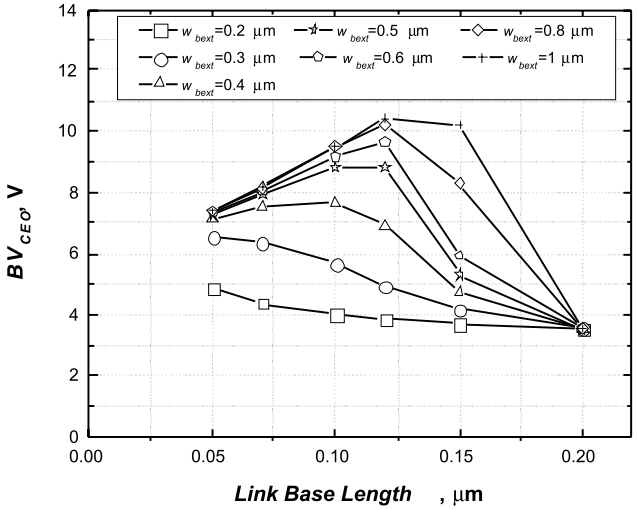

Fig. 14. Dependence of BV_{CEO} on link-base length (l_b) for different w_{bext}.

f_T dependence on l_b are presented in Fig. 15. showing the similar behavior as dependence on h_E. Current crowding effects are relaxed by increasing the link-base length and f_T is improved. Degradation of f_T by current crowding is more severe in the case of larger w_{bext} as seen from Fig. 15.

4. Conclusions

LBT structure with the base contact on top is analyzed by the device simulations. Influence of the extrinsic base width (w_{bext}) on common-emitter breakdown voltage (BV_{CEO}) and cutoff frequency (f_T) is examined in detail. The effect of collector charge sharing can be used to obtain structures with different values of BV_{CEO} and f_T. Total amount of collector charge is determined by the collector concentration and the silicon film thickness, which can be controlled to achieve full depletion of the collector region. In case of fully depleted collector, two peaks of the electric field appear along the current path in the base-collector depletion region. The first one is at the intrinsic-base collector junction and the second one in the drift region toward extrinsic collector. Extrinsic base shielding effect can be used to control the value of the peak electric field at the intrinsic-base collector junction. For smaller w_{bext}, the horizontal field associated with the intrinsic base junction is partially shielded and the peak electric field increases with V_{CE}. In case of larger w_{bext}, shielding is more effective; the peak electric field increases at slower rate with V_{CE} and approaches the critical value for avalanche multiplication at higher V_{CE}. In both cases avalanche occurs at the intrinsic-base collector junction but BV_{CEO} is increased for larger w_{bext} due to smaller increase of the peak electric field with V_{CE}. For very large w_{bext}, horizontal field is completely shielded by the vertical field and the peak electric field at the intrinsic base junction does not increase with V_{CE}. However, the second peak in the drift region increases with V_{CE} and can reach the critical value for avalanche multiplication. Transistor breakdown occurs in the drift region for transistors with larger w_{bext}. It is shown that BV_{CEO} engineering can be achieved for w_{bext} below 0.8 μm. Tradeoff between breakdown (BV_{CEO}) and transistor's cutoff frequency (f_T) is presented and design guidelines regarding collector concentration and transistor geometry is given. The potential of BV_{CEO} engineering for top contacted SOI LBT structure without additional increase in cost of technology is demonstrated.

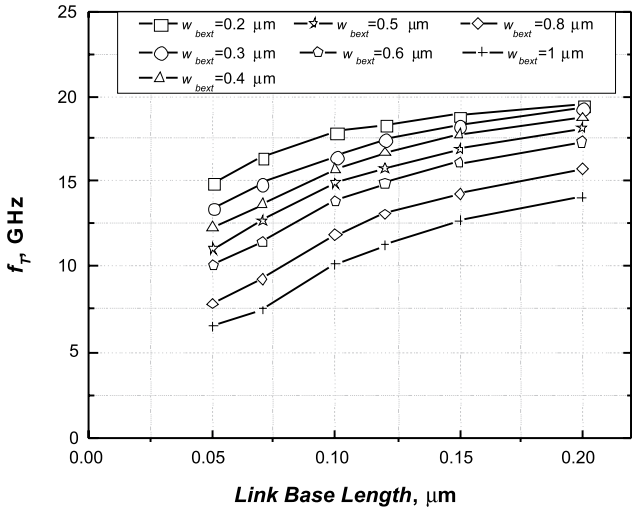

Fig. 15. Dependence of f_T on link-base length (l_b) for different w_{bext}.

References

/1/ K. Cheng, A. Khakifirooz, P. Kulkarni, S. Ponoth, J. Kuss, D. Shahrjerdi, L. F. Edge, A. Kimball, S. Kanakasabapathy, K. Xiu, S. Schmitz, A. Reznicek, T. Adam, H. He, N. Loubet, S. Holmes, S. Mehta, D. Yang, A. Upham, S.-C. Seo, J. L. Herman, R. Johnson, Y. Zhu, P. Jamison, B. S. Haran, Z. Zhu, L. H. Vanamurth, S. Fan, D. Horak, H. Bu, P. J. Oldiges, D. K. Sadana, P. Kozlowski, D. McHerron, J. O'Neill, B. Doris, "Extremely Thin SOI (ETSOI) CMOS with Record Low Variability for Low Power System-on-Chip Applications", *IEDM Tech. Dig.,* 2009, pp. 49-52

/2/ H. Nii, T. Yamada, K. Inoh, T. Shino, S. Kawanaka, M. Yoshimi, Y. Katsumata, "A Novel Lateral Bipolar Transistor with 67 GHz f_{max} on Thin-Film SOI for RF Analog Applications", *IEEE Trans. Electron Devices,* Vol. 47, No. 7, pp. 1536–1541, July 2000.

/3/ M. Sun, W. T. Ng, K. Kanekiyo, T. Kobayashi, H. Mochizuki, M. Toita, H. Imai, A. Ishikawa, S. Tamura, K. Takasuka, "Lateral High-Speed Bipolar Transistors on SOI for RF SoC Applications", *IEEE Trans. Electron Devices,* Vol. 52, No. 7, pp. 1376–1383, July 2005.

/4/ J. Cai, M. Kumar, M. Steigerwalt, H. Ho, K. Schonenberg, K. Stein, H. Chen, K. Jenkins, Q. Ouyang, P. Pldiges, and T. Ning, "Vertical SiGe-base bipolar transistors on CMOS-compatible SOI substrate", Proc. Bipolar/BiCMOS Circuits Technol. Meeting, 2003, pp. 215–218.

/5/ T. Suligoj, M. Koričić, H. Mochizuki, S. Morita, K. Shinomura, and H. Imai, "Horizontal Current Bipolar Transistor (HCBT) with a Single Polysilicon Region for Improved High-Frequency Performance of BiCMOS ICs," IEEE Electron Device Lett., in press.

/6/ S. A. Parke, C. Hu, P. K. Ko, "A High-Performance Lateral Bipolar Transistor Fabricated on SIMOX", *IEEE Electron Device Letters*, Vol. 14, No. 1, pp 33-35, January 1993.

/7/ T. Shino, K. Inoh, T. Yamada, H. Nii, S. Kawanaka, T. Fuse, M. Yoshimi, Y. Katsumata, S. Watanabe, J. Matsunaga, "A 31 GHz *f*max Lateral BJT on SOI Using Self-Aligned External Base Formation Technology", *IEDM Tech. Dig*., 1998, pp 953-956.

/8/ R. Dekker, W.T.A. v.d. Einden, H.G.R. Maas, "An Ultra Low Power Lateral Bipolar Polysilicon Emitter Technology on SOI", *IEDM Tech. Dig*., 1993, pp 75-78.

/9/ G. G. Shahidi, D. D. Tang, B. Davari, Y. Taur, P. McFarland, K. Jenkins,D. Danner, M. Rodriguez, A. Megdanis, E. Petrillo, M. Polcari, and T. H. Ning, "A novel high-performance lateral bipolar on SOI", *IEDM Tech. Dig.,* 1991 pp. 663-666.

/10/ W. L. M. Huang, K. M. Klein, M. Grimaldi, M. Racanelli, S. Ramaswami, J. Tsao, J. Foerstner, B. C. Hwang, "TFSOI Complementary BiCMOS Technology for Low Power Applications", *IEEE Trans. Electron Devices,* Vol. 42, No. 3, pp. 506–512, March 1995.

/11/ J. M. Stork, R. D. Isaac "Tunneling in Base-Emitter Junctions", *IEEE Trans. Electron Devices,* Vol. 30, No. 11, pp. 1527–1534, July. 1983.

/12/ E. O. Johnson, "Physical limitations on frequency and power parameters of transistors," *RCA Rev.*, Vol. 26, pp. 163-177, 1965.

/13/ J. D. Cressler, G. Niu, *Silicon-germanium Heterojunction Bipolar Transistors*, Artech House,2003.

/14/ C.Jungemann, R.Thoma and W.L.Engl, "A Soft Threshold Lucky Electron Model for Efficient and Accurate Numerical Device Simulation," Solid-State Electronics, Vol. 39, No. 7, pp.1079-1086, 1996.

Marko Koričić*, Tomislav Suligoj
Department of Electronics, Microelectronics, Computing and Intelligent Systems, Faculty of Electrical Engineering and Computing, University of Zagreb, Unska 3, HR-10000 Zagreb, Croatia

* Corresponding author.
Tel.: +385-1-6129671, fax.: +385-1-6129653,
e-mail address: marko.koricic@ fer.hr

Prispelo: 27.05.2010 *Sprejeto: 24.06.2011*