EXPERIMENTAL INVESTIGATION OF Si-SiO_2 INTERFACE TRAPS USING EQUILIBRIUM VOLTAGE STEP TECHNIQUE

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Key words: Si-SiO_2 interface traps; Equilibrium Voltage Step technique; traps.

Abstract: The concentration profile of Si-SiO_2 interface traps in metal-oxide-semiconductor transistors has been studied using an equilibrium voltage step techniques. The Equilibrium Voltage Step (EVS), usually applied to extract the slow states profile in 3 dimensions, was used to deduce the in-depth profile of the slow states of the Si-SiO_2 interface. The profile of the slow states decreased between 7Å and 17Å awing.

Eksperimentalne raziskave pasti na mejni plasti Si-SiO_2 z uporabo napetostne tehnike EVS

Kjučne besede: pasti na meji Si-SiO_2 , napetostna tehnika EVS, pasti

Izvleček: V prispevku preučujemo koncentracijski profil pasti na meji Si-SiO_2 v MOS tranzistorju z uporabo napetostne tehnike EVS. Tehniko EVS, ki jo običajno uporabimo za študij počasnih energijskih stanj v treh dimenzijah, smo tokrat uporabili za določanje globinskega profila le-teh na meji Si-SiO_2. Ugotovili smo, da koncentracija počasnih stanj močno pade na razdalji med 7Å in 17Å od meje.

1. Introduction

Because of their limitation on the scaling of SiO_2 based metal-oxide semiconductors (MOS), the understanding of Si-SiO_2 interface traps is necessary. Many methods and theoretical models have been proposed to study Si-SiO_2 interface traps. The "1/f" noise method was the first technique, which supposed a distribution of traps in the direction of the oxide /1-2/. Recently, different methods have been proposed for the study of slow states /3-5/. A capture time constant distribution of traps has been confirmed by Bauza et al /6/, using the in-depth approach of charge pumping. This technique consists of measuring the charge pumping current as a function of frequency evaluated at the maximum of the Elliot curves. The Equilibrium Voltage Step (EVS) technique, developed by Tanner et al /5/, has been used to simultaneously extract the trap response time, density and energy in the silicon band gap of traps located near the Si-SiO_2 interface. The technique is simple and direct and consists of scanning the gate voltage of a MOS capacitor with different delay times and then measuring the resulting current transients. In this article, the trap profile, assuming only pure tunneling for capture, using data obtained by the EVS techniques.

2. Extraction of Si-SiO_2 interface trap profile using the equilibrium voltage step technique

The EVS technique has been mainly used to characterize slow traps in the Si-SiO_2 interface/4/. Then, it was extended to extract slow trap profiles in MOS capacitors with plasma damaged oxides /10/ and with NO and N_2O nitride oxides grown on Si and SiC substrates /11/. It has been later validated by Spillane et al. /12/.

This technique is based on the extraction of the current-voltage-time information in MOS capacitors /4/. It consists of scanning the gate voltage in a staircase manner and then measuring the resulting current transients after a delay time which is composed of the measurement time of the instrument, t_0 and a time td which is adjusted by the operator. The transient current measured at time $t_0 + t_d$ corresponds to the trap density with that response time. After scanning the gate voltage with different delay times, it is possible to extract directly the trap density as a function of response time at each energy position in the silicon band gap.

To extract the slow trap profile, the measured transient substrate current shown in Fig. 1 is divided by ($q \times A \times \Delta E$), where q is the absolute electronic charge, A the area of the gate and ΔE the change in the surface Fermi level resulting from the gate voltage step.

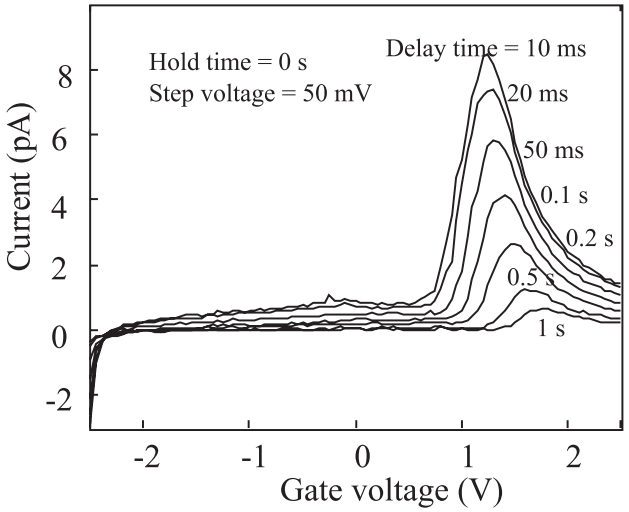

Fig 1: Transient substrate current due to the gate v oltage step at different delay times (p-type substrate MOS capacitor).

If we consider a set of slow traps at the Fermi level at equilibrium, then the capture time constant is equal to the emission time constant $\tau_c=\tau_e$ such that :

$$\tau = \frac{1}{n\sigma v_{th}} \quad (1)$$

where σ is the capture cross section, n the carrier concentration at the surface and Vth the carrier thermal velocity. If we suppose a uniform distribution of traps into the oxide, then according to the Heiman-Wrafield tunneling model /9/, the capture cross section at distance x from the interface can be written as:

$$\sigma(x) = \sigma(0)\exp(\frac{-x}{\lambda}) \quad (2)$$

Then, solving for the tunneling depth x we find /12/:

$$x = \lambda\left[\ln(N_c v_{th}\sigma(0)\tau) - (E_c - E_F)/KT\right] \quad (3)$$

where N_c is the effective density of states in the conduction band, (E_c –E_F) the Fermi energy level relative to the conduction band and KT is the thermal energy.

We assume that traps are distributed through the oxide both in energy and space with density N_t. By stepping the gate voltage, the Fermi energy changes by an amount ΔE If the device is in equilibrium before the step, then after the voltage step traps up to depth x will have changed charge (through emission or capture processes). Thus, the number of these states per unit area can be written as :

$$N(x) = xN_t\Delta E \quad (4)$$

Introducing the expression of the tunneling depth x in Equation (2) and solving for N_t we get:

$$N_t = \frac{I_{sub}(t)t}{\lambda Aq\Delta E} \quad (5)$$

where $I_{sub}(t)$ is the transient current measured at the substrate.

In this part, a MOS p-type capacitor with a thick oxide is used. When the surface of the semiconductor is swept from accumulation to inversion using a staircase gate signal with increment V_{step}= 50 mV, and a variable delay time from 10ms to 2s, we obtain positive transient current peaks attributed to emission of holes to the substrate, this peak decreases as the delay time increases, as shown in Fig.3. Applying the model of Tanner et al. /4/, which consists of dividing the measured current density by (q x ΔE), where q is the absolute electronic charge and ΔE the energy swept by the surface Fermi level, one obtains the 3D trap profile illustrated in Fig.2. This figure is attributed to the slow trap profile having response times from 70 ms to 2060 ms (since the measuring time of the instrument is 60ms). One can see the existence of a peak at 0.25 eV above the mid-gap which decreases as the response time is increased. This device has a Dit value of 10^{12} $ev^{-1}cm^{-2}$ measured using a conventional charge pumping technique. By applying now the theory of charge tunneling through energy barriers, one obtains the in-depth profile of traps, as shown in Fig.3.

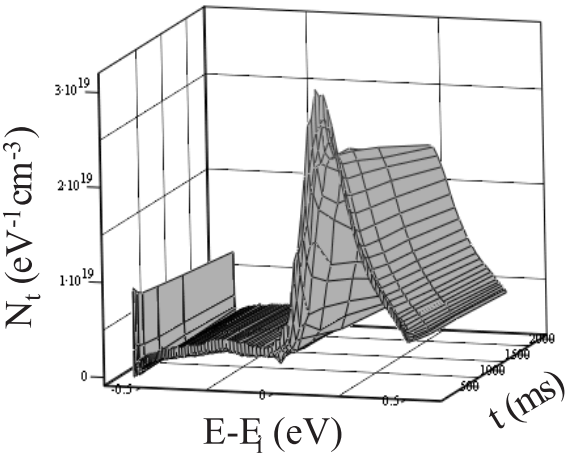

Fig 2: 3D slow trap profile of a p-type substrate MOS capacitor measured with delay times between 10 ms and 2s.

3. Resultants and discussion

The EVS technique allows the exploration of trap concentration into the oxide near the Si-SiO_2 interface, between 7 and 17Å, which corresponds to slow traps. Nevertheless, the charge pumping technique not only explores these types of traps, represented by the plateau of the profile, but probes also the fast states, which correspond to the exponential part of the profile /14/. The difference between the two techniques is that in charge pumping we measure a constant value of trap concentration for tunneling depth greater than 5 to 6Å, while with EVS we measure a decreasing value of the trap concentration between 7 and 17Å into the oxide. Another main difference concerns the energetic distribution of traps probed by each technique. The CP interface states located up to ±0.42eV around the mid-gap of silicon, depending on measuring conditions /13-14/, contribute to the recombination process and hence to the charge pumping current. However, in the EVS technique only slow traps located at specific energy

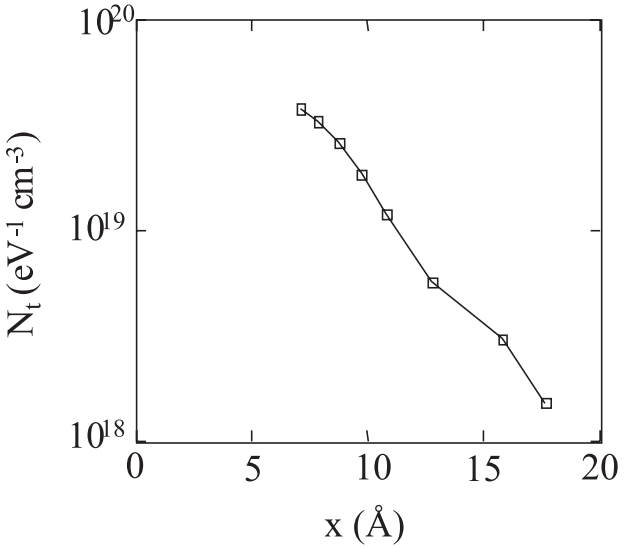

Fig. 3: Tunneling depth distribution obtained from the measured 3D profile of Fig. 2.

levels in the silicon band-gap contribute to the measured transient current.

4. Conclusion

The EVS technique has proven to be a simple and direct tool to simultaneously measure both the energy and response time distribution of traps located in the oxide near the Si-SiO_2 interface by scanning the gate voltage with different delay times. By applying the theory of carrier tunneling through energy barriers, the trap response time has been related to the tunneling depths into the oxide. The EVS technique only the slow traps located near the Si-SiO_2 interface and at specific energy levels in the silicon mid-gap are probed. This profile shows a decreasing trap concentration between 7 and 17Å from the Si-SiO_2 interface.

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