UWB FAST-HOPPING CARRIER FREQUENCY GENERATOR

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Key words: Ultra Wide band (UWB), NMOS switch, oscillator, multi-band OFDM alliance (MBOA)

Abstract: This paper discusses on the UWB carrier frequency generator that is capable of fast switching between different center frequencies. By using a switching network, the different frequencies from different local oscillators are switched within 4ns. A new topology of NMOS switch based on series-shunt configuration is proposed so that it is able to pass the signal from oscillators to output without transition spike. The performance of our carrier frequency generator is estimated through post layout simulation with a target technology of Silterra 0.18 µm CMOS at a supply voltage of 1.8 V. The post layout simulation results indicate that our carrier frequency generator is able to produce a signal with three center frequencies, i.e. 3432 MHz, 3960 MHz, and 4488 MHz at 400mV peak-to-peak swing within every 4ns.

Zelo hiter generator nosilne frekvence

Kjučne besede: širokopasovni, UWB, NMOS stikalo, oscilator, MBOA združenje, multi-band OFDM alliance

Izvleček: V članku je predstavljen UWB generator nosilne frekvence, ki je zmožen hitrega preklapljanja med različnimi centralnimi frekvencami. Z uporabo stikalnega vezja uspemo v času 4ns preklopiti različne frekvence iz različnih lokalnih oscilatorjev. V prispevku predstavimo novo tipologijo NMOS stikala, ki omogoča prenos signala od oscilatorja do izhoda brez prehodne špice. Delovanje generatorja nosilne frekvence smo ovrednotili s simulacijami na osnovi parametrov 0.18 µm CMOS tehnologije Silterra pri napetosti 1.8 V. Rezultati nam pokažejo, da je generator sposoben proizvesti signal s tremi centralnimi frekvencami in sicer 3432 MHz, 3960 MHz in 4488 MHz vsake 4ns z vrhnjo napetostjo 400mV.

1. Introduction

The center frequencies for the three mandatory bands (i.e., "mode-1") for MBOA are 3432 MHz, 3960 MHz, and 4488 MHz /1/, /2/. The MBOA proposal assumes per-OFDM-symbol frequency hopping over these bands with a transition time below 9.5 ns, while remaining in a band for around 300 ns. Various different UWB LO concepts have already been proposed /3–5/, but none of them seems to give a clear advantage over the other. The required ability of hopping from one LO frequency to the other within 9 ns /1/ prevents the use of a conventional approach based on a single wide-band PLL. Single-sideband (SSB) mixers can be used to offset a fixed frequency to simultaneously generate the required carriers which are dynamically selected by a multiplexer /3-4/. This approach, however, in CMOS requires a huge power consumption to achieve low spurious. Another possibility is to use an array of PLLs /5/, leading to a large area. A recent paper /6/ focus on using sub-harmonic injection locking technique, but it seems to achieve the worst hop time.

In this paper, we will describe a fully integrated carrier frequency generator to generate the three mandatory carrier frequencies. The post-layout simulation of the design able to achieve settling time between bands less than 1 ns, which is the fastest reported so far.

2. Concept

The concept of the design is similar to array of PLLs /5/. The carrier frequency generator employs three local oscillators with center frequency of 3432 MHz, 3960 MHz, and 4488 MHz respectively based on the UWB specification. A switching network instead of a multiplexer as in /5/ is used to switch between the center frequencies. Fig. 1(a) shows the architecture of carrier frequency generator with active oscillators topology. A sequence pulse generator that is used to control the switch is assumed ideal and external.

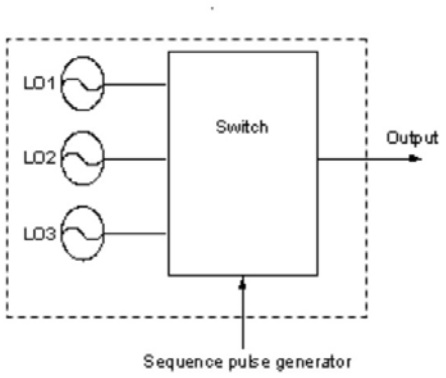

Fig. 1a. Block diagram of active oscillator solution

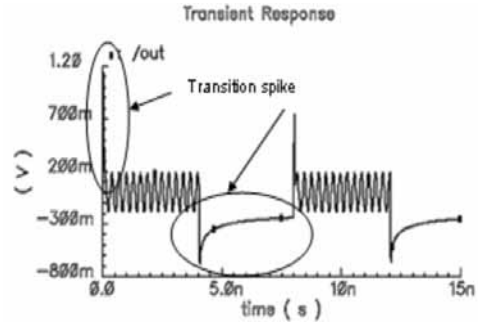

Fig. 1b. Transient response of NMOS switch

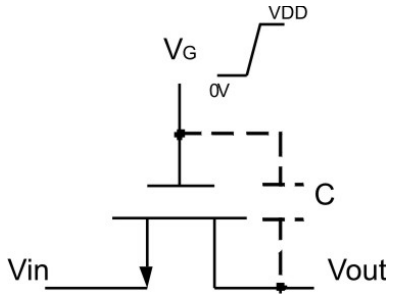

Fig. 1c. NMOS switch with parasitic capacitance

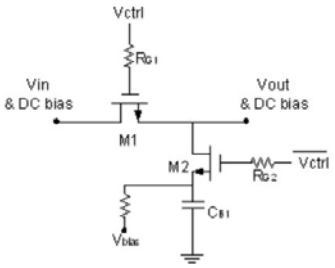

Fig. 1d. Schematic of series-shunt switch.

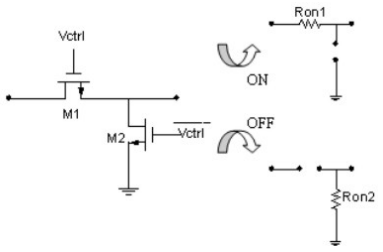

Fig. 1e. Equivalent circuit of series-shunt switch when it is turned on or off.

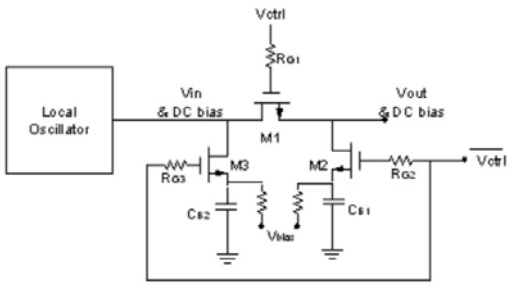

Fig. 1f . Modified series-shunt switch with additional shunt transistor at the input node.

2.1 NMOS Switch

A single NMOS can form a switch by its natural behavior. With the gate voltage acts as the control voltage, the NMOS can provide a path for the signal to pass through from drain to source or vice versa when it operates in linear region; and it blocks the signal when it operates in cutoff region. However a single NMOS switch is not a perfect switch. Fig.1(b) shows transient response of single NMOS switch.

There are two major issues in the NMOS switch that need to be eliminated in order to get a good switch. They are: transient spike at the transition from the switch "off" to switch "on"; and the negative going voltage when the switch is off. A MOS device exhibits inherent parasitic capacitances. These capacitances cannot be avoided. Fig.1(c) shows the NMOS switch with parasitic capacitance between the gate and output node.

We know that C = dQ/dV, where dQ is the magnitude of differential change in charge on one plate as a function of the differential change in voltage dV across the capacitor. The fundamental property of capacitor is it resists any sudden change of voltage across it. Thus when there is a sudden change in V_G, from 0V to VDD, the voltage at the output node is increased for the amount that is sufficient to maintain the charge between the capacitor. Hence a voltage spike equal to the difference occurs at the output node.

When the switch is on, there is a channel conducting under the NMOS gate and between the source and drain to allow the input signal passes to output node. Certainly there are some charges present in the channel. The charge in the channel is on the order of $C_{OX}(V_{GS}-V_{TH})$. When the switch is turned off, these charges either flow to the input source or the output node. The total charges flow to the input source or output node is a function of several parameters, which include input impedance, source impedance, control voltage falling edge and etc. To the first order, 50% distribution between the input source and output node can be assumed. This charge injection phenomenon makes the switch is not totally off in off state.

2.2 Series Shunt Topology

Series-shunt topology is proposed mainly to solve the charge injection phenomenon. In addition to charge injection, since the switch designed is operating at high frequency, the parasitic drain-source capacitance C_{DS} provides a path for signals to pass through from drain to source. This is unwanted because it will degrade the off-state of the switch /7/. Fig. 1(d) shows the schematic of a series-shunt switch.

Transistor M1 performs the main switching function, while the shunt transistor M2 is used to improve the isolation of the switch /8/. When the main switch transistor is on and the shunt transistor is off, the switch performs as a usual NMOS switch. When the main switch is off, the shunt transistor is on to ground the leakage signal due to the parasitic drain-source capacitance. The shunt transistor

also provides a path for the output to ground and the extra charge to be shorted to ground, and hence reduce the charge injection problem. The width of the shunt transistor is half of the main switch. This ratio can be intuitively selected based on the assumption that 50% of charges stored in the M1 channel are distributed to the output node when M1 turns off.

C_{B1} is the bypass capacitor, which allows DC biasing of the output node of the switch. By applying the same DC voltage on the top plate of the bypass capacitor as the output node, DC power consumption is made negligible. R_{G1} and R_{G2} are gate bias resistances used to improve DC bias isolation. The typical value of the gate bias resistance is about 5kΩ /9/. Without the gate bias resistances, the fluctuations of V_{GD} and V_{GS} of the transistors will be higher. These fluctuations will affect the channel resistance and also result in excessive voltage across the gate dielectric and cause breakdown /8/.

The top plate of bypass capacitor, the output node, as well as the input node are biased at the same DC voltage to reverse bias the drain/source-to-substrate p-n junctions. This is purposely to reduce the junction capacitances and RF signal coupled to the substrate and thus decrease the insertion loss /8/.

2.3 Integration of Switch and Oscillators

The switch directly connected to the oscillator definitely brings the effect of loading to the oscillator. As known, a transistor is approximate to a resistor with the value of on-resistance when it is operating in triode region. When the transistor is cut-off, its resistance is very high and approximate to open-circuit. So when the series-shunt switch directly connected to the oscillator circuit, the loading effect is mainly comes from the main switch, M1 and the effect are different when the switch is on and off.

Now we consider the condition when the switch is turned on and turned off as shown in Fig. 1(e). It is clear that when the switch is on, the load connected to oscillator is the on-resistance of transistor M1. When the switch is off, M1 acts as open-circuit and we can assume that no load is connected to oscillator. So it is expected that the amplitude of the oscillating signal will be different when the switch is on and off. When the signal amplitude becomes not stable, we can also expect the occurrence transition noise.

Thus a modification is done on the switch by adding another shunt transistor at the input node as shown in Fig. 1(f). This brings a more symmetrical solution of switch and when the switch is off, transistor M3 is turned on and acts as R_{ON3}. If we choose the width of M3 to be same as M1, the R_{ON3} is equal to R_{ON1}. As a result, no matter the switch is on or off, there is a same load connected to the oscillator. Hence the amplitude of the oscillating signal would be stable regardless the switch is on or off. Finally three oscillators and three switches are integrated to form a complete carrier frequency generator. By properly controlling the pulse generator, we can switch between the three oscillators within 4ns.

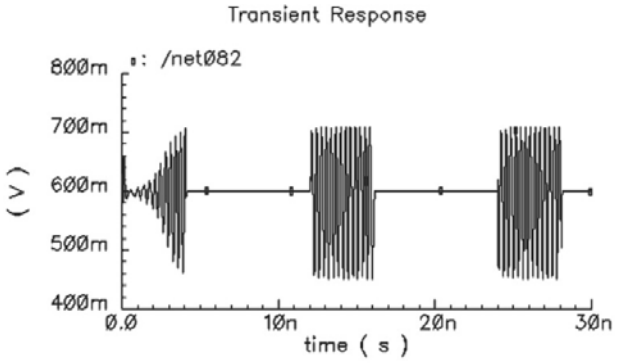

Fig. 2a. Smooth transition of signal generated with modified differential series-shunt switch

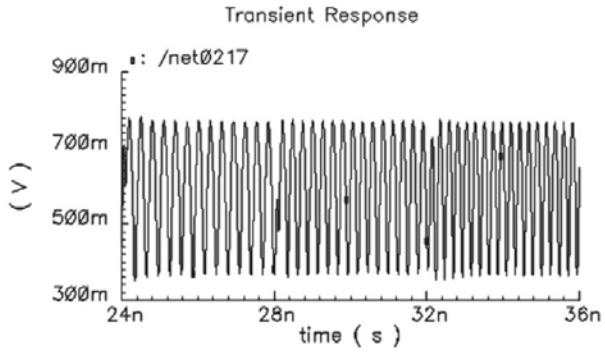

Fig. 2b. Transient response of signal generated from UWB carrier frequency generator

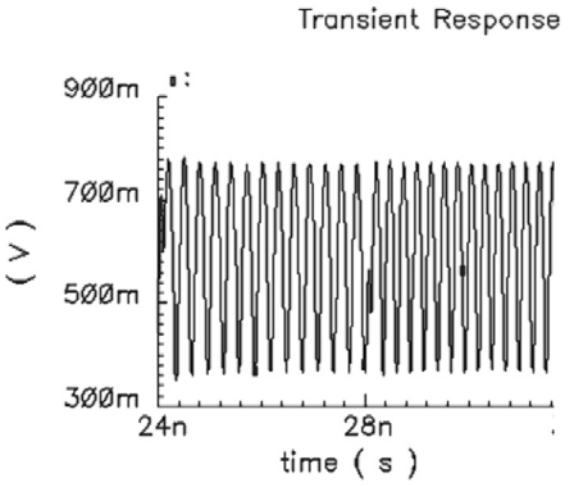

Fig. 2c. Hop time between 3.43 GHz to 3.96 GHz.

3. Simulation Results

Fig. 2(a) shows the signal generated from the local oscillator with center frequency of 3.43GHz integrated with the modified shunt-series switch. The switch is able to

eliminate the spike charge injection problem. In addition, the modified switch had improved the switch performance during transition period

Fig. 2(b) shows the signal generated from the full carrier frequency generator. It can be clearly seen that the signal generated is sinusoidal waveform without clipping and the frequency is different for every 4ns. The amplitude of the signal swing is stable and the transition is considered smooth.

Fig. 2(c) shows the hop time between 3.43 GHz to 3.96 GHz, the settling time is clearly less than 1ns.

Table I shows comparison of this work with other UWB LO Generation system.

Table I. Summary of the performance and comparison to other UWB LO Generation system

	/5/	/6/	This work
Tech/µm/	0.13	0.09	0.18
Band Group	#1	#6	#1
Area /mm^2/	1.9	0.074	2
P_{DC} /mW/	39	36	10.8
Spur Level /dBc/	<-28	<-19	<-20
Hop time /ns/	<2	<4	< 1

This work: Post-Layout simulation result, P_{DC} = 1.8x6 mA (three oscillators).

4. Conclusion

In this work, the design of carrier frequency generator, targeting fast switching between three different center frequencies that are suitable for UWB wireless application is presented. The design is done by using Silterra 0.18µm CMOS technology and the simulation is done by Cadence. A switch is developed that is able to pass the signal from oscillators to output without transition spike. The switch was designed such that it would not give unbalance-loading effect to the oscillator circuit when it is turned on or turned off. The optimization of transistor size was the key point to determine the switch performance. The weakness of a single NMOS switch is investigated then a topology developed that is capable to pass the signal with good transient response. The designed carrier frequency generator is capable to produce a signal with three center frequencies, i.e. 3432 MHz, 3960 MHz, and 4488 MHz at 400mV peak-to-peak swing. The frequency is switched in every 4ns with negligible transition noise. Hop time between frequencies is achieved within less than 1ns.

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