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Crystal Controlled CMOS Oscillator for 13.56 MHz RFID Reader

S. M. A. Motakabber, M. I. Ibrahimy

Department of Electrical and Computer Engineering, Faculty of Engineering, International Islamic University Malaysia, Malaysia

Abstract: A design procedure of CMOS integrated crystal oscillator for 13.56 MHz RFID is described in detail by using mathematical and Mentor Graphics VLSI design tools ADK-3. The system is designed by using CMOS 0.18 µm foundry rules and Level-3 transistor model. The frequency stability of the oscillator is created by using piezoelectric crystal. The designed CMOS crystal oscillator can be integrated with the other parts of the RFID reader systems during VLSI design. The computer-generated phase noise is showed -139.5 dBc/Hz at offset of 10 kHz and the power dissipation is 1.25 mW at power supply 2.2V.

Key words: Crystal oscillator, CMOS oscillator, 13.56 MHz RF oscillator, piezoelectric ISO14443

S kristalom krmiljen CMOS oscillator za 13.56 MHz RFID bralnik

Povzetek: V članku je opisan postopek načrtovanja CMOS oscilatorja z integriranim kristalom za 13.56 MHz RFID s pomočjo matematičnega in Mentor Graphics VLSI načrtovalskega orodja ADK-3. Sistem uporablja 0.18 µm CMOS tehnologijo in model tranzistorjev Level-3. Piezoelektričen kristal skrbi za stabilizacijo oscilatorja. CMOS kristalni oscilator se lahko vgradi v ostale dele RFID sistema med načrtovanjem VLSI. Računalniško generiran šum j eprikazan pri -139.5 dBc/Hz pri odmiku 10 kHz in moči 1.25 mW ob napajanju 2.2 V.

Ključne besede: kristalni oscilator, CMOS oscilator, 13.56 MHz RF oscilator, piezoelektričnost ISO14443

* *Corresponding Author's e-mail: amotakabber@iium.edu.my*

1 Introduction

Radio Frequency Identification (RFID) is used to identify a tagged object by using radio frequency wave. Due to huge potential and robustness nature, the RFID systems have various types of applications such as products chain management systems, access control electronic tickets, fare collection, product labeling, proximity card etc. In fact the heart of the system is a well stable RF source or oscillator. Almost all modern radio communication system is used at least one highly stable radio-frequency source or oscillator for ensuring the reliable communication. A crystal oscillator has the property of generating extremely stable frequency.

An electronic oscillator circuit produces repetitive electric signal from a dc source. The circuit and operation principles of two main types of electronic oscillator (harmonic oscillator and relaxation oscillator) are completely different. The basic structure of a harmonic oscillator is an electronic amplifier of which output is attached with an electronic filter network. The output of the filter network is feedback again into the input of the amplifier. In the beginning when the power supply of the circuit is switched on, the amplifier's output contains only noise. The noise travels through the filtering network is being filtered out. The output (or a portion of the output) is then re-amplified, filtered and feedback repeatedly until it gradually resembles the sinusoidal output. A piezoelectric crystal may take place of the filter network to stabilize the frequency of oscillation, resulting as a crystal oscillator. There are many techniques to implement the harmonic oscillators [1], because there are different ways to design an amplifier and filter network. On the other hand relaxation oscillator produces non-sinusoidal output wave such as a square or saw-tooth waves. This oscillator contains a nonlinear active component like as transistor is used for periodically charging and discharging the energy in a capacitor or inductor. The change of energy in the de-

vice causes abrupt variations on the output waveform and generates non-sinusoidal wave. Like as harmonic oscillator crystal oscillators are often preferred for generating a stable oscillation.

The integrated circuit is more reliable and stable to implement as an amplifier than discrete components amplifier circuit. Therefore, the CMOS circuits are best suitable for design of the active part of the oscillators with a quartz crystal unit. The current mode operations of analog circuits are more suitable for implementing in the CMOS integrated technology. They have a greater gain-bandwidth product than circuits operating in the voltage mode with the same transistors characteristics [2]. Thus current mode operations of analog circuits are suitable for high frequency analysis. The current conveyor is the basic building block for current mode operation. It can be used for realization of negative impedance converters (NICs) with current or voltage controlled negative input resistance. Such NIC circuits have a great gain-bandwidth product and static characteristics whose parameter can be easily modified to the optimal form for oscillator under design.

2 Electrical Model of the Crystal

A piezoelectric (quartz) crystal can be modelled as an equivalent electrical network with low impedance (series) and high impedance (parallel) resonance point spaced closely together as shown in Figure 1.

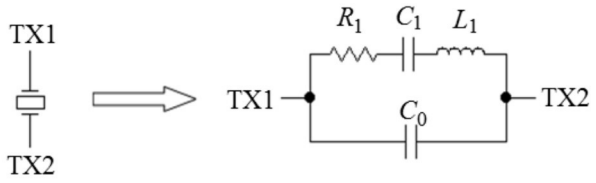


Figure 1: Crystal symbol and its electrical equivalent model

Using Laplace transform, form the equivalent model of the crystal the impedance of this network can be written as:

$$Z(s) = (1/(s.c_{\downarrow}1) + s.L_{\downarrow}1 + R_{\downarrow}1) \| (1/(s.C_{\downarrow}o))$$

Or,
$$Z(s) = \frac{s^2 + s.\frac{R_1}{L_1} + \omega_S^2}{s.C_0\left\{s^2 + s.\frac{R_1}{L_1} + \omega_p^2\right\}} \quad (1)$$

From Equation (1) assume,

$$\omega_s = \frac{1}{\sqrt{L_1.C_1}} \quad (2)$$

and
$$\omega_p = \sqrt{\frac{C_1 + C_0}{L_1.C_1.C_0}} = \omega_s\sqrt{1 + \frac{C_1}{C_0}} \quad (3.a)$$

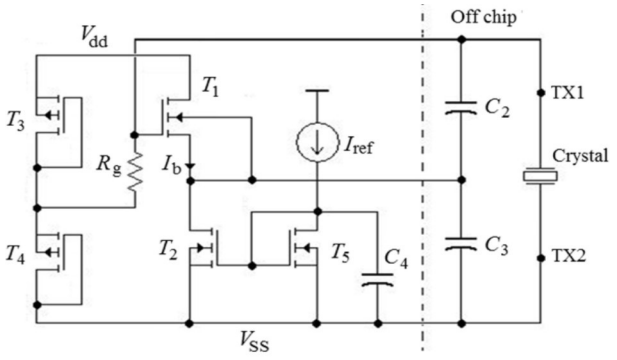
Or, $\omega_p \approx \omega_s\left(1 + \frac{C_1}{2C_0}\right); when(C_0 \rangle\rangle C_1)$ (3.b)

Where, s = jω, is the complex frequency, ω_s and ω_p are the series resonant and parallel resonant angular frequency in radians per second respectively. In this research work the design parameters of the crystal C_0 = 6 pF, L_1 = 6.9 mH, C_1 = 0.02 pF and R_1 = 35 Ω are considered for generating 13.56 MHz frequency.

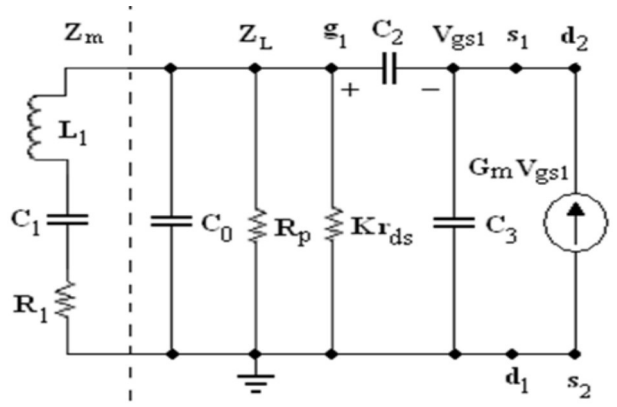
3 Equivalent Circuit of the CMOS Crystal Oscillator

The detailed schematic of the Colpitts crystal oscillator [3] and its equivalent circuit are shown in Figures 2(a) and 2(b) respectively. The nMOS transistor T_1 act as a negative resistance device and transistor T_2 as a bias current source I_b respectively. The transistor T_2 also performed as a current mirror for the reference current I_{ref} in the same chip through nMOS transistor T_5. It provides the stable current with respect to change of the power supply and temperature. The 5pF decoupling capacitor C_4 is added to prevent the high frequency noise leakage from the oscillator. The grid bias resistor R_g combined with the two pMOS transistors T_3 and T_4 is provided the bias for the nMOS transistors T_1 and T_2. The biasing is designated in such a way so that the transistors can always operate in the saturation region during the oscillation. The pMOS transistors T_3 and T_4 are set to be W/L as 0.6/4.0 for giving a bias voltage at the node 1 as $\frac{V_{dd}}{2}$. The external capacitors C_2 and C_3 along with the piezoelectric crystal are worked as a reactive feedback network for three-point Colpitts oscillator circuit.

The capacitor C_2 and C_3 are selected as 10pF and 60pF respectively in this project. The MOSFET's parameters are used in this design as shown in Table 1. In Figure 2(b) the equivalent circuit parameter, $K = \left(1 + C_3/C_2\right)^2$, the effective drain resistance of T_1 and T_2 as, $r_{as} = (r_{ds1} \| r_{ds2})$, and finally $R_p = R_c + (r_{ds3} \| r_{ds4})$ are used. The drain resistance of T_5 is considered as zero value since during the oscillation the capacitor C_4 becomes short circuit.



(a)



(b)

Figure 2: (a) Schematic of a Colpitts crystal oscillator and (b) its equivalent circuit

4. Critical Transconductance g_m

The critical transconductance g_m of the transistor T_1 is the minimum value which is essential for sustaining the oscillation of the circuit. Figure 2(b) is the simplified small signal equivalent circuit of the crystal oscillator where the passive motional impedance Z_m is considered as the series $R_1L_1C_1$ tank (resonant) circuit. The remaining part of the circuit which includes the passive as well as active components is considered as the load impedance Z_L. On the basis of negative-resistance model of the oscillator, the oscillation may occur [4][5] only if,

$$R_1 + R_e\{Z_L(j\omega_0)\} \leq 0 \tag{4}$$

Here, $R_e\{Z_L(j\omega_0)\}$ is the real component of the impedance Z_L at angular frequency ω_0 of oscillator.

If it is considered that, $R_1 = R_e\{Z_L(j\omega_0)\}$ and $\omega_0 = 2\pi\ x13.56x10^6$ rad/s, the critical transconductance of the transistor T_1 is calculated as $g_m \approx 1.4$ mA/V. Using a safety factor of about 4, the transistor T_1 must have a critical $g_m \approx 5.6$ mA/V. From MOSFET theory, the relation of g_m with transistor's physical dimensions and process parameters are as follows

$$g_m = \sqrt{2\mu_n C_{0x}\left(\frac{W}{L}\right)I_d} \tag{5}$$

The parameters, μ_n and C_{0x} are defined by the process considered, W and L are the physical dimension of width and length of the transistor respectively. The parameter I_d is the bias current of the transistor T_1, in this design it was considered as 150 µA. The bias current I_d can be calculated from the reference current I_{ref}, in this design I_{ref} has been considered as 300 µA. The aspect ratio $\frac{W}{L}$ and the other parameters of the respective transistors are shown in Table 1.

Table 1: Physical dimensions and parameters of the MOSFETs are used in the design. (Technology used 0.18 µm and process used for transistor model Level-3)

FET No.	FET type	W (µm)	L (µm)	Aspect ratio $\frac{W}{L}$	gm (mA/V)	rds (MΩ)
T1	nMOS	13.0	0.2	65.0	5.600	0.01
T2	nMOS	1.0	0.2	5.00	0.450	0.1
T3	pMOS	0.6	4.0	0.15	0.008	50.0
T4	pMOS	0.6	4.0	0.15	0.008	50.0
T5	nMOS	2.0	0.2	10.0	0.850	0.04

5 Estimation of the Oscillation Frequency by the Feedback Model

According to the feedback theory, a circuit would be oscillating only, if the small signal close-loop gain of the circuit is greater than unity and the phase shift of the feedback loop is equal to zero (positive feedback). The closed-loop gain can be represented as Equation (6).

$$T(s) = A(s)F(s) \tag{6}$$

Here, A(s) is the gain without feedback and F(s) is the feedback factor. From Figure 2(b), the value of the generated frequency can be calculated by Equation (7)

$$\omega_0 = \left\{\frac{1}{(L_1.C_1)} + \left[L_1.\left(\frac{C_0 + C_2.C_3}{C_2 + C_3}\right)\right]^{-1}\right\}^{\frac{1}{2}} \tag{7}$$

When the capacitors and inductors design values are used in Equation (7), the generated frequency of oscillation is, $\omega_0 = 85.184\,x10^6\,\frac{rad}{s}$, or, $f_0 = 13.557\,x10^6\,Hz$.

6 Layout Design

The layout design is done in analog design mode by Mentor Graphics design tool kit ADK-3. The designed oscillator layout with an isolation buffer amplifier is shown in Figure 3.

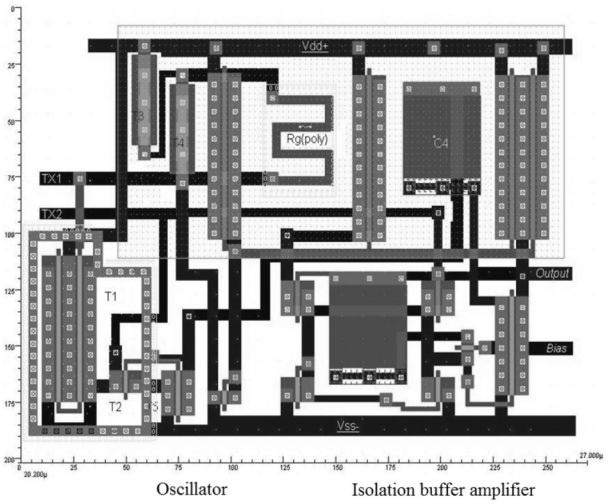


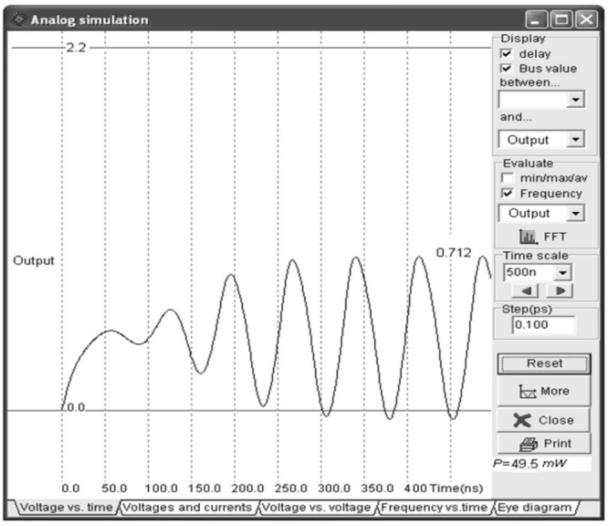
Figure 3: The designed oscillator and an isolation buffer amplifier layout

To prevent the oscillator circuit from the substrate noise all the p-channel transistors are placed inside the n-well and the n-well is connected with the power supply rail V_{dd} In addition the n-channel transistors T_1 and T_2 are surrounded by two guard rings which are connected to the substrate. The unused areas of the chip are filled with extra connection to the substrate and well-regions. To avoid the loading effect of the oscillator an isolation buffer amplifier is also designed on the same silicon chip. The oscillator including an analog buffer amplifier is occupied a die area of 27µm x 20µm. The amplitude of the oscillation is controlled carefully to prohibit the potential of the drain of T_1 and the source of T_2 from exceeding power supplies V_{dd} and V_{ss} respectively to prevent the latch-up effect.

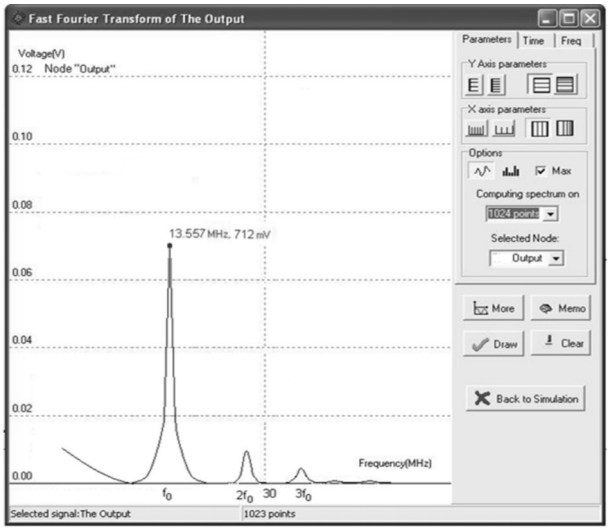
7 Simulated Results

The simulated results are shown in Figure 4. The oscillator layout circuit is simulated which has been designed by using CMOS 0.18 µm foundry rules together with a buffer amplifier as shown in Figure 3. Different VLSI design software are used for simulation purpose and it found the same performance of the circuit.

The maximum amplitude swing of the sinusoidal wave is 712 mV_{PP} at power supply 2.2V, and power consumption is 1 25 mW The phase noise measured by simulation is –139.5 dBc/Hz at 10 kHz offset frequency. The designed oscillator can start up reliably within a wide ranges of supply voltage (0.9~3.6V) and able to operate in a wide ranges of temperature (–10~65°C) to maintain a stable frequency.



(a)



(b)

Figure 4: (a) Build-up of oscillation and time domain signal of the oscillator, (b) frequency domain representation of the output signal

8. Discussion and Conclusion

A step by step procedure of integrated crystal oscillator design has been described. This design can be a guideline for a reliable short time start-up and low phase noise allowing frequency stability ± 7.0 kHz for 13.56 MHz RFID system. In ISO14443 standard this is essential for 13.56 MHz RFID system. Any additional capacitor

across the piezoelectric crystal causes the parallel resonance to shift downward. This technique can be used to adjust the oscillator frequency exactly at 13.56 MHz. The capacitors C_2 and C_3 values are affected the gain of the oscillator circuit and observed that lower the values higher the gain, again the gain is also affected by the ratio $\frac{C_3}{C_2}$, higher the value as the result of higher gain. A buffer circuit is used in this design with the oscillator to derive a load during simulation. This buffer is used to isolate the load from the oscillator circuit which ensures the stable oscillation.

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