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Voltage summing current conveyor (VSCC) for oscillator and summing amplifier applications

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Abstract: In this paper, a voltage summing current conveyor (VSCC) as an active building block for realizing the controlled oscillator and the summing amplifier applications has been presented. The VSCC required low supply voltage as ± 0.5 V consumes low power and has a simple structure. The controlled oscillator has three passive components. The VSCC based oscillator offers using of the grounded capacitors which are suitable for IC implementation, using the less passive components, very good frequency stability and the low voltage operation. In addition, the summing amplifier has been realized using only one VSCC and a grounded passive resistor. The amplifier provides some advantages such as high accuracy and very high input impedance. The performance of the proposed circuit is simulated with SPICE to confirm the presented theory.

Keywords: Current conveyor, oscillator, voltage summing circuit, low-voltage, floating gate MOS

Krmiljen tokovni ojačevalnik za realizacijo oscilatorjev in napetostnih seštevalnikov

Izvleček: V članku je, kot aktivni gradnik, predstavljen krmiljen tokovni ojačevalnik (VSCC) za realizacijo oscilatorjev in napetostnih seštevalnikov. Zahtevana nizka napajalna napetost ± 0.5 V zagotavlja nizko porabo in enostavno zgradbo. Krmiljen oscilator ima tri pasivne elemente. Oscilator na osnov VSCC nudi, ob uporabi ozemljenih kondenzatorjev in manj pasivnih elementov, dobro frekvenčno stabilnost in nizkonapetostno delovanje. Seštevalni ojačevalnik je realiziran le z enim VSCC in ozemljenim pasivnim uporom. Ojačevalnik nudi visoko natančnost in zelo visoko vhodno impedanco. Predlagano vezje je simulirano v SPICE okolju.

Ključne besede: tokovni ojačevalnik, oscilator, napetostni seštevalnik, nizkonapetostno vezje, MOS s plavajočimi vrati

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1 Introduction

In recent years, differential difference current conveyor (DDCC) has been reported [1]. In [2], this circuit has been improved to the differential difference complementary current conveyor (DDCCC) [3]. The differential voltage current conveyor (DVCC) was proposed in [4], which could be realized using a DDCCC (grounding terminal Y_3 of a DDCCC results in a DVCC). Numerous applications employing DVCC and DDCC have been proposed earlier [5-9]. Although there are various circuit topologies using voltage summer [10-13], it has not been shown in any active block using current conveyor implementing only voltage summing. Also, the voltage summing current conveyor can be realized with using DDCC. A current conveyor providing arithmetic operations has already been presented by Kuntman [9]. The linearity range of the circuit has been increased due to the properties of the FGMOS differential pair. However, such a complex circuitry structure has not been required for voltage summing function and also, the circuit has no tunability.

The sinusoidal waveform is an important function in electronics systems. The sinusoidal oscillators are commonly utilized in signal processing circuits, communication, control and measurement systems, etc. Therefore, several sinusoidal oscillators using operational amplifier (Op-Amp) have been introduced in the literature [14, 15]. On the other hand, the op-Amp allows the limited gain-bandwidth product. Thus situated, both the condition of the oscillation (CO) and the oscillation frequency of the oscillators designed using op-Amp are negatively affected. For this reason, these oscillators are not suitable for operating at higher frequencies [16]. Lately, current-mode circuits have been attracted

attention due to having advantages such as wide bandwidth, simple circuit structure, wider dynamic range and low power dissipation [17]. In this context, there are many controllable oscillators with two or more active elements or employing only one active element such as current conveyor (CC), transconductance amplifier (OTA), current differencing transconductance amplifier (CDTA) and differential voltage current conveyor transconductance amplifier (DVCCTA) in the literature [18-22]. It can be seen that the above mentioned performance parameters of the current-mode circuits, especially total power dissipation, have been gone the worse when the more active elements have been used in the designing circuit. Although one active element has been used in design, the circuit structure using as an active element can be included a lot of components. Thus, both using less components and designing at low-voltage have been aimed recently [5, 23].

The summing amplifiers and the difference amplifiers using generally Op-Amp and the current conveyor have been presented in the previous studies [12, 24]. The circuit proposed in 2003 uses only three CCCIIs to realize the functions which are current variable by the bias currents of the conveyors [11]. It is shown that the dynamic range and the linearity of the circuit are not sufficient. Also, it has utilized a high supply voltage as ± 2.5 V. The designed circuits using Op-Amp usually suffers from having lots of passive components and restricted frequency performance of the circuit [16].

In this study, a voltage summing current conveyor (VSCC) for realizing the controlled oscillator and the summing amplifier applications has been presented. Therefore, the purpose of this paper is to introduce a proposed VSCC as a new approach and to show the usability of its applications as a controlled oscillator and a summing amplifier. The VSCC has a simple structure and a good frequency performance. Besides, this circuit required low supply voltage as ± 0.5 V consumes low power. The controlled oscillator has three passive components (one grounded resistor and two grounded capacitors). This oscillator offers using of grounded capacitors which are adorable for IC implementation in a long side eliminating parasitic capacitances, using the less passive components, very good frequency stability and the low voltage operation. Additionally, the summing amplifier has been implemented using merely one VSCC and a grounded passive resistor. The amplifier exhibits high accuracy and very high input impedance. Finally, the functionality of the proposed circuit has been confirmed by the SPICE simulations.

2 Proposed Voltage Summing Current Conveyor

The VSCC is designed by employing floating gate MOS transistors (FGMOS). The symbol and the equivalent circuit of an n-type FGMOS transistor with three inputs are shown in Fig. 1. There are several models to simulate the FGMOS transistors in [25]. The model of the FGMOS used in proposed circuit is based on connecting capacitors in parallel with the resistors as given in [26].

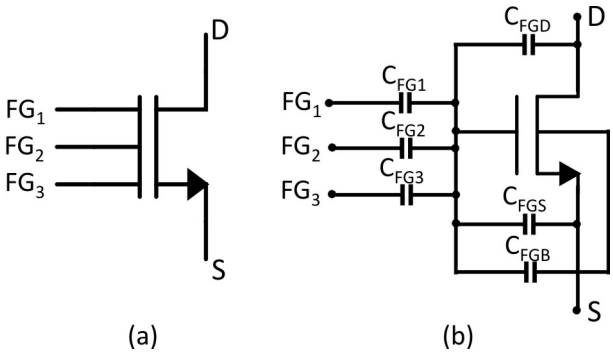

Figure 1: The n-type FGMOS transistor with three inputs a) symbol, b) equivalent circuit

FG_1, FG_2 and FG_3 are the input gate terminals of the FGMOS transistor as displayed in Fig. 1. The input capacitances are C_{FG1}, C_{FG2} and C_{FG3} and the input gates are coupled to floating gate of the FGMOS. C_{FGD}, C_{FGS} and C_{FGB} are the parasitic capacitances between the drain, source, bulk and gate, respectively. Input gate voltages and drain, source and bulk voltages affect an effective floating gate voltage in proportion to value of the coupling capacitances. C_T, sum of all the capacitances between the floating gate and the other terminals can be written as

$$C_T = C_{FGD} + C_{FGS} + C_{FGB} + C_{FG1} + C_{FG2} + C_{FG3} \quad (1)$$

Assumed that the relation shown in Eq.1 is $C_{FGD} + C_{FGS} + C_{FGB} << C_{FG1} + C_{FG2} + C_{FG3}$, then the total capacitance is approximately equal to $C_{FG1} + C_{FG2} + C_{FG3}$. Here, V_{FG} is the effective floating gate voltage and it can be defined as

$$V_{FG} = \frac{C_{FG1}V_{FG1} + C_{FG2}V_{FG2} + C_{FG3}V_{FG3}}{C_T} \quad (2)$$

The drain current I_{DS} of the FGMOS transistor in saturation region is expressed as

$$I_{DS} = \frac{k_n}{2}\left[V_{FG} - V_S - V_{TH}\right]^2 \quad (3)$$

where V_{FG} is the effective floating gate voltage, V_S is the source voltage, I_{DS} is the drain current and V_{TH} is the threshold voltage of the FGMOS transistor. In addition,

kn known as transconductance parameter is $\mu_n .C_{ox}$. (W/L) where μ_n is the electron mobility, C_{ox} is the gate-oxide capacitance per unit area, W/L is the aspect ratio of the FGMOS transistor.

The block diagram of the voltage summing current conveyor as a new approach is demonstrated in Fig. 2.

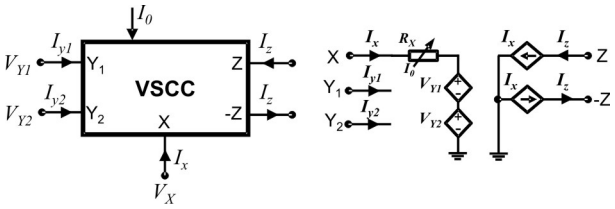

Figure 2: The block diagram and the equivalent circuit of the VSCC.

For the VSCC, Y terminals have high input impedances. The input impedance of the port X is a parasitic resistance and the resistance value can be easily adjusted by bias current I_0 of the VSCC. The Z terminals have high output impedances. The matrix equations of the VSCC are defined as follow:

$$\begin{bmatrix} V_X \\ I_{y1} \\ I_{y2} \\ I_z \end{bmatrix} = \begin{bmatrix} R_X & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \pm 1 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} I_x \\ V_{Y1} \\ V_{Y2} \\ V_Z \end{bmatrix} \tag{4}$$

The circuit structure of the active block as introduced the FGMOS transistor based VSCC is shown in Fig. 3.

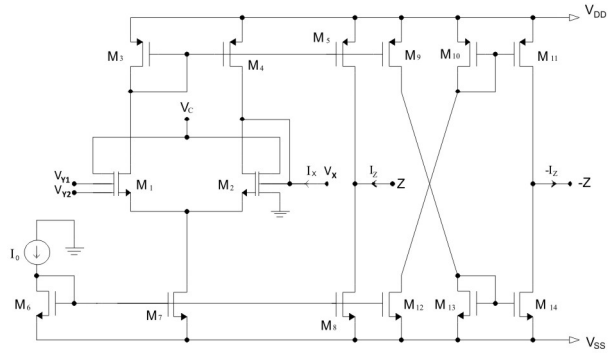

Figure 3: The circuit structure of the VSCC.

In Fig. 3, V_{FGS1} and V_{FGS2} are the floating gate-source voltages terminal for M_1 and M_2 transistors, respectively. The effective floating gate voltages of M_1 and M_2 transistors are V_{FG1} and V_{FG2}. A loop equation written from floating gate of M_2 to floating gate of M_1 transistor can be expressed as

$$V_{FG2} - V_{FGS2} + V_{FGS1} - V_{FG1} = 0 \tag{5}$$

If it is assumed that $C_{FG1} = C_{FG2} = C_{FG3} = C_{FG}$, C_T can be obtained as $3C_{FG}$ shown in Eq. 6. The gate-source voltages in (5) are given as

$$V_{FG1} = \frac{1}{3}\left(V_{Y1} + V_{Y2} + V_C\right)$$
$$V_{FG2} = \frac{1}{3}\left(V_X + V_C\right) \tag{6}$$

where V_C is used for operating the FGMOS transistors at lower voltages. If Eq. 5 is arranged, it can be written as below.

$$V_{FGS2} - V_{FGS1} = \frac{1}{3}\left(V_X - V_{Y1} - V_{Y2}\right) \tag{7}$$

The drain currents of transistors M_1 and M_2 can be written as,

$$I_{D1} = \frac{1}{2}k_n\left(\frac{W}{L}\right)\left(\frac{1}{3}\left(V_{Y1} + V_{Y2} + V_C\right) - V_{TH}\right)^2 \tag{8.a}$$

$$I_{D2} = \frac{1}{2}k_n\left(\frac{W}{L}\right)\left(\frac{1}{3}\left(V_X + V_C\right) - V_{TH}\right)^2 \tag{8.b}$$

I_{D1} and I_{D2} are the drain currents of transistors M_1 and M_2, respectively. $V_X - (V_{Y1}+V_{Y2}) = V_{XY}$. The relationship between input voltages can be calculated as

$$V_{XY} = 3 \cdot \left[\sqrt{\frac{I_0 + I_X}{k_n\left(W/L\right)}} - \sqrt{\frac{I_0 - I_X}{k_n\left(W/L\right)}}\right] \tag{9}$$

where I_0 is the biasing current of the differential pair. From equation (9), current I_X shown in figure 3 can be written as

$$I_X = \frac{1}{3}V_{XY}\sqrt{k_n(W/L)}\sqrt{2I_0 - \frac{1}{2}k_n(W/L)(V_{XY})^2} \tag{10}$$

In equation (10), it is assumed that $2I_0 >> k_n(W/L)(V_{YX})/2$ for a small input voltage. Using this approximation, the output current I_X of the differential pair is obtained as

$$I_X \cong \frac{1}{3}V_{XY}\sqrt{\frac{1}{2}k_n(W/L)}\sqrt{2I_0} \tag{11}$$

From Equation (11), parasitic resistance of the circuit will be expressed as

$$R_x \cong \frac{V_{XY}}{I_X} = \frac{3}{\sqrt{I_0 k_n\left(W/L\right)}} \tag{12}$$

The parasitic resistance is easily controlled by biasing current. It is clear that the electronic tunability of the resistance is presented by this circuit.

3 Simulation results

The proposed VSCC was simulated by SPICE to confirm the theoretical approaches. The SPICE model 0.13 μm TSMC CMOS technology parameter is used for the NMOS and the PMOS transistors. The aspect ratios of the MOS transistors, occurred in the VSCC implementation, are illustrated in Table I. The supply voltage is ±0.5 V. The value of the capacitances shown in Fig. 1 (b) as C_{FG1}, C_{FG2} and C_{FG3} can be taken as 0.07 pF.

Table 1: The aspect ratio of the MOS transistors.

Transistor	W (μm)	L(μm)
M_1, M_2	0.78	0.26
M_3,M_4,M_6,M_7,M_8,M_{10},M_{11},M_{12}	2.6	0.26
M_5,M_9,M_{13},M_{14}	6.24	0.26

Figure 4 displays the changing of the input voltage V_{Y1} versus voltage V_X for the proposed VSCC.

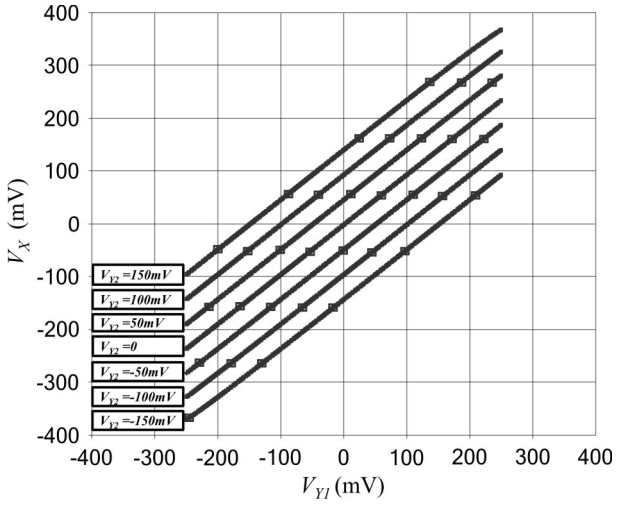

Figure 4: The voltage transfer curve for the VSCC.

The graph has been obtained for the different values of the voltage V_{Y2} as shown in Fig. 4. The curve which has highly linear characterization shows that the voltage transfer gain of the VSCC ($V_X/(V_{Y1}+V_{Y2})$) is equal to 0.99. This value is more satisfactory according to the some designs presented in early studies [27-29]. The changing of the input current I_x versus current I_z for the VSCC is depicted in Fig. 5.

The current gain between terminal X and terminal Z is 0.98. The current transfer curve of the VSCC has almost unity current gain (I_z / I_x). Also, the transfer of current is linear from X to Z node. Figure 6 displays the frequency response for the voltage transfer gain (V_X / V_{Y1}).

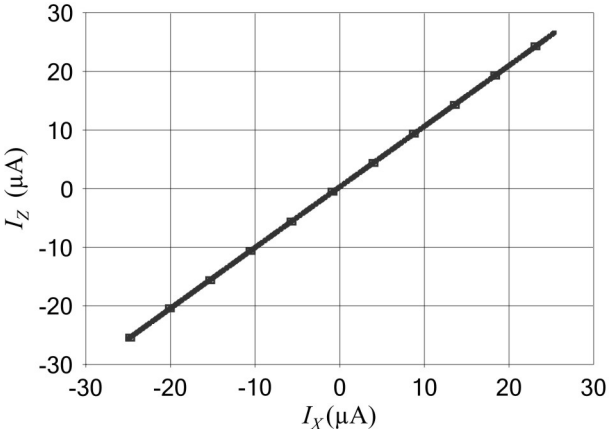

Figure 5: The current transfer curve for the VSCC.

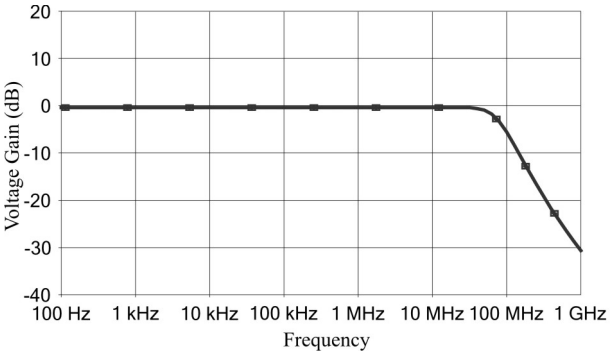

Figure 6: The frequency response of the voltage transfer gain for the proposed circuit.

The frequency response of the VSCC is shown in figure 6 giving bandwidth of 80.1 MHz. The frequency response of the current transfer gain for the VSCC is shown in figure 7. This figure is valid for the all Y terminals having same inputs capacitance values.

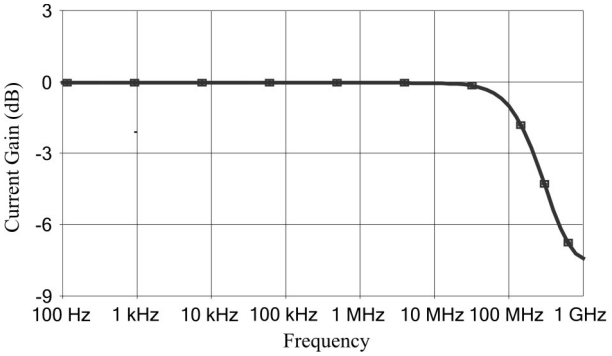

Figure 7: The frequency response of the current transfer gain for the proposed circuit.

The cut-off frequency (-3 dB) is about 211.6 MHz as shown in figure 7. The performance parameters of the VSCC is shown in Table II.

Table 2: The parametric characteristics of the VSCC.

Parameters	Values
Supply voltage	±0.5V
Input voltage range	±300 mV
Output current range	±35µA
Voltage transfer gain ($V_X/(V_{Y1}+V_{Y2})$)	0.99
Current transfer gain (I_Z/I_X)	0.98
3 dB bandwidth I_Z/I_X	211.6 MHz
3 dB bandwidth V_X/V_{Y1}, V_X/V_{Y2}	80.1 MHz
R_X adjustable range (I_0 = 1 µA – 35 µA)	14kΩ-2.1MΩ
Y_1 and Y_2 input resistance	10 GΩ
Z Output resistance	40 MΩ
Power dissipation (I_0 = 25 µA)	61 µW

The parameters of the proposed circuit according to the Table II are reasonable values. The proposed circuit offers some advantages such as described in below.

1. Low-voltage supply requirements about ±500 mV.
2. Low power consumption 61 mW.
3. Acceptable current and voltage gain bandwidth product close to 211.6 MHz and 80.1 MHz, respectively.
4. Electronically tunable intrinsic resistance having wide range.
5. Very high Z-output resistance.
6. Simple circuit design.
7. A new approach which has some advantages.

4 Controlled oscillator based on VSCC

A controlled oscillator based on VSCC shown on Figure 8 is introduced to demonstrate the usability of the proposed VSCC.

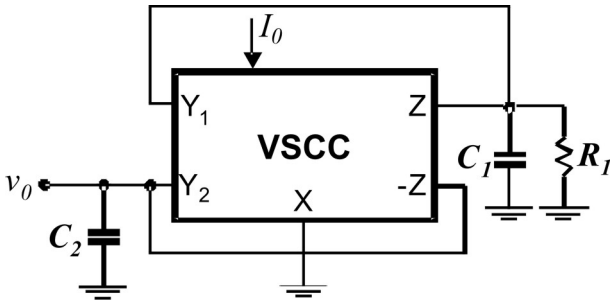

Figure 8: A controlled oscillator based on VSCC.

The circuit consists of single VSCC, one passive resistor and two grounded capacitors. The characteristic equation of the proposed circuit is formulated as below

$$s^2 + s\left(\frac{R_X C_2 + R_1 C_1 - R_1 C_2}{R_X R_1 C_1 C_2}\right) + \frac{1}{R_X R_1 C_1 C_2} = 0 \quad (13)$$

where R_x is the intrinsic resistance of all the current conveyors. From figure 15, input current Iin is equal to current I_2. From equation (11) the oscillation frequency of the oscillator and the condition of oscillation (CO) can be obtained as

$$f_0 = \frac{1}{2\pi\sqrt{R_X R_1 C_1 C_2}} \quad (14)$$

$$CO: \frac{R_1 C_1 + R_X C_2}{R_1 C_2} \leq 1 \quad (15)$$

Taking into consideration both the voltage and the current tracking errors of the current conveyors, $\beta=1-\varepsilon_V$ denotes voltage tracking error from X to the Y terminals; $\alpha=1-\varepsilon_I$ denotes current tracking error from X to the Z terminal where β and α are the voltage and the current transfer gains, respectively and ε_V and ε_I are the voltage and the current transfer errors of the VSCC, respectively. In this situation, the frequency of oscillation can be calculated as

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{\beta\alpha}{R_X R_1 C_1 C_2}} \quad (16)$$

Figure 9 represents the voltage output of the oscillator.

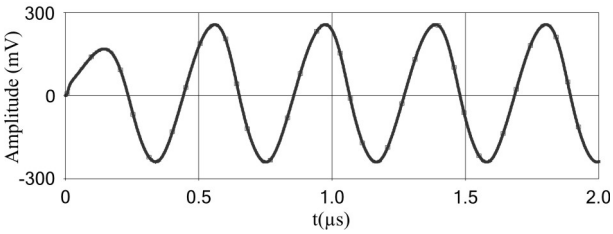

Figure 9: Oscillator output

Controlled oscillator based on VSCC shown in Figure 8 was simulated with the following values for the passive components C_1, C_2 and R_1 are equal to 1 pF, 5 pF and 40 KΩ, respectively, using the value: 25 µA for I_0. Thus, the simulated oscillation frequency value is 2.757 MHz. When this value is theoretically calculated from Eq. 14, the oscillation frequency is obtained as the value of 2.8 MHz. This small difference results from the voltage and the current transfer errors of the VSCC. Figure 10 shows the variation of the oscillation frequency for different biasing currents.

The curves have been obtained both theoretically and simulated using the values: 10, 15, 20, 25, 30 and 35 µA for I_0. The curves shown in Figure 10 exhibit a good coherence with each other. Also, the oscillation frequency between 1.89 MHz and 3.28 MHz is easily controlled by biasing current, and further, total harmonic distortion (THD) of the proposed circuit is less than 2 %.

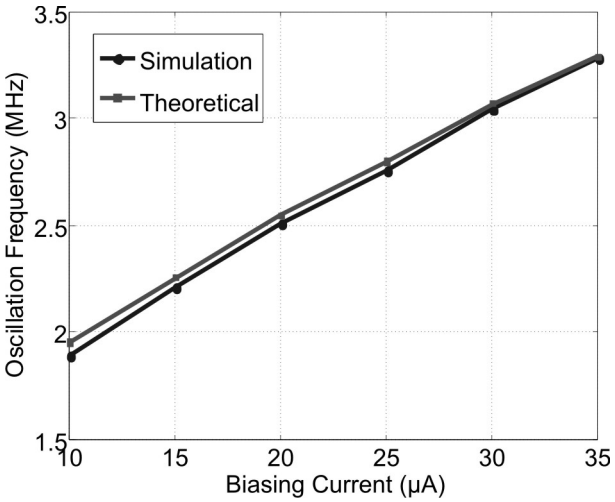

Figure 10: Oscillator frequency versus biasing current.

5 Summing Amplifier

The proposed summing amplifier circuit is shown in Fig. 11. As it is seen from Fig. 2, the circuit whose Port X and Port –Z are connected to each other contains one passive resistor.

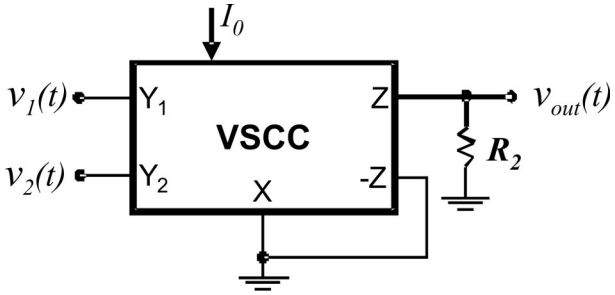

Figure 11: The summing amplifier with two inputs.

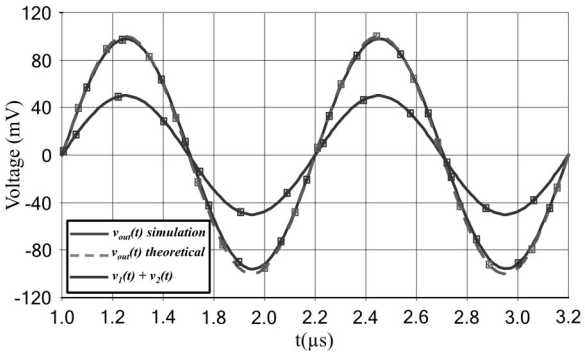

Figure 12: Sinusoidal voltage waveforms for the amplifier.

The transfer function of the summing amplifier shown in Figure 10 is written as,

$$A_V = \frac{v_{out}(t)}{v_1(t)+v_2(t)} = \frac{R_2}{R_x} \quad (17)$$

The simulation of the summing amplifier using VSCC shown in Fig. 10 has been done. Besides, voltage waveforms of the circuit is shown both simulation and theoretical in Fig. 12. The value of the passive resistor is 31 KΩ and the intrinsic resistance R_x is taken as 15.5 KΩ. As shown in Figure 12, voltage $v_1(t)$ and voltage $v_2(t)$ are chosen at 1 MHz 30 mV and 20 mV, respectively.

Sum of the voltages is named $v_{out}(t)$ as shown in Figure 12. On the other hand, the voltage gain of the amplifier can be obtained as 2. The simulation results almost correspond with theoretical results. Maximum error of the gain is about 1 % for $V_{out} = \pm 300$ mV. However, the error of the gain is 0.1 % for -100 mV ≤ V_{out} ≤ +100 mV. Additionally, DC output offset voltage and total power dissipation of the amplifier are 329 μV and 79.8 μW, respectively. The frequency responses of the amplifier for

Table 3: The comparison between this study and the others.

Parameters	This study	[30]	[31]	[32]	[33]
Supply voltage	± 0.5 V	± 1.35 V	± 2.5 V	± 15 V	5 V
Input voltage range	± 250 mV	-2.5 V, + 5.5 V for $V_S^* = +5$ V	NA	± 10 V	NA
Output voltage range	± 300 mV	(+V_S) - 0.35 V (-V_S) + 0.3 V	± 280 mV	± 10 V	NA
DC offset voltage	329 μV	250 μV	25 mV	100 μV	150 mV
Total voltage noise	13.89 nV/√Hz	87 nV/√Hz	NA	60 nV/√Hz	212 nV/√Hz
Power dissipation	79.8 μW	NA	40 mW	NA	1068 mW
Bandwidth	61.3 MHz	800 kHz	NA	1 MHz	20 kHz
Gain Error	1 %	0.1 %	NA	NA	NA
Input impedance	10 GΩ	80 kΩ	NA	1 MΩ	NA
Electronically Tunability	Yes	No	No	No	No

*V_S : Supply voltage

different biasing current are displayed in Figure 13. The biasing current is changed from 20 µA to 30 µA step by step with 5 µA. The cut-off frequencies of the considered amplifier have been obtained as 54.5 MHz, 61.3 MHz and 66.4 MHz for 20 µA, 25 µA and 30 µA, respectively.

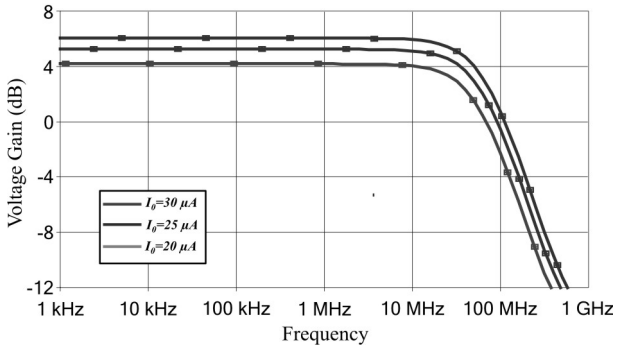

Figure 13: Frequency responses of the amplifier for different biasing current ($V_z/V_{y1}+V_{y2}$).

A noise analysis of the summing amplifier was performed in SPICE. Therefore, with respect to SPICE results, the noise curve belonging to the total output voltage of the amplifier is given in Fig. 14. Total voltage noise of the proposed circuit can be obtained as 13.89 nV/√Hz for I_0=30 µA.

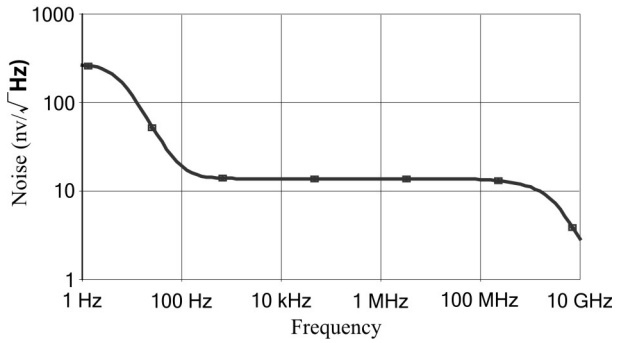

Figure 14: The total output voltage noise versus frequency.

When the literature is investigated, it has been seen that there are a lot of Op-Amp based summing amplifier as an IC structure. Their summing amplifier IC products and proposed amplifier displayed in Table III are compared with each other.

The frequency performance of the presented circuits is restricted as shown in Table III. The circuits have no electronically tunability. Also, these circuits have low input impedance of about KΩs. On the other hand, the proposed amplifier has high input resistance. The obvious advantage is the high input resistance of the proposed circuit reducing the loading on the input signal sources, and therefore affords better signal accuracy and linearity. When the low value input resistors are used, the input leakage currents to the amplifiers significantly are higher than the lowest input signal currents available such that the accuracy of the summing amplifier is not preserved. The multi-input summing amplifier which has four inputs shown in Figure 15 can be given as an example.

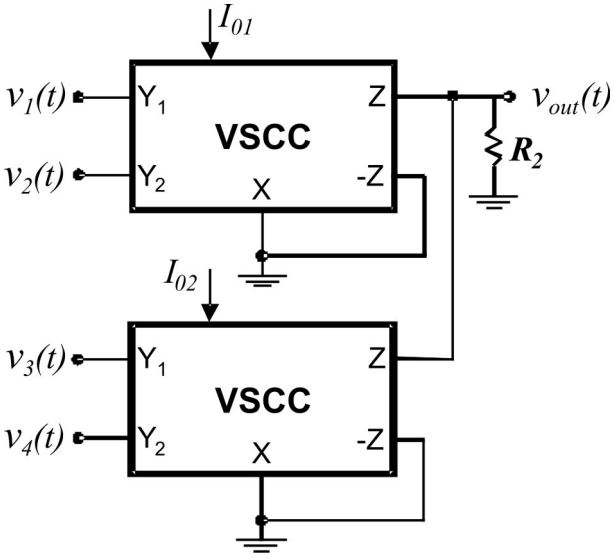

Figure 15: The multi-input summing amplifier.

The voltage output of the circuit can be calculated as below.

$$v_{out}(t) = \frac{R_2}{R_x}\left[v_1(t) + v_2(t) + v_3(t) + v_4(t)\right] \quad (18)$$

The voltage gain of the circuit can be controlled by intrinsic resistance R_x shown in Equation 18. This situation is an important advantage in the electronic circuit design.

6 Conclusion

In this paper, a new approach called voltage summing current conveyor for realizing controlled oscillator and summing amplifier applications has been presented. Simulation results done by SPICE confirm the validity of the theory and demonstrate the use of the VSCC in the controlled oscillator and the summing amplifier applications. FGMOS based the proposed circuit which has highly linear characterization shows that voltage transfer gain and current transfer gain are equal to 0.99 and 0.98, respectively. These values are admirable. Moreover, the frequency responses of the VSCC are acceptable levels. This VSCC is designed in 0.13 µm CMOS process and has ± 0.5 V supply voltage. The linear electronically tunable intrinsic resistance can be tuned for the resistive value from 14 kΩ to 2.1 MΩ. The simulation

results show that this design is powerful sufficient to be utilized in the proposed circuit to achieve low-voltage and low-power. The controlled oscillator used as an application has a stable sinusoidal output. Furthermore, the oscillation frequency value can be controlled by the biasing current. As another application, the summing amplifier having high input resistance and controllable gain has been introduced.

Finally, such an active element is rather proper for low-voltage and low-power IC realizations of which results in decreasing of power consumption. That's why it is clearly shown that the proposed circuit can be used in general electronic circuit design as an active element which has different features such as voltage summing operation.

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