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Development of an Improved Zinc Oxide Thin Film Transistor for Next-Generation Smartphone Display Technologies

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Abstract: This study introduces hypothetical circuit elements, specifically the Constant Phase Element (CPE) and Zeroth-Order Approximation of a RC Circuit (ZARC), into the SPICE circuit simulation environment to enhance Electrochemical Impedance Spectroscopy (EIS) analysis. EIS, a critical method for understanding electrochemical processes in fields such as fuel cell analysis, corrosion studies, and biomaterials, relies on fitting measured impedance curves to Equivalent Electrical Circuit (EEC) models. However, existing approaches require expert knowledge and significant mathematical effort, limiting automation. By integrating CPE and ZARC into SPICE, this work bridges the gap between EIS analysis and advanced automatic circuit design methodologies, enabling efficient model selection and parameter determination. Experimental results demonstrate the accuracy of the implemented elements through a series of case studies, evaluated using Sheppard's criteria function. This integration marks a significant step toward automated EIS model fitting and optimization, with potential implications for advancing electrochemical and materials research.

Keywords: Electrochemical Impedance Spectroscopy, Circuit Simulators, Hypothetical Circuit Elements, Equivalent Electronic Circuits

Razvoj izboljšanega tankoplastnega tranzistorja iz cinkovega oksida za naslednje generacije tehnologij za predvajanje na pametnih telefonih

Izvleček: Študija uvaja hipotetične elemente vezja, zlasti element konstantne faze (CPE) in aproksimacijo RC vezja (ZARC), v simulacijskem okolju SPICE za izboljšanje analize elektrokemične impedančne spektroskopije (EIS). EIS, ki je ključna metoda za razumevanje elektrokemijskih procesov na področjih, kot so analiza gorivnih celic, študije korozije in biomaterialov, temelji na prilagajanju izmerjenih impedančnih krivulj modelom ekvivalentnih električnih vezij (EEC). Vendar obstoječi pristopi zahtevajo strokovno znanje in veliko matematičnega napora, kar omejuje avtomatizacijo. Z vključitvijo CPE in ZARC v SPICE to delo zapolnjuje vrzel med analizo EIS in naprednimi metodologijami samodejnega načrtovanja vezij ter omogoča učinkovito izbiro modela in določanje parametrov. Eksperimentalni rezultati dokazujejo natančnost implementiranih elementov z vrsto študij primerov, ki so ovrednoteni s Sheppardovo kriterijsko funkcijo. Ta integracija pomeni pomemben korak k samodejnemu prilagajanju in optimizaciji modelov EIS, kar lahko vpliva na napredek elektrokemijskih raziskav in raziskav materialov.

Ključne besede: Elektrokemijska impedančna spektroskopija, simulatorji vezij, hipotetični elementi vezij, ekvivalentna elektronska vezja

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1 Introduction

A conventional technology extensively utilized in new-generation flat-panel displays, laptops, desktop computers, smartphones, video gaming systems, and personal digital assistants is thin-film transistor (TFT) technology. Due to this technology, flat screens with ever-larger dimensions are now possible, revolutionizing video systems: The most common substrates being used nowadays for the production of TFT-enabled liquid crystal display (TFT-LCD) have a diagonal dimension of 164 inches. It took a long time for their fabrication technique to

advance to the point where it could be utilized in production, even though it has a history that is almost as old as CMOS technology [1]. There are three sides to the advancement and development of TFT technology: the enhancement of the semiconductor layer, the stability of the manufacturing process for large-scale production, and the advancement of process machinery to create ever-larger devices. The first factor was primarily what initially slowed down the massive development of this technology. TFT-LCDs have used this technology since it first appeared. However, some other applications have been critically reviewed over the past 20 years in diverse areas like X-ray detection [2, 3], microelectronic devices-enabled memory [4, 5], chemical sensing [6], and bio-chemical sensing [7]. The last field has seen a significant contribution from organic thin film transistors (OTFTs) [8].

The display industry makes extensive use of TFTs as specific devices for data available in pixel display. TFTs also hold promise for flexible 3D ICs and large-area integrated circuit applications. A type of flat panel display also known as Active Matrix LCD was made possible by TFT technology, which is majorly considered the main building block behind the display unit of laptop computers. Flat panel displays are increasingly being used in place of cathode ray tube (CRT) screens in desktop computer systems. Recent advancements in the mobility and stability of amorphous silicon, along with the higher manufacturing costs of polysilicon, have heightened interest in oxide semiconductors such as ZnO and indium gallium zinc oxide (IGZO). Although some special designs of ZnO-TFT with field-dependent saturation mobility higher than 100 cm^2/Vs have already been reported [9] and the manufacturing process of such devices greatly used pulsed laser deposition (PLD) technique, which could restrict their use in large-area and low-cost applications. RF Sputtering is a desirable deposition technique for the high-volume manufacturers of oxide semiconductor devices, particularly ZnO, in contrast to PLD.

In this study, we have demonstrated an efficient TFT device structure that utilizes an RF-sputtered zinc oxide (ZnO) film as the active layer. The ZnO TFT, which has a channel width of 60 nm, was fabricated on a single-sided polished p-type <100> crystal-oriented silicon die with dimensions of 2 cm x 2 cm. This device exhibits a high on/off drain current ratio of approximately 2 x 10^8 and a field-dependent saturation mobility of 48 cm^2/Vs.

A bottom gate TFT is developed where ZnO plays the pivotal role of the active channel layer. A thin layer of Silicon dioxide (SiO_2) provides an isolation between the p-type Silicon substrate and the conducting ZnO channel. Source and drain metallic contacts are applied on the top of the conductive ZnO layer. The gate contact terminal of the Transistor lies on the top of the Silicon layer through which the modulation of charge carrier concentration takes place inside the ZnO channel. TFTs are a special class of Field Effect Transistor that consumes current in the microampere range which is a hundred times smaller than a conventional silicon MOSFET. It is also important that the size of the TFT is much smaller than the conventional silicon MOSFET.

2 Literature review

A review of the literature was collected to explore relevant research articles. TFTs are essentially MOSFET transistors, and the first TFT was made in 1962, around two years after the first MOSFET [10]. The first TFT-LCD was demonstrated in 1973, establishing the primary course for TFT technology research and development [11]. The manufacture of TFTs and MOSFETs does not share the same challenges. This distinction explains why TFT-LCDs took more than 20 years to become commercially viable. The process steps are where the fundamental distinction between CMOS and TFT technology exists. While TFT technology just requires deposition, CMOS technology also includes the steps of implantation and layered growth from the substrate. This has significant ramifications for the source, drain, and channel's crystalline quality: the carrier mobility in CMOS is unquestionably better than in sin TFTs because of the crystallinity preservation with the implantation approach, whereas deposition only yields amorphous layers. TFT technology, on the other hand, has a significant advantage over CMOS technology in that since just a deposition procedure is required, transistors may be made on virtually any substrate, including transparent materials like glass and plastic. That is why technology has always been chosen for the creation of LCD screens.

A CdSe TFT was introduced in 1973 [12, 13] after the CdS TFT, which was the first, was introduced. The carrier mobility of both was above 40 cm^2/Vs, which was fairly good mobility. However, the application to LCDs never became commercially viable due to challenges in the fabrication process, such as the stability of the semiconductor quality on a broad surface followed by the reliability issues of the devices.

Due to the invention of hydrogenated amorphous silicon (a-Si:H) at the beginning of the 1980s, which significantly enhanced the stability and properties of TFTs, this technology underwent a significant advancement, enabling the production of active matrix (AM) LCDs, and in 1989 the first TFT-LCD was commercialized. Due to the advancement of other materials, the semiconducting layer was then improved. A significant step in further enhancing the properties of TFTs was the creation of transparent oxide semiconductors, such as IGZO. Due to the high carrier mobility and the creation of transparent transistors, the LCDs' aperture ratio increased while power consumption was further decreased [14]. Some other groups also reported potential TFTs with high K gate dielectrics [15, 16, 25, 28] and in both cases, the performance of the device was found to be remarkably good in terms of its mobility and on/off current ratio.

Another element of technological growth is product dimensions. The diagonal measurement of the first TFT-LCD to be commercialized was 10.4 inches. The 10th generation of mother glass, which corresponds to glass substrates as large as 2850 mm by 3050 mm, is now being used in TFT-LCD manufacturing facilities (164 in.). The 11th generation of mother glass, measuring 3200 mm by 3600 mm (189 in.), is now being developed and ought to be put into use soon. Companies like SHARP, LG, Samsung, and Innolux, among others, have been working hard to develop stable processes on large-scale substrates and to make progressively huge equipment for the deposition, lithography, etching, and testing of even larger substrates. LCD panels are the principal device that uses TFTs. TFTs are nevertheless frequently utilized as sensors in X-ray detectors. In numerous sensing applications, TFT devices are also used.

Resistive pressure sensors are among the most used physical sensors and were created for TFT touch panels. Since the start of the 2010s, businesses like LG Display, AUO, and JDI have started producing them [12]. OLED and pressure sensor layers have been incorporated into the TFT array substrate. In the latter, pressure is converted into an electrical signal that is then

sent to TFTs, which modulate and operate the OLED. A soft polymer containing conductive particles or a pressure-sensitive rubber with resistance that varies with pressure, such as poly (methyl methacrylate) (PMMA), can be used as the pressure sensor [13]. For example, when TFTs are made on a flexible substrate utilizing organic TFTs (OTFT), this application of e-skin technology for physical sensors has attracted a lot of interest from the robotics community [17]. In addition to that the application of TFTs was also found in the field of uncooled infrared sensor arrays for thermal, pollution management, or watching over semiconductor wafers while they're being processed [18, 19].

Recent advancements in electronic device design emphasize power efficiency, scalability, and stability across various applications, including IoT and biomedical devices. For instance, a novel Sense Amplifier-Based Flip-Flop (SAFF) demonstrated robust performance under wide voltage and temperature variations, showcasing significant power and area efficiency for IoT applications [20]. Similarly, a high-performance frequency divider utilizing advanced CMOS technology achieved reduced delay and improved precision, making it suitable for biomedical applications [21]. These studies highlight the importance of innovative methodologies to enhance device efficiency, scalability, and applicability. Building on these principles, this research employs advanced nanofabrication techniques, including RF magnetron sputtering, to develop a ZnO TFT with a high on/off current ratio and superior field-dependent mobility, offering a low power solution for next-generation laptop and smartphone displays.

3 Theory and analysis

The semiconductor industry has experienced tremendous expansion as a result of the dependence of daily life on its products. Achieving progress necessitates the creation of ever more compact devices that are also faster, more adaptable, more efficient, and less expensive. To fulfill the demands of the expanding semiconductor industry, new technologies and materials have been developed in response to this demand. One of the newest and busiest fields of study is nanotechnology, which produces items with very small particles and unique features. Thin-film technology, which enables the deposition of extremely thin layers of semiconductor material on a supporting substrate (from a few nanometers down to the angstrom level), is crucial in this regard. Due to surface and quantum confinement effects, the resultant material has unprecedented mechanical, chemical, optical, and electrical properties after being shrunk to the nanometer scale. ZnO is an attractive material because of its superior electronic and optoelectronic properties. ZnO is excellent for a variety of devices because of its direct and wide band gap (i.e., 3.4 eV) nature along with large exciton binding energy [22]. In the tetrahedral geometry of the crystal lattice, each Zn atom is surrounded by four O atoms, while each O atom is also surrounded by four Zn atoms. Rock salt, zinc blende, and wurtzite are the three crystal forms that ZnO can take. ZnO exists in wurtzite form at ambient temperatures [23]. The growth of ZnO on a cubic substrate can produce a stable zinc blende phase [24, 25, 26]. The lattice parameters for the wurtzite structure are equal, between 3.2475 and 3.5201 angstrom, and between 5.2042 and 5.2075 angstrom. Strong ionic characteristics are seen in the link between Zn and O in the crystal lattice. ZnO is thus categorized as a compound that falls between an ionic and a covalent kind [23].

In this context, a necessary initiative is taken towards the fabrication and characterization of an efficient ZnO-based TFT structure with bottom gate arrangement. Fabrication of a TFT is a complex process and it occupies a lot of steps starting from mask layout design to the development of the end device on a single side polished <100> crystalline silicon wafer.

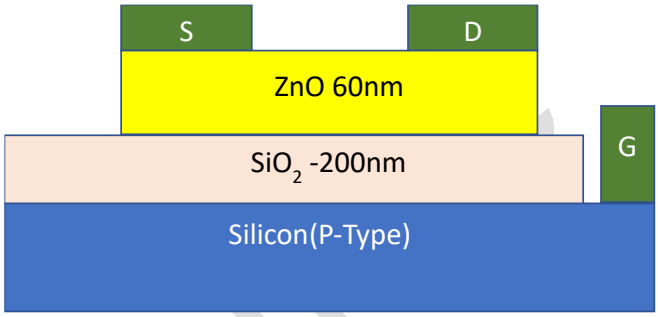

Figure 1. Structure of proposed ZnO TFT

In Figure 1, a two-dimensional design of a TFT is proposed where ZnO is the active layer. The Transistor will be developed on a p-type single crystal <100> silicon substrate. Source, Drain, and Gate metal contacts are made up of aluminium. Figure 2 represents the layout design of the ZnO TFT with a *W/L* ratio of 75/25. The light blue region represents the ZnO layer, and the pink-colored region represents the source and drains metal contacts respectively, and the dark blue region placed at the right side represents the bottom gate metal contact. One might find it confusing to compare Figure 2 with Figure 1. However, the process involved a blanket deposition of SiO_2 on top of the silicon wafer. Following this, a square section was completely etched away from the SiO_2 using UV photolithography, indicated by the shaded dark blue area. Later the bottom gate aluminium contact was deposited in that region.

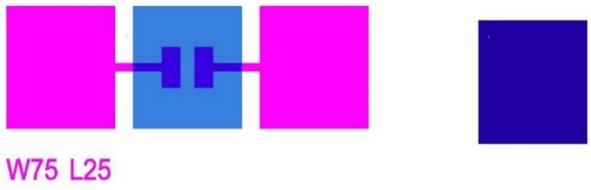

Figure 2. Mask Layout Design of a ZnO TFT in Clewin Software

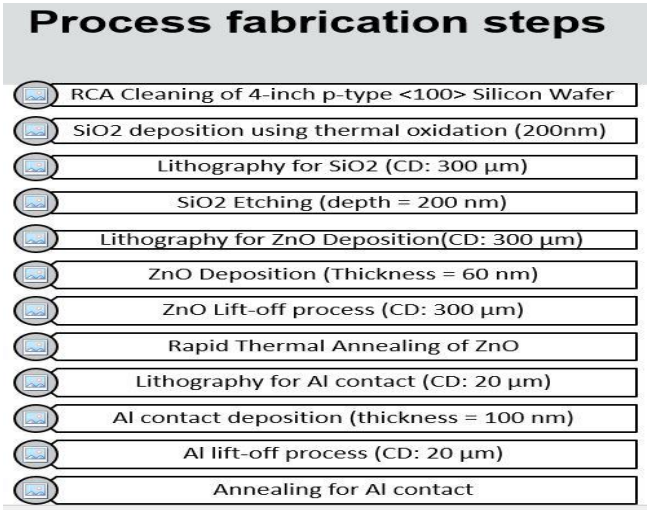

Figure 3. Process fabrication steps

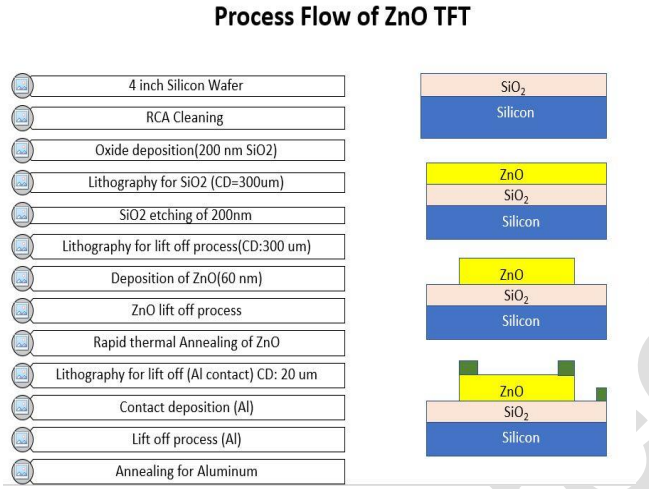

Figure 4. Complete process flow chart of ZnO TFT with tentative step-by-step design

In Figures 3 and 4, a step-by-step process fabrication method is given. Contamination is a big problem in the nanofabrication process so to minimize the effect of contamination a cleaning is a must for a fresh new wafer. It is highly recommended to clean the silicon wafer before doing any process. Therefore, an RCA (Radio Corporation of America) cleaning was performed followed by a dilute HF dip just before the thermal oxidation process.

RCA Cleaning: The RCA cleaning is a three-stage cleaning process and in the first stage the wafer is immersed in a mixture containing Deionized water, NH_4OH, and H_2O_2 in a ratio of 5:1:1. The solution temperature is kept constant at 75 °C during the cleaning process. Similarly, the second stage of RCA cleaning was done at 75 °C with the following quantities present in the mixture (Deionized water and H_2O_2 and HCl) in the ratio of 6:1:1. The total duration of the first and second stages of cleaning is around 20 mins (i.e., 10 mins for each stage). The first stage of RCA is used to remove the inorganic oxides from the wafer surface and the second stage of RCA is used to remove metallic and ionic contaminants from the wafer surface. After the RCA process, one has to clean the wafer using a solution containing a dilute Hydrofluoric Acid (i.e., a mixture of HF and wafer in a ratio of 1:50) for 30 s. Silicon tends to react naturally with atmospheric oxygen and in this process, a thin layer of native oxide develops on the surface of the silicon wafer. A dilute Hydrofluoric Acid (HF) dip completely removes the native oxides from the wafer surface.

Thermal Oxidation: Once after the cleaning process, the wafer should be taken to the thermal oxidation chamber without further delay. Dry oxidation is then performed inside the oxidation chamber at a temperature of 1100 °C where silicon reacts with oxygen and a thin oxide (SiO_2) layer of 200 nm is formed at the surface of the wafer. The process duration was around four hours.

Maskless Lithography: The lithography process used in this study was performed with the Heidelberg µPG 501, a direct laser writing tool that operates at a UV wavelength of 365 nm. This mask-less lithography method enables precise patterning of photoresist-coated substrates by directly writing the desired features without the need for traditional photomasks. This approach offers enhanced flexibility and accuracy, especially for prototype fabrication.

A maskless UV photolithography is then performed for the selective etching of the thermal SiO_2 layer from the top of the wafer. A UV light source of 365nm wavelength was projected on the photoresist coated wafer surface in Figure 2. Laser/LED writing is a photolithography process that uses a laser beam or LED to create the required patterns on the photoresist (direct writing). The Mask Writer's unique feature is its ability to generate patterns directly on any substrate using photolithographic principles, with or without the aid of a traditional mask plate. Mask writers are primarily used to create photolithographic mask reticles and masks up to 5 inches in size for the Heidelberg uPG 501 system. AZ5214 type positive tone photoresist was used during this process. A positive tone photoresist is an organic compound found in the solid form (i.e., a thick substance) and upon UV exposure the exposed area becomes softer. That part can be removed by using the proper developer solvent. 22 s of development of the wafer in a solution containing MF26A (i.e., usually used for the development of positive photoresist-coated silicon wafers) gave the desired output and it was thoroughly confirmed during a microscopic inspection.

Wet Chemical Etching: Just after the photolithography process, the wafer was taken to the Chemical Wet etch bay to execute a SiO_2 chemical etch process to remove the SiO_2 from the selective areas where the photoresist is not present. A buffered oxide etchant solution was used to etch the 200 nm thin SiO_2. A wet etchant called buffered oxide etchant (BOE) is utilized in microfabrication. Its main application is to etch SiO_2 or silicon nitride thin films (Si_3N_4). BOE contains a combination of Hydrofluoric acid (HF) and a buffering agent like ammonium fluoride (NH_4F) whose work is to supply the fluorine ion into the solution and to maintain the uniformity in etch rate. The optimized etch rate of the BOE solution was found to be 71 nm/minute after testing. The Silicon wafer was dipped into the mixture for the desired time duration to etch the thermal oxide completely from the selective area.

Deposition of ZnO: After the completion of the SiO_2 etching process, the substrate was sent for optical lithography since a lithography process must be performed before the deposition of the transparent ZnO layer through RF (Radio Frequency) magnetron sputtering. The lithography process for ZnO is the same as discussed before. The minimum feature size was found to be 300 µm.

One of the methods for depositing thin films that are most frequently employed is sputtering. The substance from which a

film is created or a plate with the materials to be deposited serves as the target. The target often called the cathode, is connected to the negative terminal of a DC (Direct Current) or RF power supply. It typically receives several kilovolts of electricity. The substrate that is exposed to the cathode may be grounded, electrically floating, biased either positively or negatively, heated, chilled, or any combination of these. After the chamber has been emptied, a gas (typically argon) is added and used as the medium to start and sustain a discharge. Typically, gas pressures range from a few to 100 mtorr. It is seen that current flows and a film condense on the substrate after a visible light discharge has been maintained between the electrodes. Of course, there is no current flow and no film deposition in a vacuum. Positive ions from the discharge interact with the cathode plate under a microscope and use momentum transfer to eject neutral target atoms. These atoms enter the discharge region, travel through it, and then eventually deposit on the developing film. In addition, the target emits radiation (X-rays and photons) as well as other particles (secondary electrons, desorbed gases, and negative ions).

The RF magnetron sputtering involves a thermal process where the sample is heated up to 100 °C using a halogen lamp. The ZnO deposition was done by RF magnetron sputtering through rotation mode. The rotation mode was chosen to achieve good uniformity of ZnO deposition throughout the desired area.

ZnO Lift-off Process: After the deposition process, the ZnO-containing wafer was immediately transferred to the wet chemical bay for a lift-off process. It is noted that during photolithography a positive photoresist was coated all over the wafer or sample and only the area exposed to UV rays doesn't contain any photoresist after the development. Inside the RF Magnetron sputtering chamber, the ZnO was deposited all over the wafer and it is expected that ZnO to be present only at the place where it faces a SiO_2. In the lift-off process firstly, the wafer is dipped into an acetone solution, and therefore applying extra acetone to the top of the wafer with a high velocity. During this process, there was a peel-off of the Photoresist which was present underneath ZnO. ZnO was also eliminated from the wafer surface along with the photoresist. Only that part of ZnO will be stacked to the wafer which faces the underneath SiO_2 layer. The process is very complex and it requires continuous microscope inspection but during microscope inspection, the wafer must be transferred into an IPA (Isopropyl Alcohol) solution because the volatile nature of acetone damages the microscope objective. The wafer can only be taken out from the chemical bay when a 100% elimination of the undesired ZnO layer is observed during microscope inspection.

Rapid Thermal Annealing: A Rapid Thermal Process was done to establish a bonding between ZnO and Underneath SiO_2 just after the lift-off process. RTP (Rapid Thermal Processing) technology rapidly heats silicon wafers to high temperatures, reaching up to 1100 °C in just a few seconds. However, to avoid dislocations and wafer breakage brought on by thermal shock, wafer temperatures must be gradually lowered during cooling. Available gases include N_2, Ar, O_2, and H_2. It can be used for Annealing Contact Alloying, Rapid Thermal Oxidation (RTO), Rapid Thermal Nitridation (RTN), Densification and Crystallization, Silicidation, etc.

After all this process there was a need for aluminium contact deposition at the source, drain, and gate terminal. The photolithography process was repeated followed by aluminium deposition and lift-off which have already been explained. The minimum feature size of the aluminium mask was found to be 20 μm. All the Photolithography steps included in this fabrication process were done inside a class 100 cleanroom under yellow light ambient so that the unnecessary polymerization of Chemical Photoresist can be avoided.

Deposition of Aluminium: An Aluminium layer of 100 nm thickness was deposited using the electron beam evaporation method and the rotation mode of deposition was preferred in our case because of better uniformity during deposition. The metal is heated in the electron-beam evaporation process so that it can be deposited. Thin films are achieved through a controlled deposition. Solid sources are capable of deposition of metals and dielectrics. The substance is held in a water-cooled crucible and subjected to the electron beam, which causes it to evaporate and condense on the wafers/samples. The deposition is homogenous because of the planetary substrate rotation system. For substrate heating, radiant heaters are offered. There is also an option for ion etching, ion-assisted deposition, and ion co-deposition. During the deposition process, a pressure of 2 x 10^{-7} torr must be maintained. To reduce source atom collisions with background material atoms, a high vacuum is required.

Aluminium Lift-off Process: The aluminium (Al) lift-off process was done exactly in a similar way that has already been discussed in the case of ZnO lift-off, ZnO is exchanged by aluminium in this case.

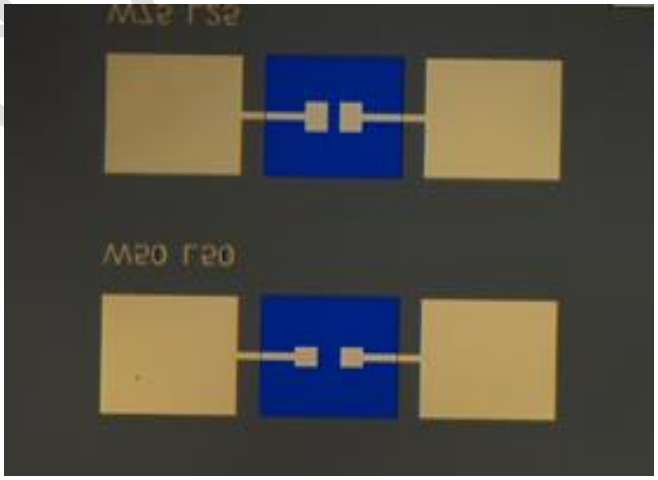

Figure 5. A single crystal silicon die containing two ZnO TFT

Figures 5 and Figure 6 were captured just after the successful aluminium lift-off process, the transparent blue area in Figure 5 and Figure 6 refers to ZnO and the aluminium contact looks like a golden-shaded area.

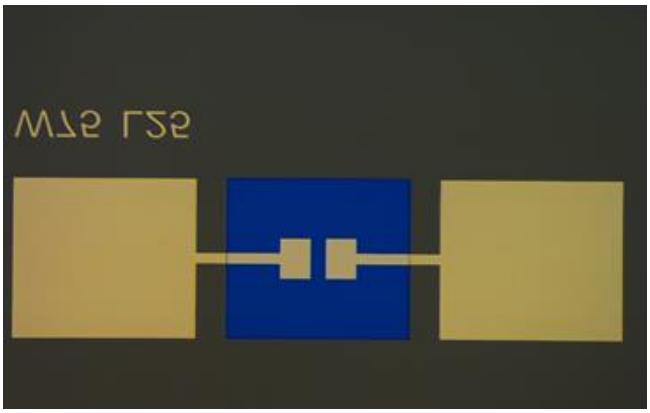

Figure 6. Zoomed view of a single TFT with a *W*/*L* ratio of 75/25

Forming Gas Annealing: The device was subjected to a 15-minute forming gas annealing process at 400 °C in an environment with a 9:1 ratio of nitrogen and hydrogen before being allowed to leave the clean room facility.

4 Result and discussion

TFT belongs to the family of new generation portable Field Effect Transistors. Like all our conventional Field Effect Transistors, it requires a thorough electrical characterization to be proven efficient in next-generation mobile smartphone display technologies. The choice of active material always plays the most significant role in deciding the ultimate performance of the fabricated transistor in our case, which is ZnO.

In this context, a bottom gate ZnO TFT is fabricated on a single crystal silicon die under a centralized contamination-free Clean Room Facility, and after its development, it is mounted on a Printed Circuit Board for proper electrical characterization. The final output wires are connected to the relevant PCB electrical contacts designated as Source, Drain, and Gates, respectively, to connect with the external Electrical probe station for characterization. All necessary transistor terminals, such as Source, Drain, Gate, and others, are wire bonded with the PCB electrical contacts.

A wafer level electrical characterization system also known as a DC Probe Station (PM5, Agilent Device Analyzer B1500A with pulsed source of 5 MHz) was used to perform the IV and CV measurements for the specific TFT. The characterization system's fundamental characteristics include superior IV measurement performance: measuring resolution of 0.1 fA/0.5 μV, Measurement features for the HV-SPGUs include direct control, arbitrary linear waveform generating GUI, single and multi-channel sweep, time sampling, list sweep, quasi-static CV (using the SMUs), a 10 ns pulsed I-V solution is available for characterizing samples, and an integrated capacitance module supports CV measurements between 1 kHz and 5 MHz.

ZnO TFT's transfer characteristics and output characteristics are shown in Figures 7 and 8, respectively, and an on/off current ratio that was derived from Figure 7 was found to be in the order of 2 x 10^8. At V_{DS} = 10 V and V_{GS} = 20 V, the highest drain current was determined to be 1 x 10^{-3} A, while the minimum drain current was determined to be 0.5 x 10^{-11} A at V_{DS} = 10 V and V_{GS} = −1.2V. Calculating the on/off current ratio was done using the data presented above. The Transfer Characteristics plot, however, makes it abundantly evident that our manufactured ZnO TFT is a depletion-type Field Effect Transistor with a negative threshold voltage.

Figure 9 explains a functional relationship between the device mobility and the applied gate to source voltage. The mobility of the transistor is an extraordinarily important parameter for describing the optimal performance of the resulting device on-chip. A very high magnitude of field-dependent mobility is the reason for the presence of a polycrystalline ZnO channel layer between SiO_2 and metallic contact. With increasing V_{GS}, the ratio of free carrier to fixed charge at the grain boundaries increases in proportion to the charge density of induced free carrier, resulting in a reduction of the potential barrier at the grain boundaries. A maximum saturation mobility of 48 cm^2/Vs was recorded at V_{GS} = 24.1 V and V_{DS} = 10 V. Some of the studies [28, 29, 31] were done in the past on ZnO nanostructures to prove their worth for potential high-speed device applications but this research clearly shows the novelty of ZnO TFT in terms of speed and power consumption. Furthermore, the magnitude of field-dependent mobility was compared with much recent literature shown in Table 1 to conclude the superiority of this device.

Figure 10 shows the Capacitance-Voltage characteristics for a wide range of frequencies, from 1 kHz to 1 MHz. According to the plot at 1 kHz, the accumulation zone is shown by the left-hand region of V_{GS} = −5V, the depletion zone is indicated by the region between −5 V and −1.2 V, and the strong inversion region by the region immediately to the right of V_{GS} = −1.2 V. The observed value of gate oxide capacitance at the frequency of 1 kHz was found to be 28.5 pF from the CV characteristics plot. It is discovered that the estimated value of V_{TH} from the CV measurement curve is −1.2 V. Figure 9 shows a clear example of the shift in threshold voltage towards the negative x-axis that interferes with the depletion-type operation of the TFT. At the point where the applied Gate voltage is larger than −1.2 V, a strong inversion effect causes the n-channel to be formed from the p-type silicon substrate.

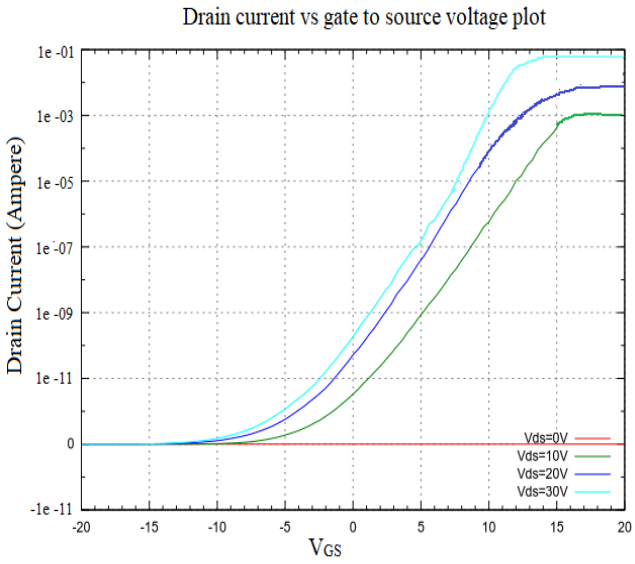

Figure 7. Drain current vs Gate to Source voltage plot of ZnO TFT

When a very high frequency (1 MHz) is reached, a differential change in capacitor voltage has no impact on the inversion layer

charge. The differential change in charge carrier occurs at the meal as well as the space charge region of the p-type semiconductor substrate. Therefore, the capacitance achieves a minimum value. The frequency dependence of the Capacitance-Gate Voltage plot can be visualized in Figure 10.

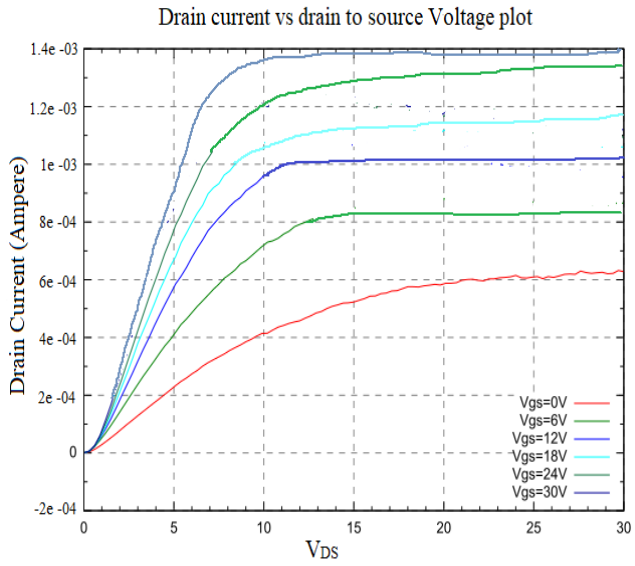

Figure 8. Drain current vs Drain to Source voltage plot

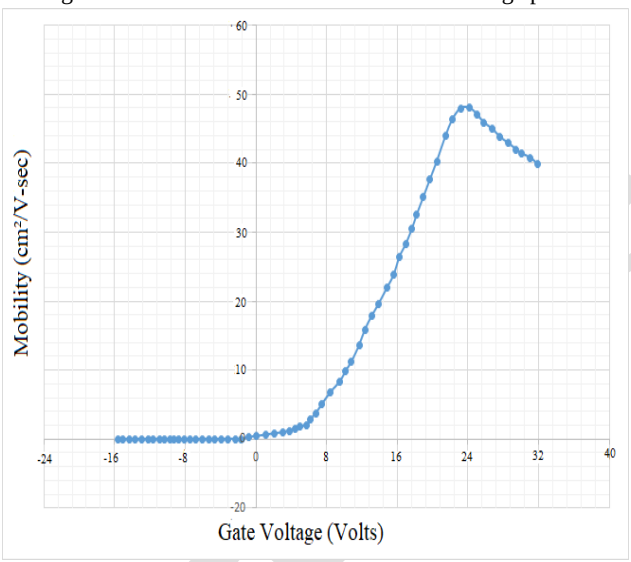

Figure 9. Field-dependent mobility plot

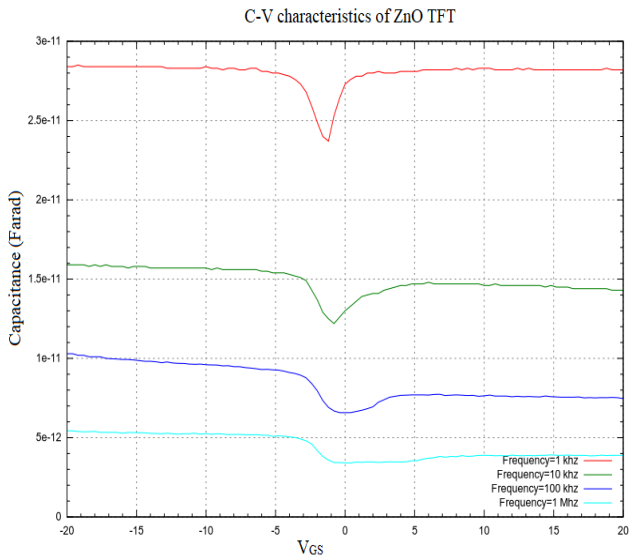

Figure 10: CV characteristics plot of ZnO TFT

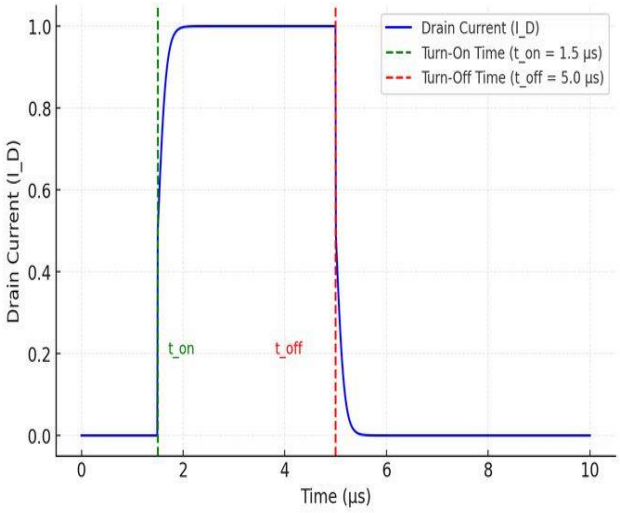

Figure 11: Transient response of ZnO TFT

To measure the transient response of a ZnO TFT fabricated on a single-crystal silicon (100) substrate, a Source Measure Unit (SMU), such as the Keithley 2460, is typically used. The SMU applies a pulsed gate voltage (V_G) to switch the device between its ON and OFF states, while a constant drain voltage (V_D = 10 V) is applied, and the normalized drain current (I_D) is monitored as a function of time. The transient response curve in Figure 11, showing I_D versus time, provides critical metrics: the turn-on time (t_{on}), defined as the time for I_D to reach 90% of its steady-state value when V_G transitions from OFF to ON, and the turn-off time (t_{off}), the time for I_D to drop to 10% of its steady-state value when V_G transitions from ON to OFF. The fabricated ZnO TFTs, known for high carrier mobility, typically exhibit t_{on} = 1.5 µs and t_{off} = 5 µs. This setup and analysis highlight the device's suitability for high-speed electronic applications.

The off current in the ZnO-TFT was measured at V_{DS} = 10 V, and V_{GS} = −1.2 as these values correspond to the depletion mode, ensuring the device operates at its minimum drain current ($I_{DS,off}$), which aligns with the threshold voltage (V_{TH}) experimentally determined from the capacitance-voltage (C-V) characteristics. The choice of these bias values allows for an accurate on/off current ratio calculation, as V_{TH} at −1.2 V, represents the onset of the depletion zone, consistent with the transfer characteristics. The threshold voltage (V_{TH}) was determined by analyzing the C-V curves, which delineated the transition between the depletion and inversion regimes. This analysis confirmed the negative V_{TH} observed in the transfer characteristics.

Sub-threshold conduction is a critical aspect of the ZnO-TFT, particularly for applications in energy-efficient display technologies where minimizing power consumption is essential. In the fabricated device, the sub-threshold leakage current, measured as the minimum drain current ($I_{DS,\,min}$) at V_{GS} = −1.8 V, is approximately 0.0001663×10^{-11} A with a calculated subthreshold slope of 0.075 V/Decade using two sets of values (V_{GS} = −1.2, I_D = 0.5 x 10^{-11}) and (V_{GS} = −1.8, I_D = 0.0001663 x 10^{-11}) putting into to relation mentioned in equation (1) shown below,

$$s = \left[\frac{\hat{a}^{\wedge}, ln\, I_{Ds}}{\hat{a}^{\wedge}, V_{Gs}}\right]^{-1}$$

(1)

This value indicates that sub-threshold conduction is minimal, highlighting the effective gate control over the channel in the depletion mode. A low sub-threshold leakage current reduces standby power consumption, making the device well-suited for portable and low-power applications such as next-generation displays. The implications of sub-threshold conduction are closely tied to the sub-threshold slope, which determines the voltage required for an order-of-magnitude increase in current. The reported low leakage current suggests efficient control in the sub-threshold regime. Including this discussion and potentially calculating the sub-threshold slope based on experimental data would strengthen the analysis of the ZnO-TFT's suitability for display applications.

Repeated measurements were conducted for key parameters, including mobility and on/off current ratios to ensure data reliability. The mobility of the ZnO TFT was measured with a maximum uncertainty of ±1.2 cm²/Vs, derived from variations in multiple measurements. Similarly, the on/off current ratio was determined with an error margin of ±5%, calculated based on fluctuations in the recorded drain current under consistent conditions. These measurements were performed using an Agilent Device Analyzer B1500A with a pulsed source of 5 MHz, which has a resolution of 0.1 fA/0.5 µV for current and voltage measurements, ensuring high precision. The reported data represent the mean values obtained from at least five measurements, with the standard deviations used to estimate the error margins.

ZnO is typically found to have an n-type structure. This n-type is caused by structural point defects (vacancies and interstitials) and extended defects (threading/planar dislocations). The n-type conductivity of the ZnO lattice is due to oxygen vacancies. The pre-existence of n-type nature creates an n channel in the ZnO thin film structure, resulting in electrical conduction at V_{GS} less than 0 volt and compels the TFT to be operated in the depletion mode.

Table 1 gives a survey of all potential ZnO-based TFTs along with their on/off current ratios and saturation mobility values. Both of these parameters are extremely crucial to determine the performance of a TFT. In this context, the fabricated ZnO TFT on a p-type single crystal Silicon substrate not only exhibits an extremely high value of on/off current but also exhibits a remarkable magnitude of field-dependent saturation mobility that was never reported before which implies a largely improved operating speed of the Transistor at the on-state condition.

Table 1. Different types of ZnO TFTs with their on/off current ratio and saturation mobility values

Different types of ZnO TFTs	**Associated on/off current ratio and Saturation mobility values**
Transparent ZnO thin-film transistor fabricated by rf magnetron sputtering [32]	on/off current ratio = 10^6 saturation mobility = 2 cm^2/Vs
Stable ZnO thin film transistors by fast open-air atomic layer deposition [33]	on/off current ratio = 10^8 saturation mobility = 10 cm^2/Vs
Improving the Gate Stability of ZnO Thin-Film Transistors with Aluminum Oxide Dielectric Layers [34]	on/off current ratio = 1.45 x 10^3 saturation mobility = 0.24 cm^2/Vs
Investigation on doping dependency of solution-processed Ga-doped ZnO thin film Transistor [35]	on/off current ratio = 4.17 x 10^6 saturation mobility = 1.63 cm^2/Vs
Fully flexible solution-deposited ZnO thin-film transistors [36]	on/off current ratio = 10^6 Saturation Mobility = 0.35 cm^2/Vs
Characteristics of ALD-ZnO Thin Film Transistor Using H_2O and H_2O_2 as Oxygen Sources [37]	on/off current ratio = 2 x 10^7 saturation mobility = 10.7 cm^2/Vs
Effects of yttrium doping on the electrical performances and stability of ZnO thin-film transistors [38]	on/off current ratio = 10^7 saturation mobility = 9.8 cm^2/Vs
Controllable Doping and Passivation of ZnO Thin Films by Surface Chemistry Modification to Design Low-cost and High-performance Thin Film Transistors [39]	on/off current ratio = 10^5 saturation mobility = 0.117 cm^2/Vs
Impact of electrode materials on the performance of amorphous IGZO thin-film transistors [40]	on/off current ratio = 10^7 to 10^8 saturation mobility = 24 to 50 cm^2/Vs

The fabricated ZnO TFT has been compared against amorphous silicon (a-Si) TFTs and IGZO TFTs, the most commonly used technologies in display applications that ZnO TFTs aim to replace. Amorphous silicon TFTs, known for their low field-effect mobility (0.1–1 cm²/Vs) [1], dominate low-cost display applications but are limited by slower response times. IGZO TFTs, with their significantly higher mobility (10–20 cm²/Vs) and excellent uniformity and stability, are more suited for high-end displays [14], [37]. In contrast, the fabricated ZnO TFT demonstrates a remarkable field-effect mobility of 48 cm²/Vs, significantly surpassing both a-Si and IGZO technologies. Furthermore, it exhibits a high on/off current ratio of 2×10^8, outperforming many reported IGZO devices [37]. ZnO TFTs can also be fabricated using cost-effective methods such as RF magnetron sputtering at room temperature [32], combining the performance advantages of IGZO TFTs with the scalability and affordability of a-Si TFTs.

A comparative analysis with IGZO TFTs studied by Tappertzhofen et al., 2022, further underscores the competitive performance of the ZnO TFT. While IGZO TFTs in Tappertzhofen's study achieved saturation mobilities ranging from 24 to 50 cm²/Vs and on/off ratios up to 10^8, depending on the electrode materials (Pt, W, or Ti) [40], the ZnO TFT from our study matches these benchmarks with a saturation mobility of 48 cm²/Vs and an on/off ratio of 2×10^8. Importantly, our research emphasizes low-cost fabrication using RF magnetron sputtering and Al electrodes, whereas Tappertzhofen et al. focused on optimizing IGZO TFTs with advanced electrode materials to enhance performance. Both studies highlight their devices' potential for high-resolution and flexible display applications. The

ZnO TFT stands out for its balance of excellent performance and cost-effective manufacturing, making it a strong candidate for next-generation display technologies.

An experiment was conducted on the depletion-type ZnO TFT with an initial threshold voltage V_{TH} of −1.2 V to study the effects of Negative Bias Stress (NBS). A gate voltage V_{GS} of −6 V was applied for stress durations of 10,000 s (2.8 hours) and 24 hours. The results showed a shift in threshold voltage ΔV_{TH} of approximately −0.4 V for the shorter stress duration, resulting in a final threshold voltage $V_{TH,\,final}$ of −1.6 V. For the extended stress duration of 24 hours, the ΔV_{TH} increased to −0.9 V, yielding a final $V_{TH,\,final}$ of −2.1 V. These observations confirm that the shift is attributed to charge trapping at the ZnO/dielectric interface and defect generation within the channel or dielectric layer, highlighting the device's stability under prolonged negative bias stress. This ensures the reliability of the fabricated ZnO TFT for smartphone display applications.

The term "improved" in the title is justified by the significant advancements demonstrated in this study. The fabricated ZnO Thin Film Transistor (TFT) exhibits an exceptionally high on/off current ratio of 2×10^8 and a maximum field-dependent saturation mobility of 48 cm^2/Vs, outperforming many previously reported ZnO-based TFTs (refer to Table 1 of the manuscript). These parameters highlight superior switching behavior and enhanced operational speed. Additionally, the use of RF magnetron sputtering at room temperature ensures a cost-effective and scalable fabrication process compared to more expensive techniques like PLD, making it suitable for mass production. The bottom-gate structure developed on a p-type single-crystal silicon substrate ensures high device quality and compatibility. These improvements position the ZnO TFT as a promising candidate for next-generation display technologies, addressing the demand for high-performance, low-power, and flexible devices, particularly in advanced laptop and smartphone displays.

The ZnO TFT fabrication process described in this study demonstrates significant potential for large-area display applications due to its scalability and cost-effectiveness. The use of RF magnetron sputtering ensures uniform ZnO deposition across extensive surfaces, which is critical for achieving consistency and reliability on large substrates, such as Gen 10 or Gen 11 mother glass commonly used in the display industry. Maskless UV photolithography, employed in this work, eliminates the need for expensive masks, enabling flexible and direct patterning over large areas. This approach can be scaled using industry-standard step-and-repeat or digital lithography techniques, further enhancing its applicability for mass production. The modular fabrication steps—such as SiO_2 etching, ZnO deposition, and Al metallization—can be easily adapted to automated processes and advanced systems like roll-to-roll sputtering for high-throughput manufacturing. Additionally, RF sputtering, a cost-effective alternative to methods like PLD, makes the process economically viable for industrial-scale production. Future work will focus on demonstrating the fabrication of large-area TFT arrays on substrates like flexible polymers, optimizing throughput and uniformity, and validating performance, yield, and scalability for flat-panel display applications.

5 Conclusion

This study demonstrated the successful development of a highly efficient ZnO-based Thin Film Transistor (TFT) fabricated using RF magnetron sputtering on a single-crystal silicon substrate. The device exhibited exceptional performance metrics, including an on/off current ratio of 2×10^8 and a maximum saturation mobility of 48 cm^2/Vs. All fabrication and characterization processes were conducted in a controlled cleanroom environment, maintaining a temperature of (24±3) °C and a relative humidity of 30–55%. These results establish the ZnO TFT as a strong candidate for next-generation smartphone and laptop displays, combining high operational speed, low power consumption, and scalability for large-area manufacturing. Furthermore, the cost-effective fabrication process using maskless photolithography and RF sputtering ensures its practical applicability for mass production.

Future research can explore further optimization of the ZnO TFT structure for flexible substrates, aiming to enhance mechanical durability while maintaining electrical performance. Such advancements could expand its potential applications, including foldable and wearable display technologies.

6 Conflicts of interest

The authors declare no conflict of interest.

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